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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569ecvjankgb

NOTE

The MPC8569E is also available without a security engine in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

The following figure shows the major functional units within the MPC8569E.

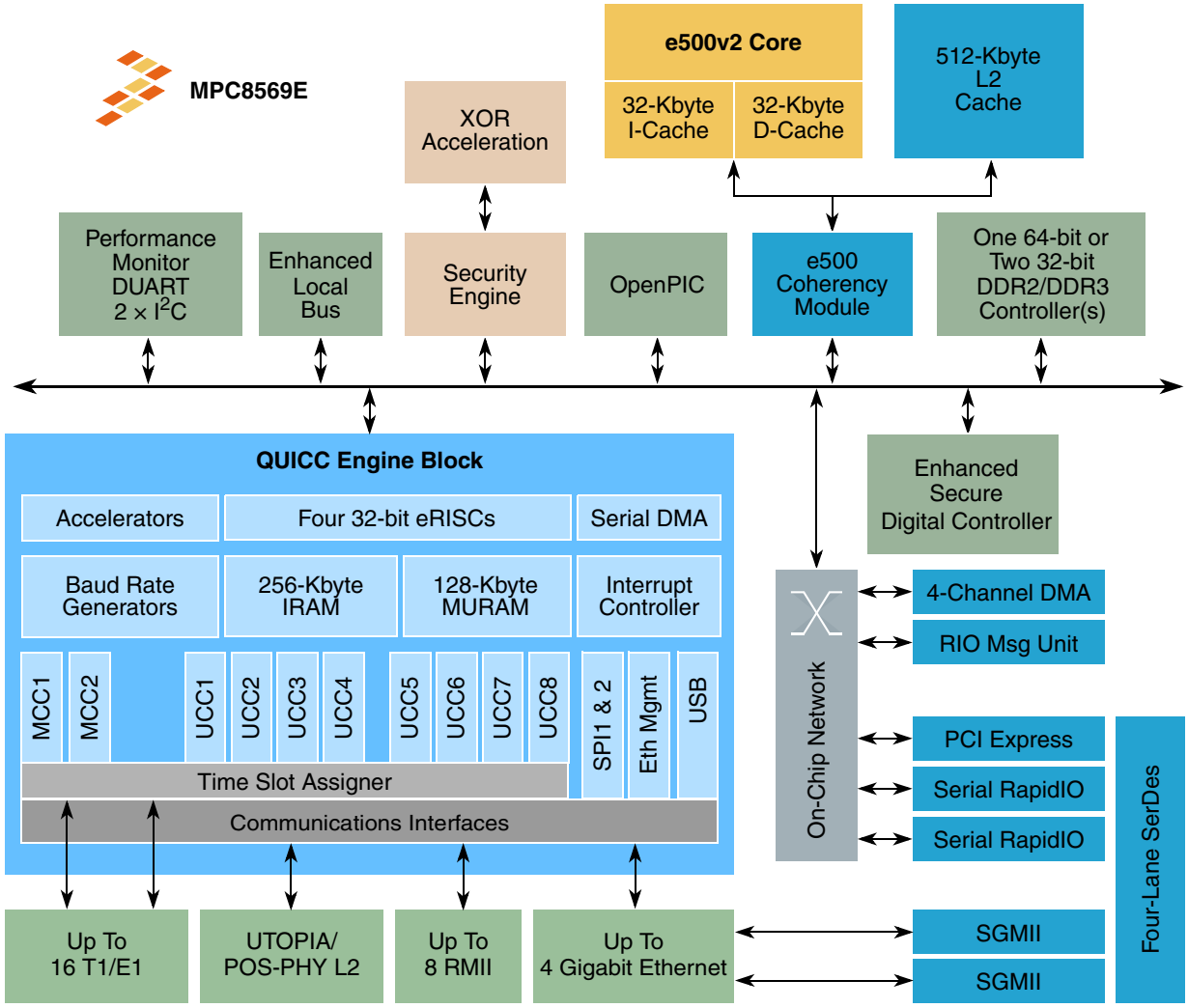


Figure 1. MPC8569E Block Diagram

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{D1\_MWE}}$	E17	O	GV_{DD}	—
D2_MA0	E4	O	GV_{DD}	—
D2_MA1	A4	O	GV_{DD}	—
D2_MA2	J7	O	GV_{DD}	—
D2_MA3	G6	O	GV_{DD}	—
D2_MA4	B4	O	GV_{DD}	—
D2_MA5	H4	O	GV_{DD}	—
D2_MA6	G3	O	GV_{DD}	—
D2_MA7	J8	O	GV_{DD}	—
D2_MA8	E5	O	GV_{DD}	—
D2_MA9	G5	O	GV_{DD}	—
D2_MA10	J6	O	GV_{DD}	—
D2_MA11	A5	O	GV_{DD}	—
D2_MA12	J9	O	GV_{DD}	—
D2_MA13	D3	O	GV_{DD}	—
D2_MA14	D6	O	GV_{DD}	—
D2_MA15	B1	O	GV_{DD}	—
D2_MBA0	J5	O	GV_{DD}	—
D2_MBA1	F4	O	GV_{DD}	—
D2_MBA2	E6	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	J4	O	GV_{DD}	—
D2_MCK0	E10	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	E9	O	GV_{DD}	—
D2_MCK1	J11	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	J10	O	GV_{DD}	—
D2_MCK2	C6	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	C5	O	GV_{DD}	—
D2_MCKE0	G7	O	GV_{DD}	—
D2_MCKE1	K8	O	GV_{DD}	—
D2_MCKE2	C2	O	GV_{DD}	—
D2_MCKE3	A2	O	GV_{DD}	—
$\overline{\text{D2\_MCS0}}$	E3	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	A6	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	H7	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	G2	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ28/D1_MDQ60	B10	I/O	GV_{DD}	—
D2_MDQ29/D1_MDQ61	A10	I/O	GV_{DD}	—
D2_MDQ30/D1_MDQ62	A8	I/O	GV_{DD}	—
D2_MDQ31/D1_MDQ63	A7	I/O	GV_{DD}	—
D2_MDQS0/D1_MDQS4	C12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$	C13	I/O	GV_{DD}	—
D2_MDQS1/D1_MDQS5	G12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$	F12	I/O	GV_{DD}	—
D2_MDQS2/D1_MDQS6	J13	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$	K14	I/O	GV_{DD}	—
D2_MDQS3/D1_MDQS7	D9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$	C9	I/O	GV_{DD}	—
D2_MDQS8	H9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	G9	I/O	GV_{DD}	—
D2_MECC0	G10	I/O	GV_{DD}	—
D2_MECC1	H8	I/O	GV_{DD}	—
D2_MECC2	G8	I/O	GV_{DD}	—
D2_MECC3	F7	I/O	GV_{DD}	—
D2_MECC4	F10	I/O	GV_{DD}	—
D2_MECC5	D8	I/O	GV_{DD}	—
D2_MECC6	E7	I/O	GV_{DD}	—
D2_MECC7	D7	I/O	GV_{DD}	—
D2_MODT0	C1	O	GV_{DD}	—
D2_MODT1	A3	O	GV_{DD}	—
D2_MODT2	H3	O	GV_{DD}	—
D2_MODT3	E1	O	GV_{DD}	—
D2_MAPAR_OUT	F1	O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	G1	I	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	G4	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	E2	O	GV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK0}}$	AF23	O	OV_{DD}	2
$\overline{\text{DMA\_DACK1}}$/MSRCID1	AD27	O	OV_{DD}	11
$\overline{\text{DMA\_DACK2}}$/SD_CMD	AD24	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE0}}$	AD25	O	OV_{DD}	2

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	H13	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H20	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K11	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K6	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K9	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L21	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L23	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to OV_{DD}.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Range	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD}_CORE AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	ScoreVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR2 and DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	2
QUICC Engine block Ethernet interface I/O voltage	$LV_{DD}1$	–0.3 to 3.63 –0.3 to 2.75	V	—

2.4.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.4.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 17. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 533 MHz data rate	V_{ILAC}	—	MVREF*n* – 0.20	V	—
	≤ 533 MHz data rate		—	MVREF*n* – 0.25		
AC input high voltage	> 533 MHz data rate	V_{IHAC}	MVREF*n* + 0.20	—	V	—
	≤ 533 MHz data rate		MVREF*n* + 0.25	—		

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.175	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.175	—	V	—

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 19. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications[3]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
800 MHz data rate		–200	200		1
667 MHz data rate		–240	240		1
533 MHz data rate		–300	300		1
400 MHz data rate		–365	365		1

2.4.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

The following table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[*n*] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
≤ 667 MHz		–0.6	0.6		

The following figure provides the AC test load for the DDR2 and DDR3 controller bus.

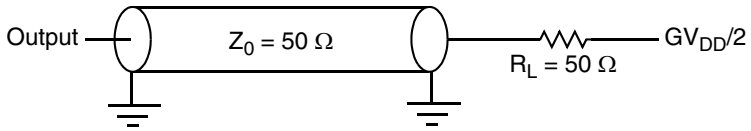


Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.5 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8569E.

2.5.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.5.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	—	3

Notes:

1. f_{CCB} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.6.3.2.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

The following figure shows the MII transmit AC timing diagram.

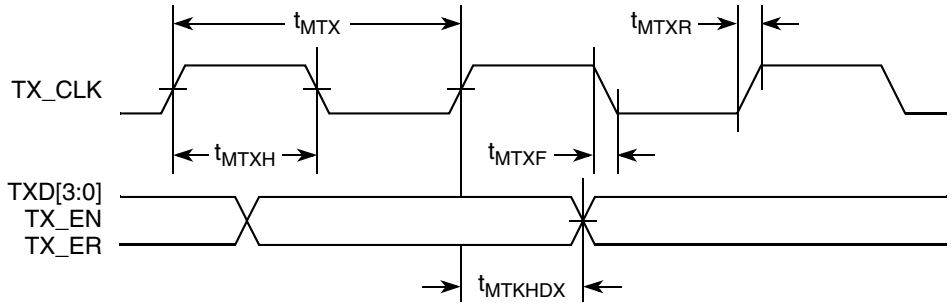


Figure 15. MII Transmit AC Timing Diagram

2.6.3.2.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns	1
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns	1
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	2
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the MII AC test load.

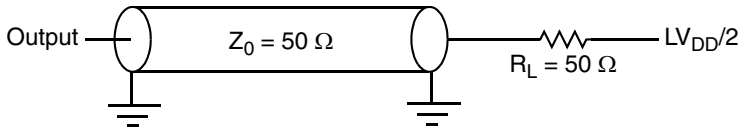


Figure 16. MII AC Test Load

The following figure shows the MII receive AC timing diagram.

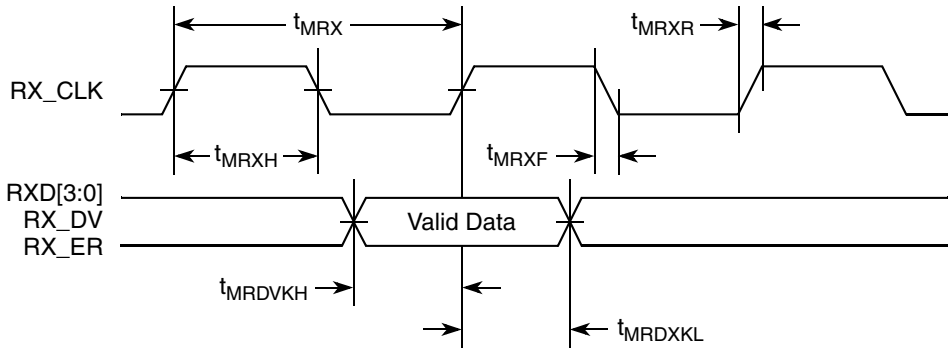


Figure 17. MII Receive AC Timing Diagram

2.6.3.3 SMII AC Timing Specification

The following table shows the SMII timing specifications.

Table 29. SMII Mode Signal Timing

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns	—
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns	—
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.5	ns	—

The following figure shows the SMII mode signal timing.

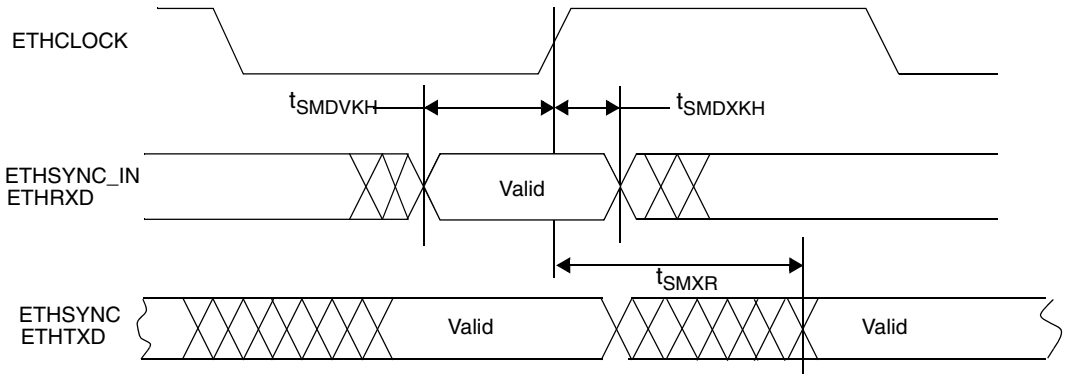


Figure 18. SMII Mode Signal Timing

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1.3	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 46. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

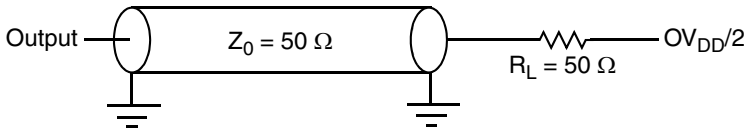


Figure 35. AC Test Load

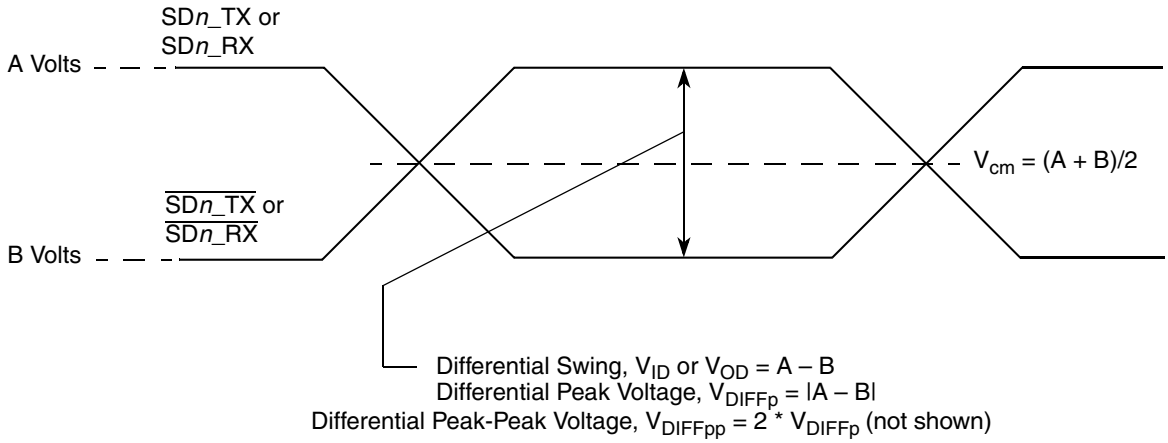


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 43 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TX} + V_{\overline{SD\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD*n*_REF_CLK) to falling edge rate (SD*n*_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6, 7

Notes:
1. **Caution:** Only 100 and 125 have been tested. In-between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 43.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 44.
7. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

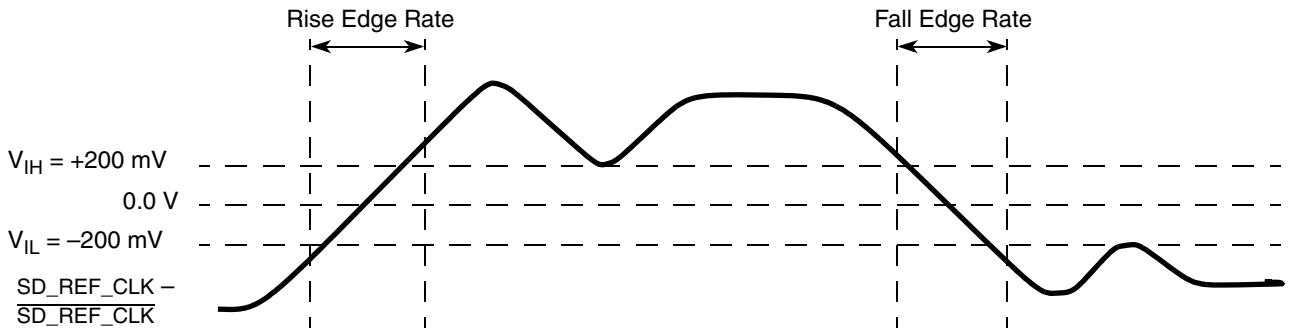


Figure 43. Differential Measurement Points for Rise and Fall Time

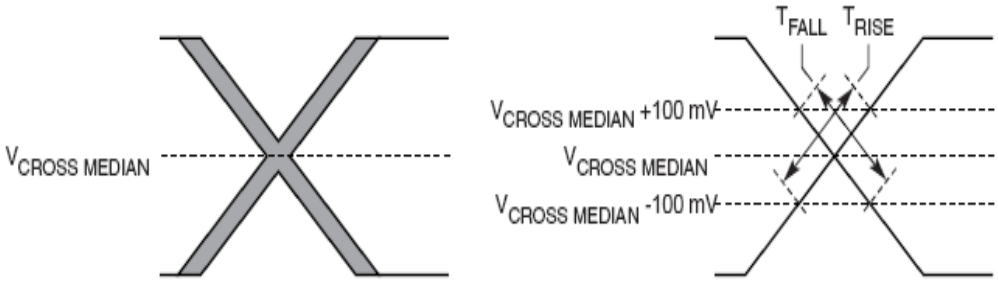


Figure 44. Single-Ended Measurement Points for Rise and Fall Time Matching

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. Measured at the package pins of the receiver.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.10.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.10.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum TX eye width	T_{TX-EYE}	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

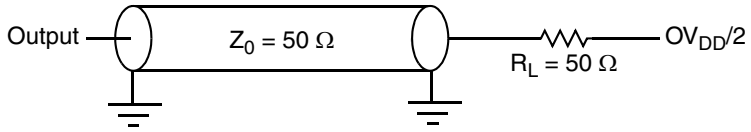
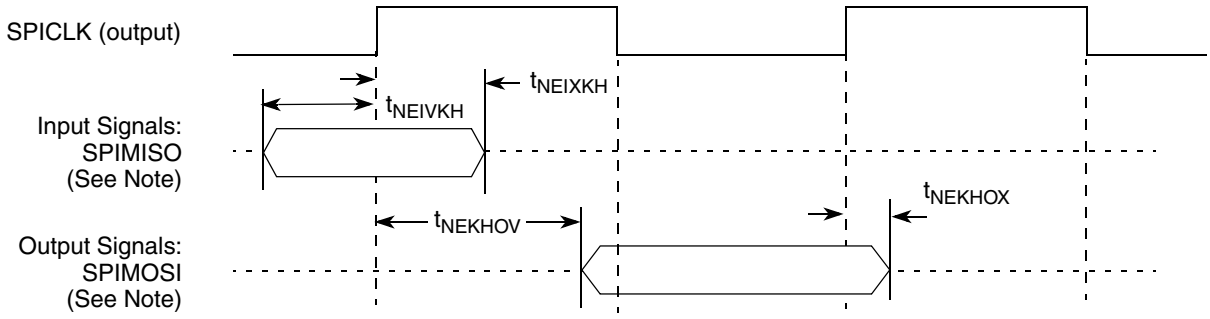


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

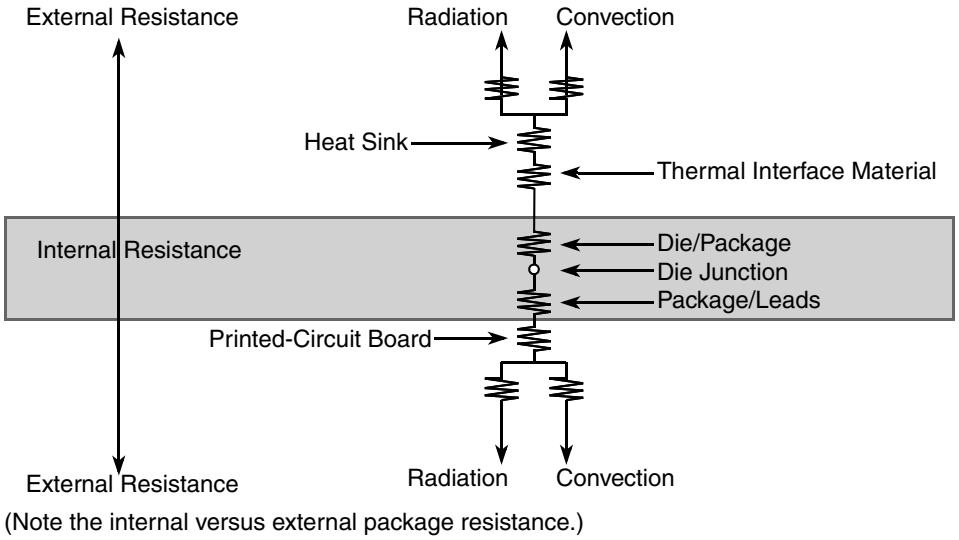


Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and the heat sink attach material (or thermal interface material), and to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 73).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.3.3 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the MPC8569E on-board temperature diode:

Operating range: 10 – 230 μA

Ideality factor over 13.5 – 220 μA; n = 1.006 +/- 0.008

4 Package Description

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters for the MPC8569E

The following table provides the package parameters for the FC-PBGA. The package type is 29 mm × 29 mm, 783 plastic ball grid array (FC-PBGA).

Table 83. Package Parameters

Parameter	PBGA
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (lead-free)	96.5% Sn 3% Ag 0.5% Cu