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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569ecvjaqljb

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to OV_{DD}.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Range	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD}_CORE AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	ScoreVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR2 and DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	2
QUICC Engine block Ethernet interface I/O voltage	$LV_{DD}1$	–0.3 to 3.63 –0.3 to 2.75	V	—

2.3.2 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the core complex bus clock (CCB_clk). The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB_clk. That is, minimum clock high time is $2 \times t_{CCB\_clk}$, and minimum clock low time is $2 \times t_{CCB\_clk}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.3.3 Gigabit Ethernet Reference Clock Timing

The following table provides the gigabit Ethernet reference clock (TX_CLK) AC timing specifications.

Table 12. TX_CLK[3,4] AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV / 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
TX_CLK frequency	t_{G125}	—	125	—	MHz	—
TX_CLK cycle time	t_{G125}	—	8	—	ns	—
TX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1, 5
TX_CLK duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 5
TX_CLK jitter	—	—	—	± 150	ps	2, 5

Notes:

1. Rise and fall times for TX_CLK are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V, and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. TX_CLK is used to generate the GTX clock for the UEC transmitter with 2% degradation. The TX_CLK duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the UEC GTX_CLK. See Section 2.6.3.7, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Gigabit transmit 125-MHz source. This signal must be generated externally with a crystal or oscillator, or is sometimes provided by the PHY. TX_CLK is a 125-MHz input into the UCC Ethernet Controller and is used to generate all 125-MHz related signals and clocks in the following modes: GMII, TBI, RTBI, RGMII.
4. For GMII and TBI modes, TX_CLK is provided to UCC1 through QE_PC[8:11,14,15] (CLK9-12,15,16) and to UCC2 through QE_PC[2,3,6,7,15:17](CLK3,4,7,8,16:18). For RGMII and RTBI modes, TX_CLK is provided to UCC1 and UCC3 through QE_PC11(CLK12) and to UCC2 and UCC4 through QE_PC16 (CLK17).
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

2.3.4 Other Input Clocks

A description of the overall clocking of this device is available in the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and Enhanced Local Bus see the specific interface section.

2.4 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8569E. Note that the required GV_{DD}(typ) is 1.8 V for DDR2 SDRAM and GV_{DD}(typ) is 1.5 V for DDR3 SDRAM.

2.6.3.4 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.6.3.4.1 RMII Transmit AC Timing Specifications

The following table shows the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMT}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMTH}	35	—	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	4.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	4.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

The following figure shows the RMII transmit AC timing diagram.

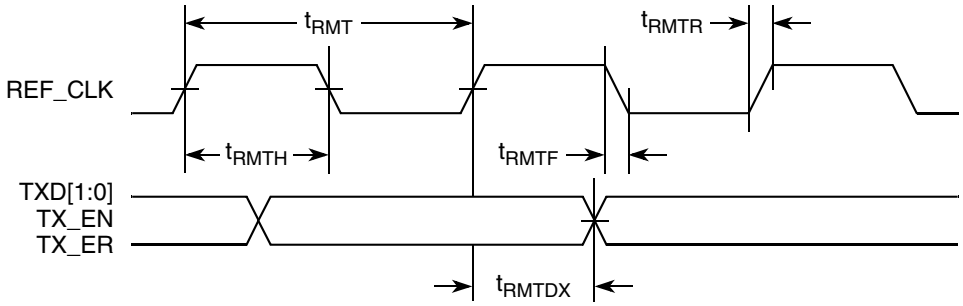


Figure 19. RMII Transmit AC Timing Diagram

2.6.3.4.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMR}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMRH}	35	—	65	%	1
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	1
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1

2.6.3.5.1 TBI Transmit AC Timing Specifications

The following table provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}	1.0	—	—	ns	1
GTX_CLK rise (20%–80%)	t_{TTXZ}	0.7	—	—	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	0.7	—	—	ns	—

Note:

1. Data valid t_{TTKHDV} to GTX_CLK minimum setup time is a function of clock and maximum hold time (min setup = cycle time – max delay).

The following figure shows the TBI transmit AC timing diagram.

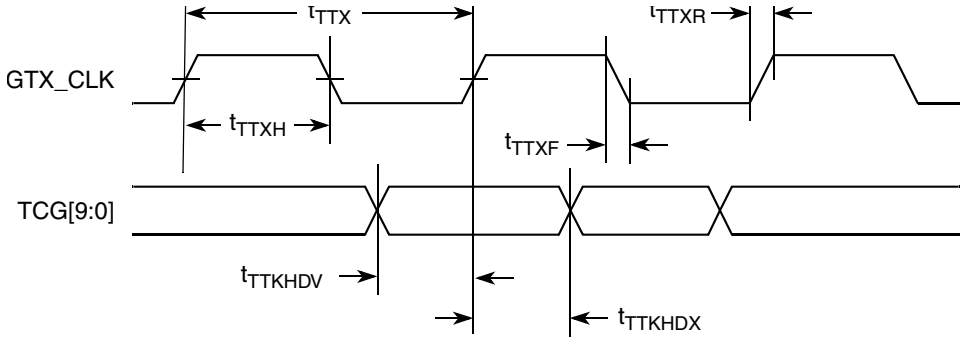


Figure 22. TBI Transmit AC Timing Diagram

2.6.3.5.2 TBI Receive AC Timing Specifications

The following table provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	1
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	2
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	—

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.6.4.1.2 SGMII Transmit DC Timing Specifications

Table 36 and Table 37 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs, SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*], as shown in Figure 28.

Table 36. SGMII DC Transmitter Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	320.0	500.0	725.0	mV	Equalization setting: 1.0×
		293.8	459.0	665.6		Equalization setting: 1.09×
		266.9	417.0	604.7		Equalization setting: 1.2×
		240.6	376.0	545.2		Equalization setting: 1.33×
		213.1	333.0	482.9		Equalization setting: 1.5×
		186.9	292.0	423.4		Equalization setting: 1.71×
		160.0	250.0	362.5		Equalization setting: 2.0×

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

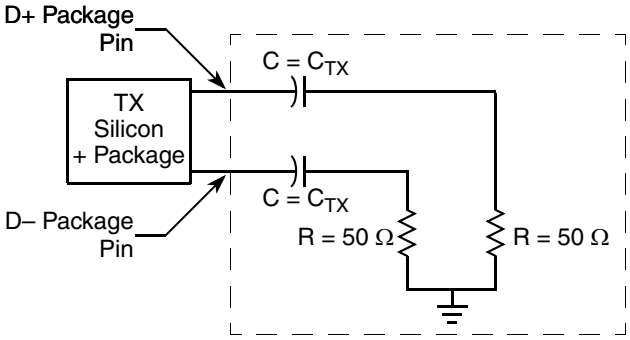


Figure 29. SGMII AC Test/Measurement Load

2.6.5 QUICC Engine Block IEEE 1588 Electrical Characteristics

2.6.5.1 QUICC Engine Block IEEE 1588 DC Specifications

The following table shows the QUICC Engine block IEEE 1588 DC specifications when operating from a 3.3 V supply.

Table 40. QUICC Engine Block IEEE 1588 DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = OV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbols referenced in Table 2 and Table 3.

2.6.5.2 QUICC Engine Block IEEE 1588 AC Specifications

The following table provides the QUICC Engine block IEEE 1588 AC timing specifications.

Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 7$	ns	1, 3
QE_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	5
QE_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	5
Rise time QE_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	5
Fall time QE_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	5
QE_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
QE_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
QE_1588_PPS_OUT	$t_{T1588OV}$	0.5	—	4.0	ns	—

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
AC-coupling capacitor	C_{TX}	75	—	200	nF	All transmitters are AC-coupled. The AC-coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The MPC8569E SerDes transmitter does not have CTX built-in. An external AC-coupling capacitor is required.

2.10.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

The following table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 52. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

(RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A – B volts
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts

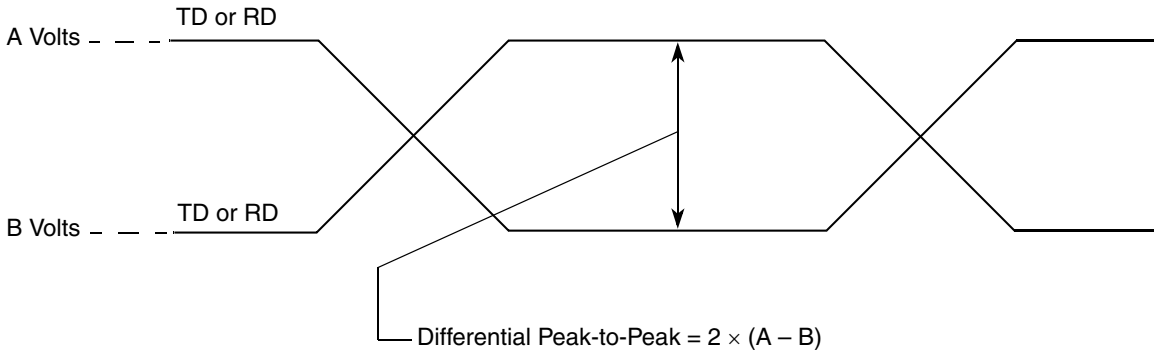


Figure 47. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.11.2 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- Pre-emphasis on the transmitter
- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Table 62. JTAG AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times: Boundary-scan data TDO	t_{JTKLDV}	 — —	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the AC test load for TDO and the boundary-scan outputs of the device.

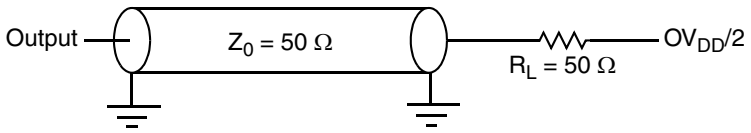


Figure 52. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

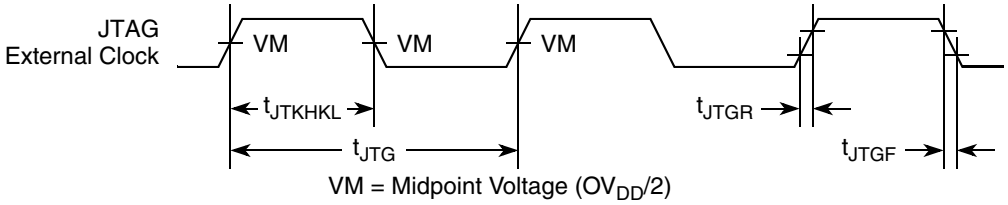


Figure 53. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

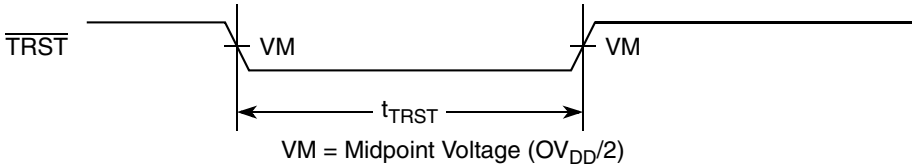


Figure 54. $\overline{\text{TRST}}$ Timing Diagram

The following figure provides the boundary-scan timing diagram.

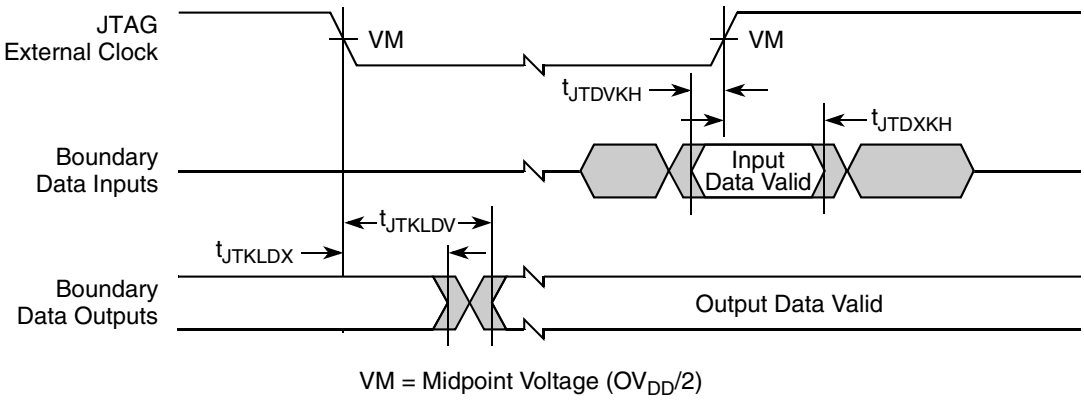


Figure 55. Boundary-Scan Timing Diagram

2.15 Enhanced Local Bus Controller

This section describes the DC and AC electrical specifications for the enhanced local bus interface of the MPC8569E.

2.15.1 Enhanced Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 3.3 V DC.

Table 63. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, “Recommended Operating Conditions.”

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 2.5 V DC.

Table 64. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 1.8 V DC.

Table 65. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

2.15.2 Enhanced Local Bus AC Electrical Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.15.2.1 Test Condition

The following figure provides the AC test load for the enhanced local bus.

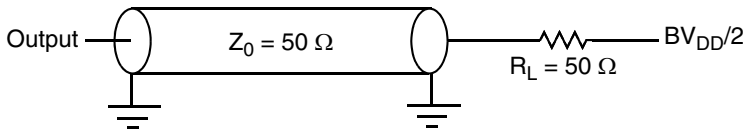


Figure 56. Enhanced Local Bus AC Test Load

The following figure shows the AC timing diagram for PLL bypass mode.

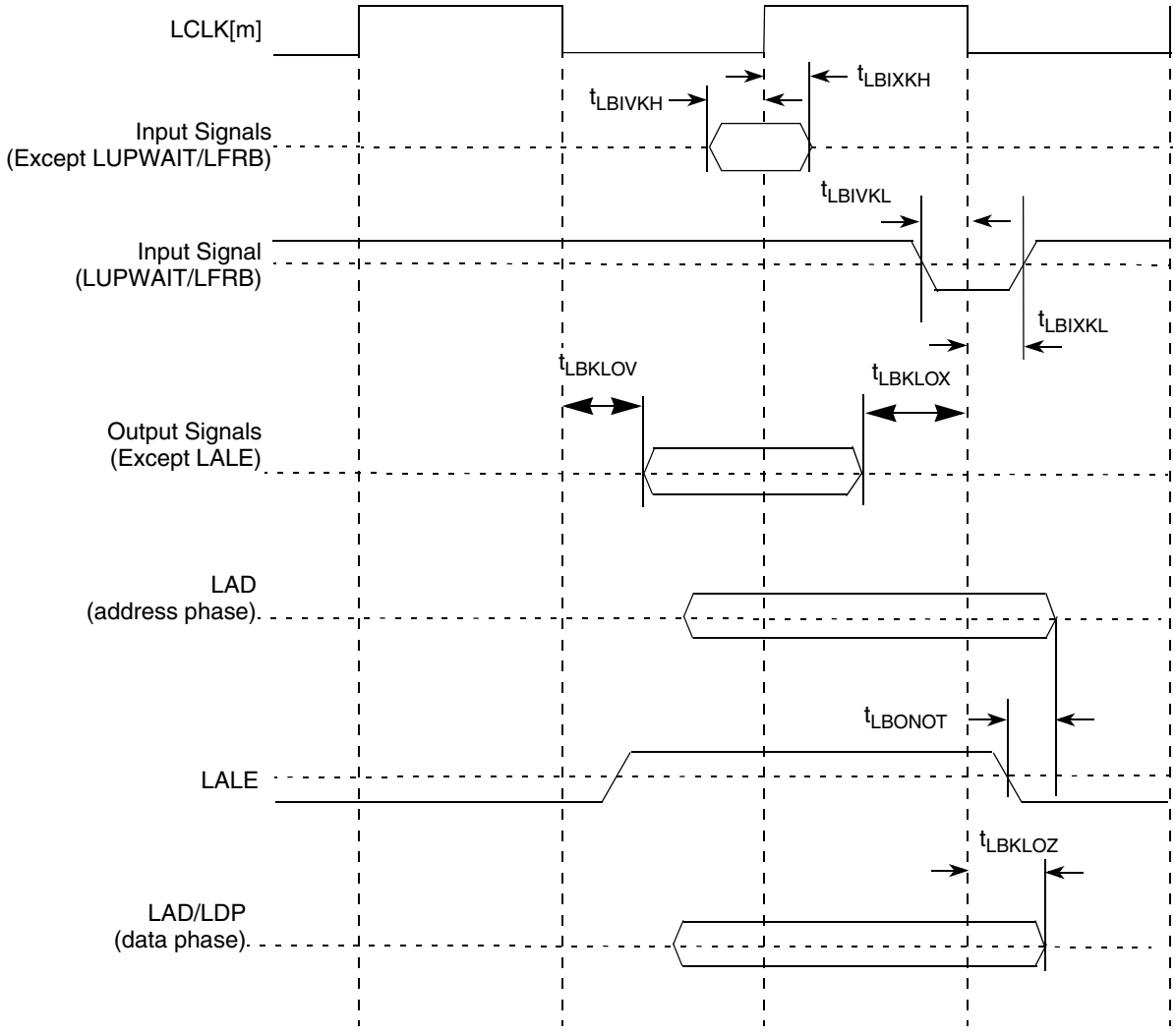


Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

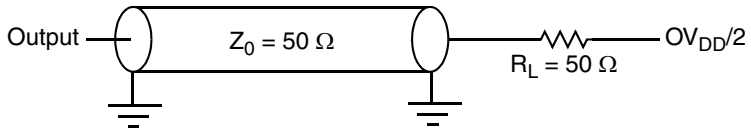


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

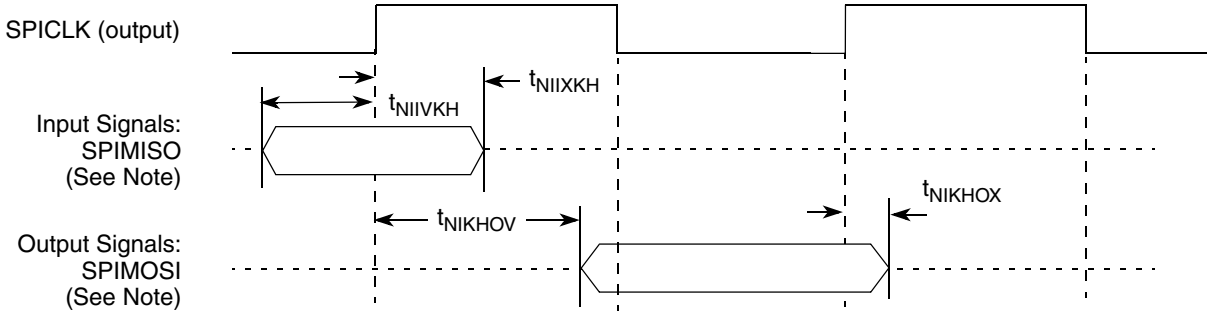
Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

Table 77. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

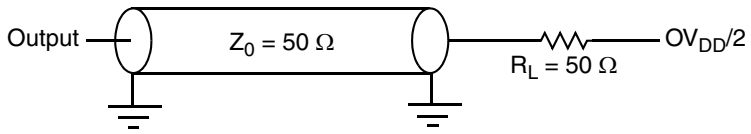
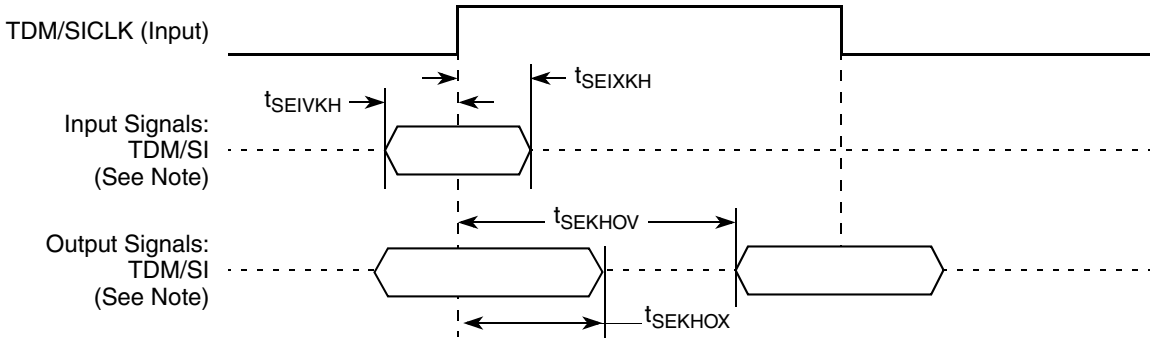


Figure 67. TDM/SI AC Test Load

The below figure represents the AC timing from Table 77. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. The following figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 68. TDM/SI AC Timing (External Clock) Diagram