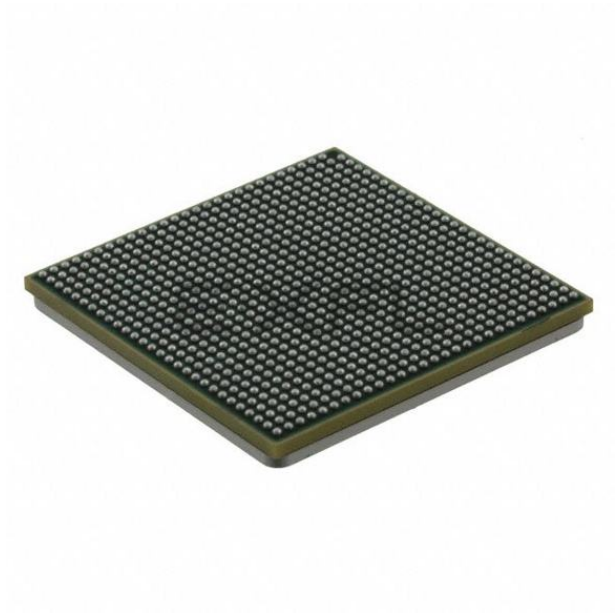


**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500v2 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 800MHz |
| Co-Processors/DSP | Communications; QUICC Engine, Security; SEC |
| RAM Controllers | DDR2, DDR3, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (8), 1Gbps (4) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.0V, 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569ecvtankgb |

## 1.2 Pinout List

The following table provides the pinout listing for the MPC8569E 783 FC-PBGA package.

**Table 1. MPC8569E Pinout Listing**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **Clocks** | | | | |
| RTC | M25 | I | $OV_{DD}$ | — |
| SYSCLK | P25 | I | $OV_{DD}$ | — |
| **DDR SDRAM Memory Interface** | | | | |
| D1_MA0 | E18 | O | $GV_{DD}$ | — |
| D1_MA1 | A18 | O | $GV_{DD}$ | — |
| D1_MA2 | H19 | O | $GV_{DD}$ | — |
| D1_MA3 | G20 | O | $GV_{DD}$ | — |
| D1_MA4 | B18 | O | $GV_{DD}$ | — |
| D1_MA5 | H18 | O | $GV_{DD}$ | — |
| D1_MA6 | C18 | O | $GV_{DD}$ | — |
| D1_MA7 | J21 | O | $GV_{DD}$ | — |
| D1_MA8 | E19 | O | $GV_{DD}$ | — |
| D1_MA9 | G19 | O | $GV_{DD}$ | — |
| D1_MA10 | J18 | O | $GV_{DD}$ | — |
| D1_MA11 | A19 | O | $GV_{DD}$ | — |
| D1_MA12 | J22 | O | $GV_{DD}$ | — |
| D1_MA13 | A15 | O | $GV_{DD}$ | — |
| D1_MA14 | D20 | O | $GV_{DD}$ | — |
| D1_MA15 | C15 | O | $GV_{DD}$ | — |
| D1_MBA0 | K17 | O | $GV_{DD}$ | — |
| D1_MBA1 | F18 | O | $GV_{DD}$ | — |
| D1_MBA2 | E20 | O | $GV_{DD}$ | — |
| $\overline{\text{D1\_MCAS}}$ | J17 | O | $GV_{DD}$ | — |
| D1_MCK0 | E24 | O | $GV_{DD}$ | — |
| $\overline{\text{D1\_MCK0}}$ | E23 | O | $GV_{DD}$ | — |
| D1_MCK1 | J24 | O | $GV_{DD}$ | — |
| $\overline{\text{D1\_MCK1}}$ | J23 | O | $GV_{DD}$ | — |
| D1_MCK2 | C20 | O | $GV_{DD}$ | — |
| $\overline{\text{D1\_MCK2}}$ | C19 | O | $GV_{DD}$ | — |
| D1_MCKE0 | G21 | O | $GV_{DD}$ | — |
| D1_MCKE1 | J20 | O | $GV_{DD}$ | — |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $V_{DD}$ | Y12 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | Y14 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | Y18 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $BV_{DD}$ | AC15 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC17 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC19 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC21 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF15 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF17 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF19 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF21 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $GV_{DD}$ | B12 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B16 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B19 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B2 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $GV_{DD}$ | H13 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H16 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H2 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H20 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H24 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H27 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | H5 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | J19 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | J3 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K10 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K11 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K18 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K22 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K26 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K3 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K4 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K6 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | K9 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | L15 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | L21 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | L23 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $LV_{DD}1$ | R4 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}1$ | — |
| $LV_{DD}1$ | R6 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}1$ | — |
| $LV_{DD}1$ | T10 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}1$ | — |
| $LV_{DD}2$ | M10 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}2$ | — |
| $LV_{DD}2$ | M3 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}2$ | — |
| $LV_{DD}2$ | M7 | 3.3-/2.5-V Ethernet power supply | $LV_{DD}2$ | — |
| $OV_{DD}$ | AB9 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AC5 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AE11 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AE2 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AE27 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AF24 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | AF7 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | M26 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | N23 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | W10 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | W6 | 3.3-V power supply | $OV_{DD}$ | — |
| $OV_{DD}$ | Y2 | 3.3-V power supply | $OV_{DD}$ | — |
| ScoreVDD | AA28 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | AC27 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | R27 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | T25 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | U28 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | V26 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | W27 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |
| ScoreVDD | Y25 | 1.0-V/1.1-V SerDes power supply | ScoreVDD | — |

### Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQ/MECC/MDM output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | | ps | 5 |
| 800 MHz | | 280[7]<br>320[8] | — | | |
| 667 MHz | | 400[7]<br>450[8] | — | | |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | | ps | 5 |
| 800 MHz | | 280[7]<br>320[8] | — | | |
| 667 MHz | | 400[7]<br>450[8] | — | | |
| 533 MHz | | 538 | — | | |
| 400 MHz | | 700 | — | | |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rate and in DDR3 mode to 667 and 800 MHz data rate.
7. DDR3 only
8. DDR2 only

## NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

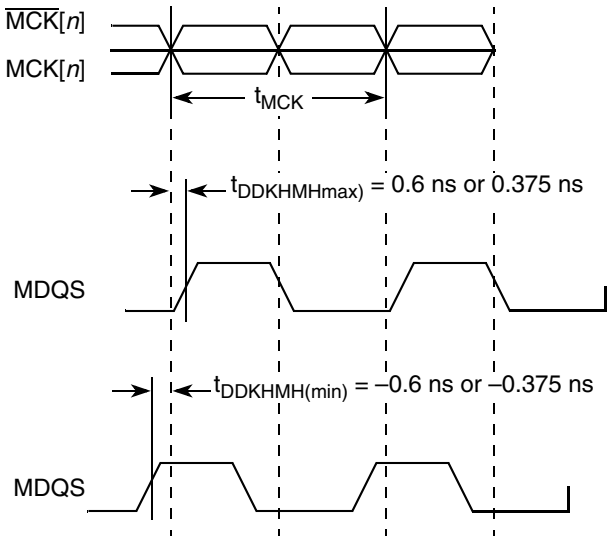



**Figure 9. Timing Diagram for $t_{DDKHMH}$**

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

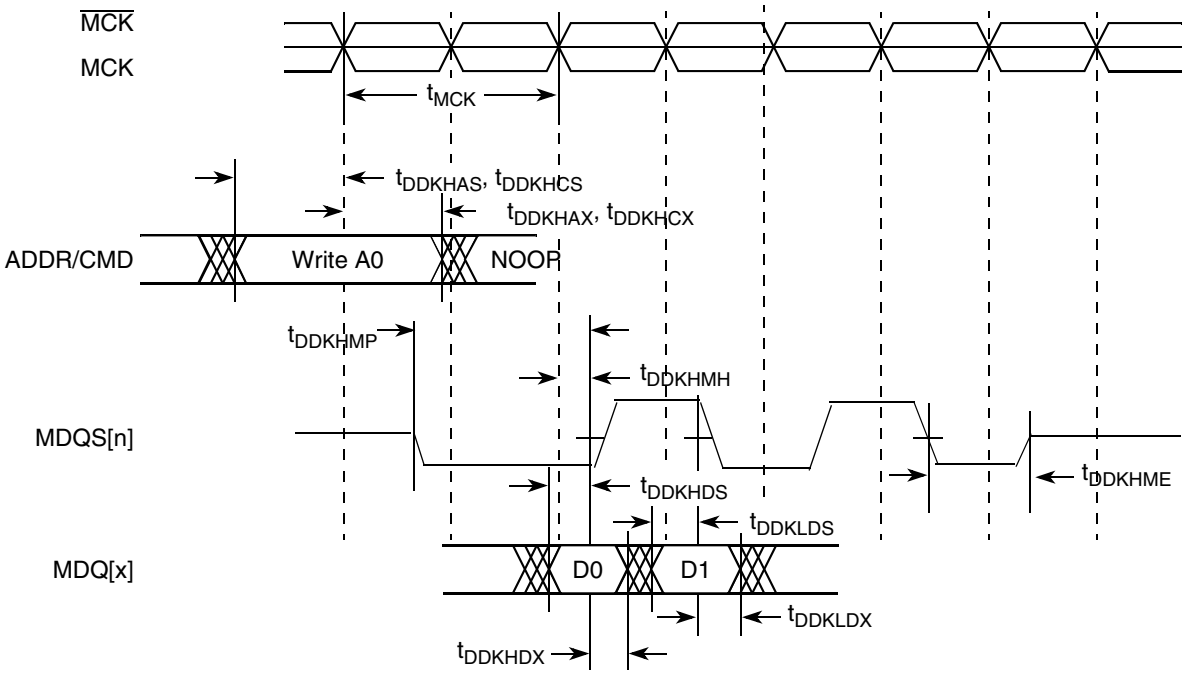



**Figure 10. DDR2 and DDR3 Output Timing Diagram**

#### 2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

**Table 26. GMII Receive AC Timing Specifications**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | 7.5 | — | — | ns | 1 |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 35 | — | 65 | % | 2 |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns | — |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0.2 | — | — | ns | — |
| RX_CLK clock rise time (20%–80%) | $t_{GRXR}$ | — | — | 1.0 | ns | 2 |
| RX_CLK clock fall time (80%–20%) | $t_{GRXF}$ | — | — | 1.0 | ns | 2 |

**Note:**
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

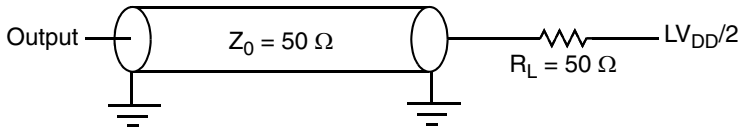



**Figure 13. GMII AC Test Load**

The following figure shows the GMII receive AC timing diagram.

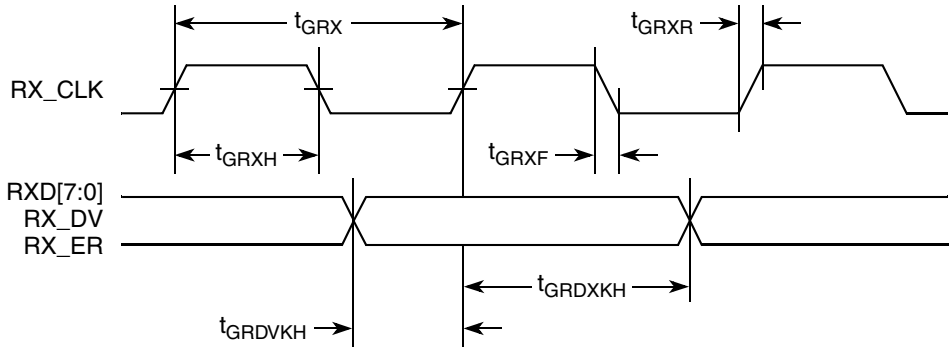



**Figure 14. GMII Receive AC Timing Diagram**

### 2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

**Table 31. RMII Receive AC Timing Specifications (continued)**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Fall time REF_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 4.0 | ns | 1 |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns | — |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns | — |

**Note:**

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

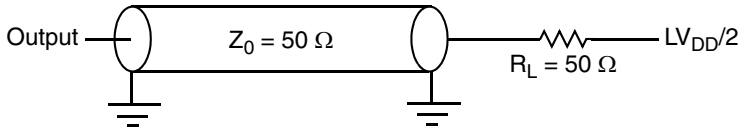



**Figure 20. AC Test Load**

The following figure shows the RMII receive AC timing diagram.

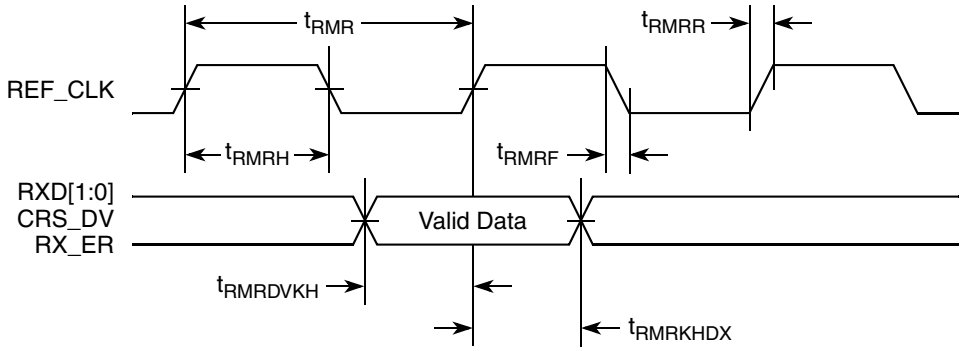



**Figure 21. RMII Receive AC Timing Diagram**

## 2.6.3.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 2.7.1.1 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

**Table 43. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ = 3.3 V ± 5%.

| Parameter | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO valid | $t_{MDKHDV}$ | $2\times(t_{plb\_clk}*8)$ | — | — | ns | 4 |
| MDC to MDIO delay | $t_{MDKHDX}$ | $(16 \times t_{plb\_clk}) - 3$ | — | $(16 \times t_{plb\_clk}) + 3$ | ns | 3, 4, 5 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 10 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| MDC fall time | $t_{MDCF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the Mgmt Clock CE_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. $t_{plb\_clk}$ is the QUICC Engine block clock/2.
5. MDC to MDIO Data valid $t_{MDKHDV}$ is a function of clock period and max delay time ($t_{MDKHDX}$).
(Min setup = cycle time – max delay

The following figure shows the MII management AC timing diagram.

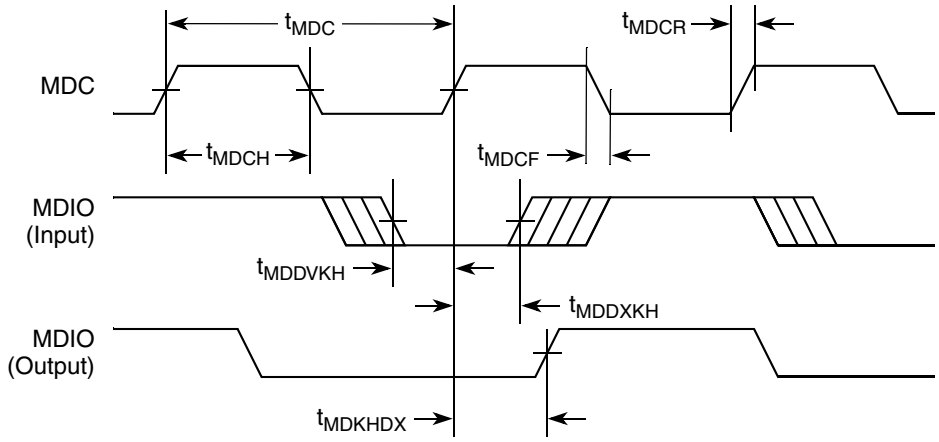



**Figure 34. MII Management Interface Timing Diagram**

# 2.8 HDLC, BISYNC, Transparent, and Synchronous UART Interfaces

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART interfaces of the MPC8569E.

## 2.8.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the HDLC, BISYNC, Transparent, and synchronous UART interfaces.

**Table 44. HDLC, BISYNC, and Transparent DC Electrical Characteristics**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. The min $V_{IL}$and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

## 2.8.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

The following table provides the input and output AC timing specifications for the HDLC, BISYNC, and Transparent protocols.

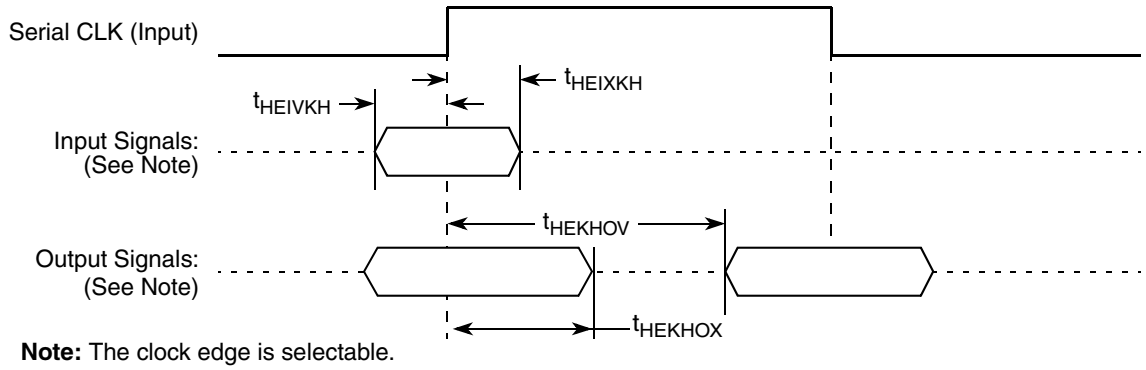
**Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications**

For recommended operating conditions, see Table 3

| Characteristic | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Outputs—Internal clock delay | $t_{HIKHOV}$ | 0 | 5.5 | ns | 2 |
| Outputs—External clock delay | $t_{HEKHOV}$ | 1 | 8.4 | ns | 2 |
| Outputs—Internal clock high Impedance | $t_{HIKHOX}$ | 0 | 5.5 | ns | 2 |
| Outputs—External clock high Impedance | $t_{HEKHOX}$ | 1 | 8 | ns | 2 |
| Inputs—Internal clock input setup time | $t_{HIIVKH}$ | 6 | — | ns | — |

Figure 36 and Figure 37 represent the AC timing from Table 45 and Table 46. Note that although the specifications generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also note that the clock edge is selectable.

The following figure shows the timing with external clock.




**Note:** The clock edge is selectable.

**Figure 36. AC Timing (External Clock) Diagram**

The following figure shows the timing with internal clock.

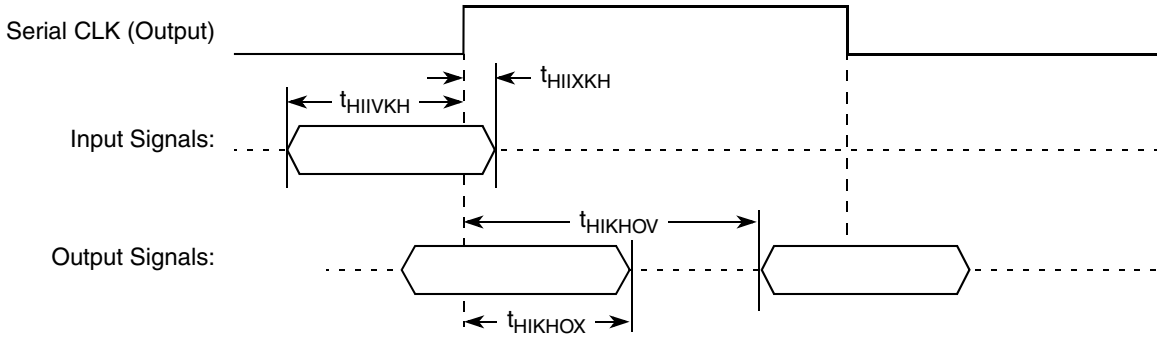



**Figure 37. AC Timing (Internal Clock) Diagram**

## 2.9 High-Speed SerDes Interfaces (HSSI)

The MPC859E features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications.The SerDes interface can be used for PCI Express and/or Serial RapidIO and/or SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

### 2.9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The below figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

The following table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 52. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications**

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

| Parameter | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Unit interval | UI | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1. |
| Minimum receiver eye width | $T_{RX-EYE}$ | 0.4 | — | — | UI | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 4. |

**Notes:**

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

**Table 58. I²C AC Timing Specifications (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | 0.1 × $OV_{DD}$ | — | V | — |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | 0.2 × $OV_{DD}$ | — | V | — |
| Capacitive load for each bus line | Cb | — | 400 | pF | — |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum $t_{I2OVKL}$ must be met only if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.

The following figure provides the AC test load for the I²C.

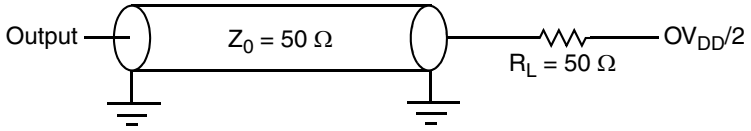



**Figure 49. I²C AC Test Load**

The following figure shows the AC timing diagram for the I²C bus.

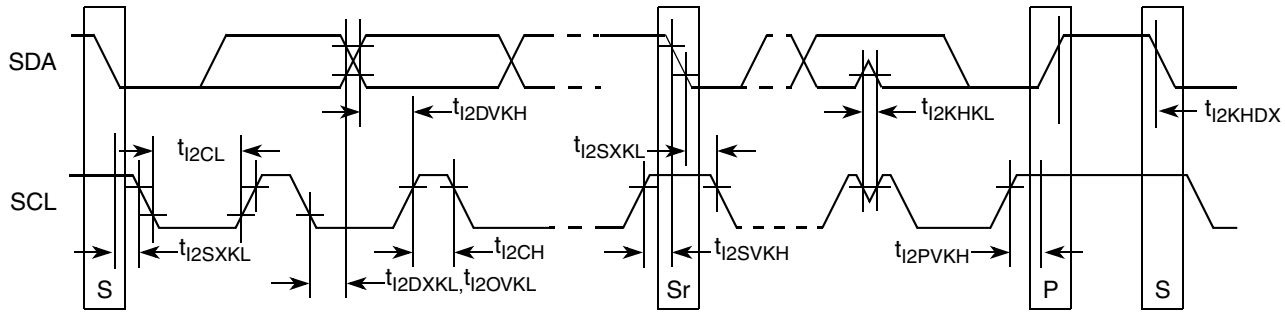



**Figure 50. I²C Bus AC Timing Diagram**

The following figure shows the AC timing diagram for PLL bypass mode.

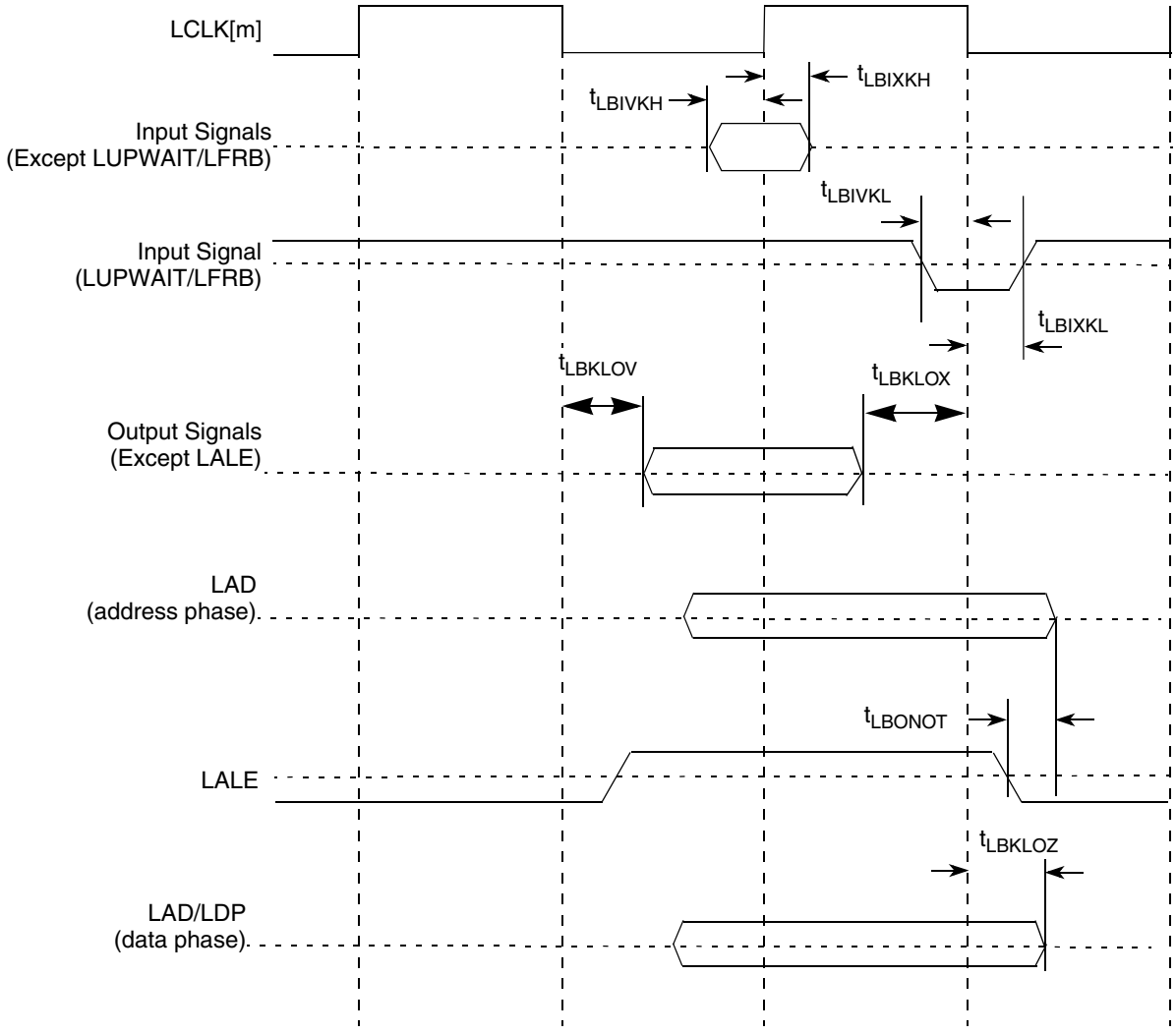



**Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)**

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by $t_{acs}$ (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

### 2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

**Table 71. Timers Input AC Timing Specifications**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Typ | Unit | Notes |
|---|---|---|---|---|
| Timers inputs—minimum pulse width | $t_{TIWID}$ | 20 | ns | 1, 2 |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least $t_{TIWID}$ ns to ensure proper operation.

The following figure provides the AC test load for the timers.

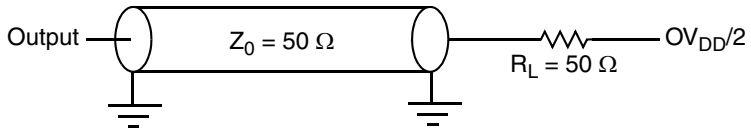



**Figure 63. Timers AC Test Load**

## 2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

### 2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

**Table 72. PIC DC Electrical Characteristics**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

**Table 75. SPI AC Timing Specifications (continued)**

For recommended operating conditions, see Table 3

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SPI inputs—Master mode (internal clock) input setup time | $t_{NIIVKH}$ | 4 | — | ns | — |
| SPI inputs—Master mode (internal clock) input hold time | $t_{NIIXKH}$ | 0 | — | ns | — |
| SPI inputs—Slave mode (external clock) input setup time | $t_{NEIVKH}$ | 4 | — | ns | — |
| SPI inputs—Slave mode (external clock) input hold time | $t_{NEIXKH}$ | 2 | — | ns | — |

**Note:**

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

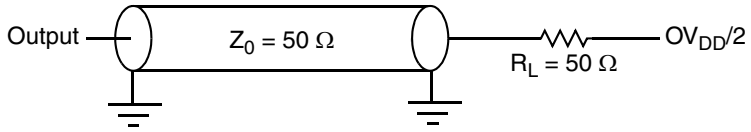
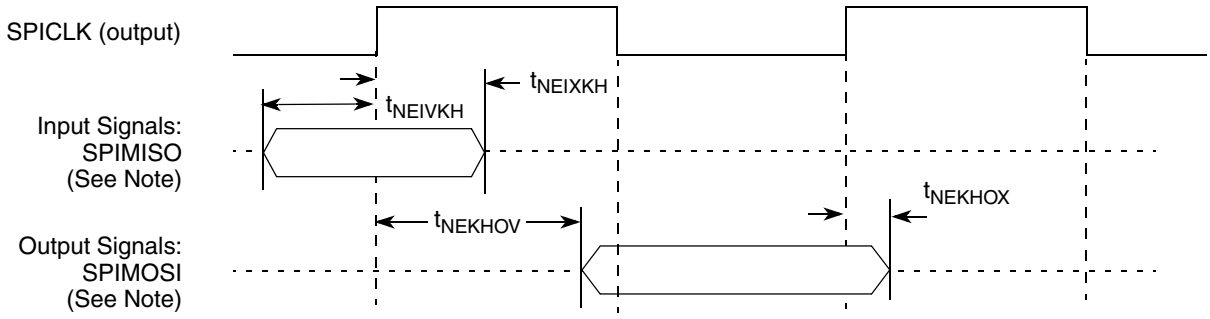



**Figure 64. SPI AC Test Load**

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

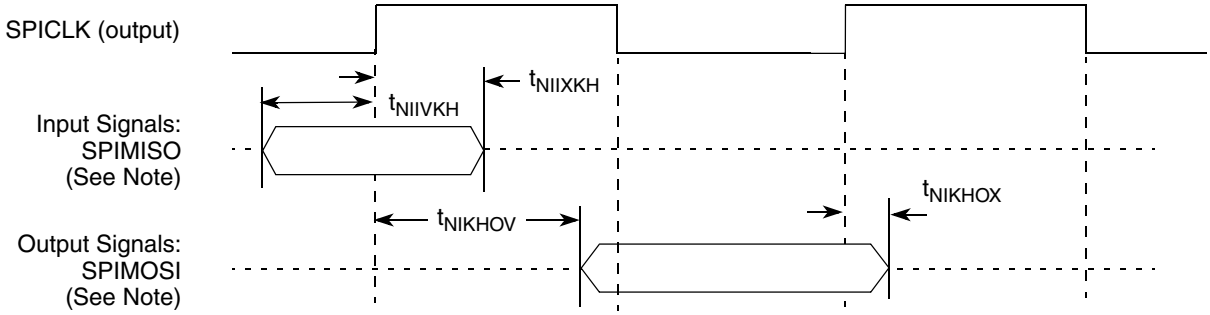
The following figure shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram**

The following figure shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram**

## 2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

### 2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

**Table 76. TDM/SI DC Electrical Characteristics**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OH}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | $OV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | 0.8 | V | — |
| Input current (0 V ≤ $V_{IN}$ ≤ $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 1 |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ referenced in Table 2 and Table 3.

### 2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

**NOTE: Rise/Fall Time on QE Input Pins**

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

# 2.21 USB Interface

This section provides the AC and DC electrical specifications for the USB interface of the MPC8569E.

## 2.21.1 USB DC Electrical Characteristics

The following table provides the USB DC electrical characteristics.

**Table 78. USB DC Electrical Characteristics**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.8 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.3 | V | — |
| Differential input sensitivity | $V_{DI}$ | 0.2 | — | V | 3 |
| Differential common mode range | $V_{CM}$ | 0.8 | 2.5 | V | 3 |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.
3. Applies to low/full speed

## 2.21.2 USB AC Electrical Specifications

The following table describes the general USB timing specifications.

**Table 79. USB General Timing Parameters**

For recommended operating conditions, see Table 3

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 20.83 | — | ns | Full speed 48 MHz |
| USB clock cycle time | $t_{USCK}$ | 166.67 | — | ns | Low speed 6 MHz |
| Skew between TXP and TXN | $t_{USTSPN}$ | — | 5 | ns | 2 |
| Skew among RXP, RXN, and RXD | $t_{USRSPND}$ | — | 10 | ns | Full-speed transitions, 2 |
| Skew among RXP, RXN, and RXD | $t_{USRPND}$ | — | 100 | ns | Low-speed transitions, 2 |

**Notes:**

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, $t_{USTSPN}$ symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

The following figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

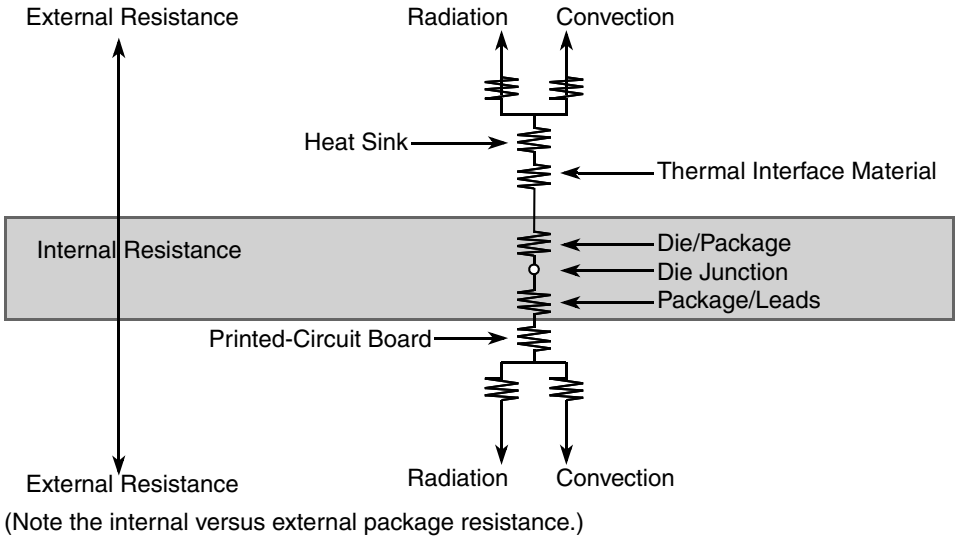



**Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and the heat sink attach material (or thermal interface material), and to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

### 3.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 73).

The system board designer can choose among several types of commercially-available thermal interface materials.

### 3.3.3 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the MPC8569E on-board temperature diode:

Operating range: 10 – 230 μA

Ideality factor over 13.5 – 220 μA; n = 1.006 +/- 0.008

# 4 Package Description

The following section describes the detailed content and mechanical description of the package.

## 5.2 Part Marking

Parts are marked as the example shown in the following figure.


FC-PBGA

**Notes:**
MPC8569xxxxxx is the orderable part number.
MMMMM is the mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
ATWLYYWW is the traceability code.

**Figure 76. Part Marking for FC-PBGA Device**

# 6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8569E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8569ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)
- *QUICC Engine Block Reference Manual with Protocol Interworking* (document number: QEIWRM)

# 7 Document Revision History

The following table provides a revision history for this document.

**Table 85. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 2 | 10/2013 | • Added footnote 5 and added new VJ package description in Table 84, “Device Nomenclature. |
| 1 | 02/2012 | • In Table 1, “MPC8569E Pinout Listing,” updated pin U20 from Reserved to THERM1 (internal thermal diode anode) and pin U21 from Reserved to THERM0 (internal thermal diode cathode). Removed note 9 and added note 32 to pins U20 and U21.<br>• In Table 38, “SGMII Transmit AC Timing Specifications,” updated min and typical values for the AC coupling capacitor parameter.<br>• In Table 48, “SD_REF_CLK and SD_REF_CLK Input Clock Requirements,” removed the condition that the reference clock duty cycle should be measured at 1.6 V.<br>• Added Section 2.6.5.1, “QUICC Engine Block IEEE 1588 DC Specifications.”<br>• Added Section 3.3.3, “Temperature Diode.” |
| 0 | 06/2011 | Initial public release |