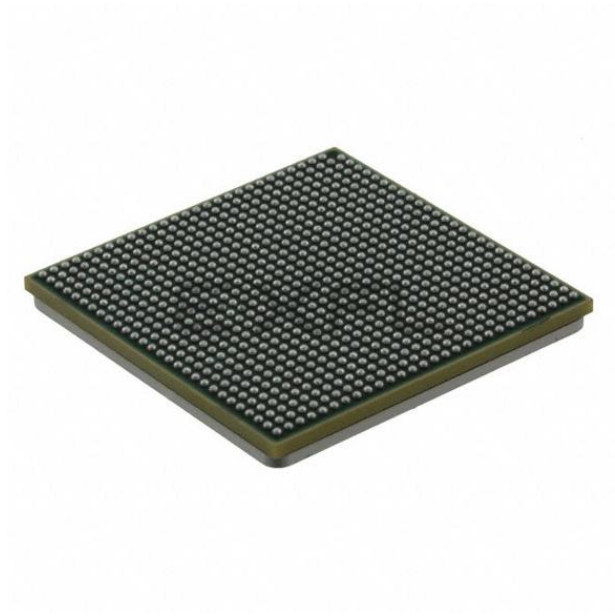


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569ecvtaqljb

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

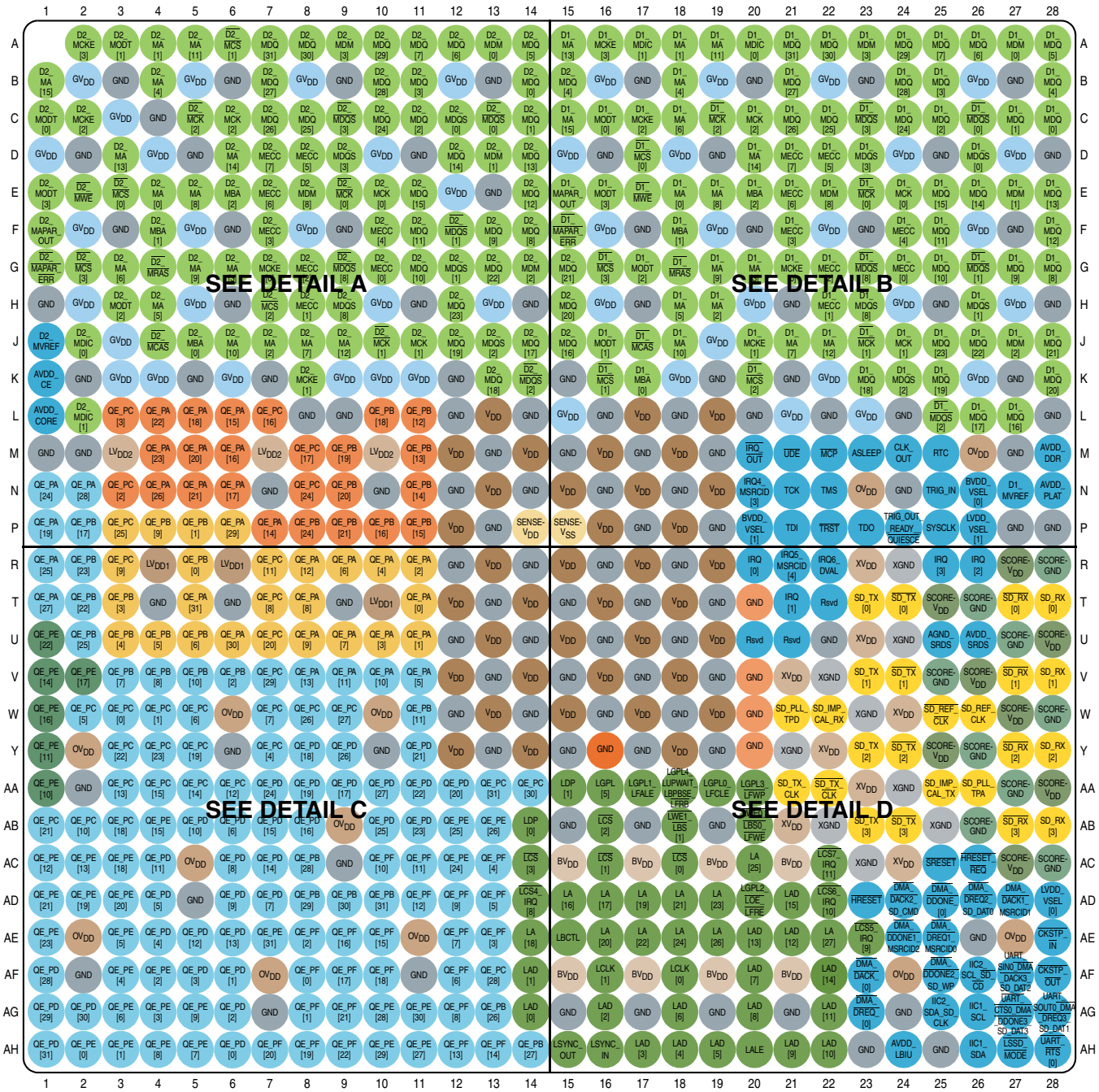


Figure 2. MPC8569E Top View Ballmap

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	B22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	C3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D1	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	E12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H10	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	H13	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H20	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K11	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K6	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K9	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L21	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L23	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	Y13	—	—	—
GND	Y15	—	—	—
GND	Y16	—	—	—
GND	Y17	—	—	—
GND	Y19	—	—	—
GND	V20	—	—	—
GND	T20	—	—	—
GND	W20	—	—	—
GND	Y20	—	—	—
SENSEVSS	P15	Ground sense	—	13
SCOREGND	AA27	SerDes Core Logic GND	—	—
SCOREGND	AB26	SerDes Core Logic GND	—	—
SCOREGND	AC28	SerDes Core Logic GND	—	—
SCOREGND	R28	SerDes Core Logic GND	—	—
SCOREGND	T26	SerDes Core Logic GND	—	—
SCOREGND	U27	SerDes Core Logic GND	—	—
SCOREGND	V25	SerDes Core Logic GND	—	—
SCOREGND	W28	SerDes Core Logic GND	—	—
SCOREGND	Y26	SerDes Core Logic GND	—	—
XGND	AA24	SerDes Transceiver Pad GND	—	—
XGND	AB22	SerDes Transceiver Pad GND	—	—
XGND	AB25	SerDes Transceiver Pad GND	—	—
XGND	AC23	SerDes Transceiver Pad GND	—	—
XGND	R24	SerDes Transceiver Pad GND	—	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Range	Unit	Notes
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	–0.3 to 3.63 –0.3 to 2.75	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Ethernet signals	LV_{IN}	–0.3 to ($LV_{DD}n$ + 0.3)	V	3
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

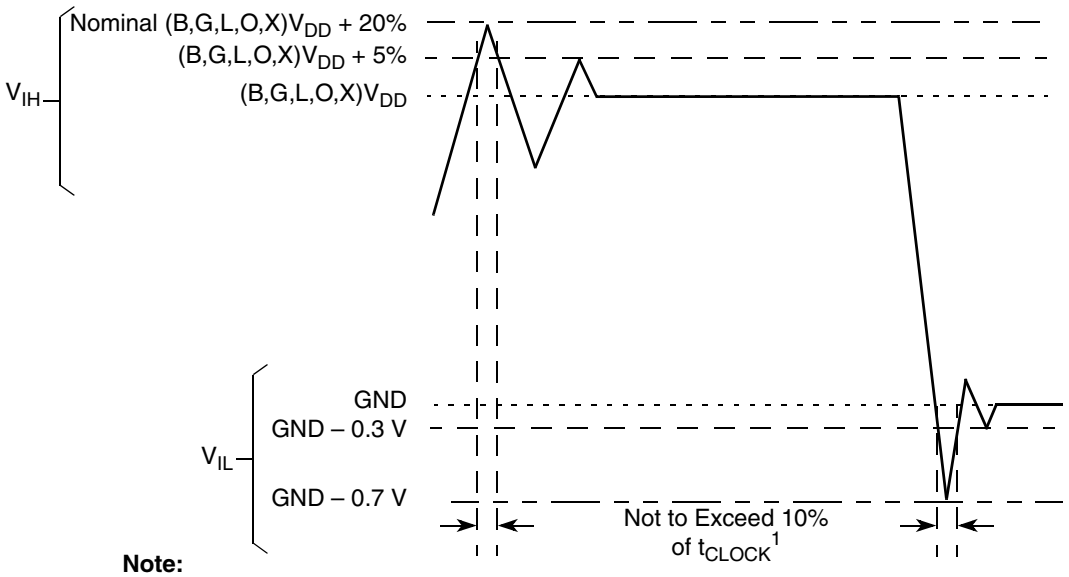
Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
PLL supply voltage	AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	1.0 V ± 30 mV 1.1 V ± 33 mV	V	2

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.1.2 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal	18 (full strength mode) 35 (half strength mode)	GV_{DD} = 1.8 V	1
DDR3 signal	20 (full strength mode) 40 (half strength mode)	GV_{DD} = 1.5 V	1
DUART, EPIC, I^2C, JTAG, system control	45	OV_{DD} = 3.3 V	—

Note:

1. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_J = 105°C and at GV_{DD} (min). Refer to the MPC8569 reference manual for the DDR impedance programming procedure through the DDR control driver register 1 (DDRCDR_1).

2.1.2 Power Sequencing

The MPC8569E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $LV_{DD}n$, OV_{DD}, ScoreVDD, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

While V_{DD} is ramping, current may be supplied from V_{DD} through the MPC8569E to GV_{DD}. Nevertheless, GV_{DD} from an external supply should follow the sequencing described above.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

2.1.3 RESET Initialization

This section describes the AC electrical specifications for the RESET timing requirements of the MPC8569E. The following table describes the specifications for the RESET initialization timing.

Table 5. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	10	—	SYSCLK	1, 2
Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion	25	—	ns	3

Table 5. RESET Initialization Timing Specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum rise/fall time of $\overline{\text{HRESET}}$	—	1	SYSCLK	5
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLK	4
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	2	—	SYSCLK	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLK	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	8	—	SYSCLK	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLK	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in *AN4232 MPC8569E PowerQUICC III Design Checklist*.
4. SYSCLK is the primary clock input for the MPC8569E.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following table provides the PLL lock times.

Table 6. PLL Lock Times

Parameter	Min	Max	Unit
Core PLL lock time	—	100	µs
Platform PLL lock time	—	100	µs
QUICC Engine block PLL lock time	—	100	µs
DDR PLL lock times	—	100	µs

2.6.3.4 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.6.3.4.1 RMII Transmit AC Timing Specifications

The following table shows the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMT}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMTH}	35	—	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	4.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	4.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

The following figure shows the RMII transmit AC timing diagram.

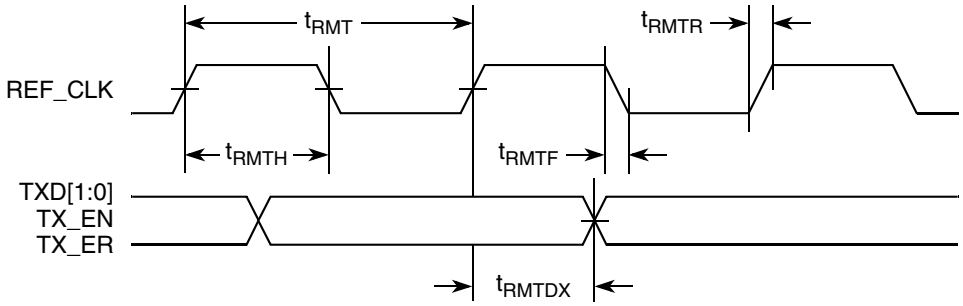


Figure 19. RMII Transmit AC Timing Diagram

2.6.3.4.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMR}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMRH}	35	—	65	%	1
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	1
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

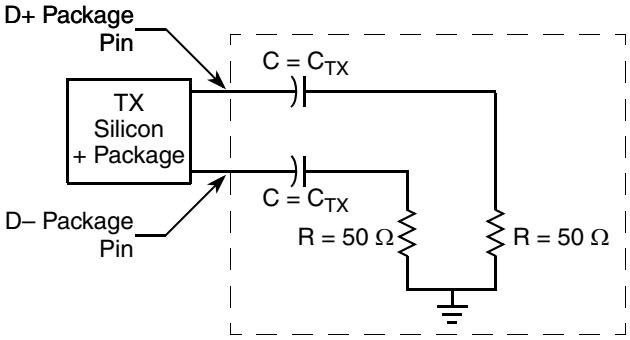
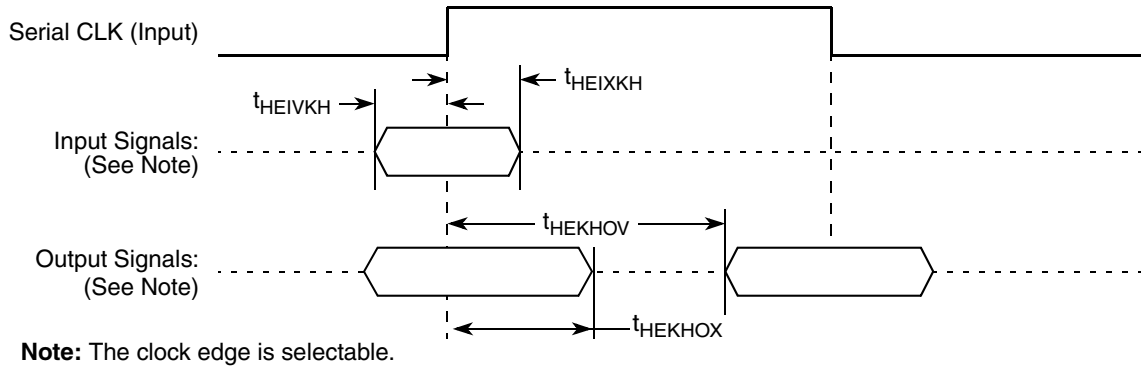


Figure 29. SGMII AC Test/Measurement Load

Figure 36 and Figure 37 represent the AC timing from Table 45 and Table 46. Note that although the specifications generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also note that the clock edge is selectable.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 36. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.

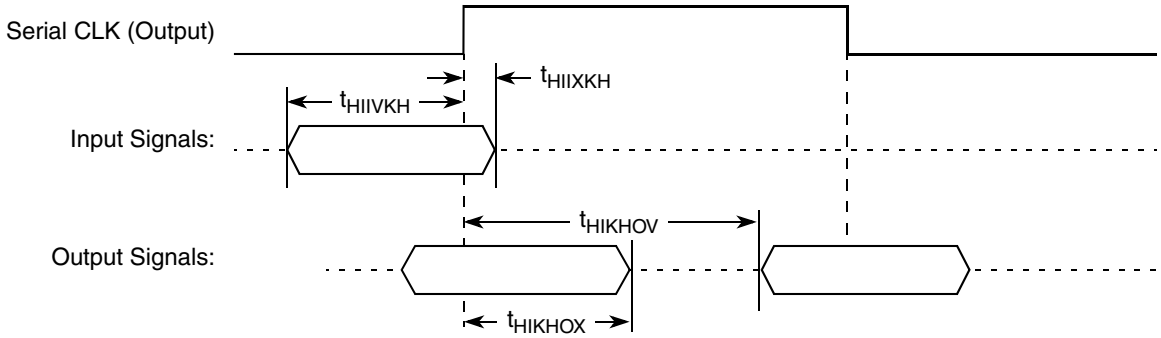


Figure 37. AC Timing (Internal Clock) Diagram

2.9 High-Speed SerDes Interfaces (HSSI)

The MPC859E features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications.The SerDes interface can be used for PCI Express and/or Serial RapidIO and/or SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The below figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
AC-coupling capacitor	C_{TX}	75	—	200	nF	All transmitters are AC-coupled. The AC-coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The MPC8569E SerDes transmitter does not have CTX built-in. An external AC-coupling capacitor is required.

2.10.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

2.10.4 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

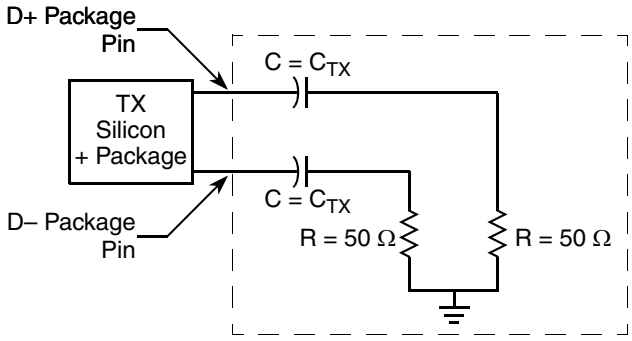


Figure 46. Compliance Test/Measurement Load

2.11 Serial RapidIO (SRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the MPC8569E, for the LP-serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC-coupling at the receiver input must be used.Signal Definitions

2.11.1 Signal Definitions

This section defines terms used in the description and specification of differential signals used by the LP-Serial links. Figure 47 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

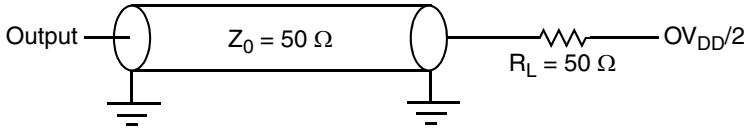


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

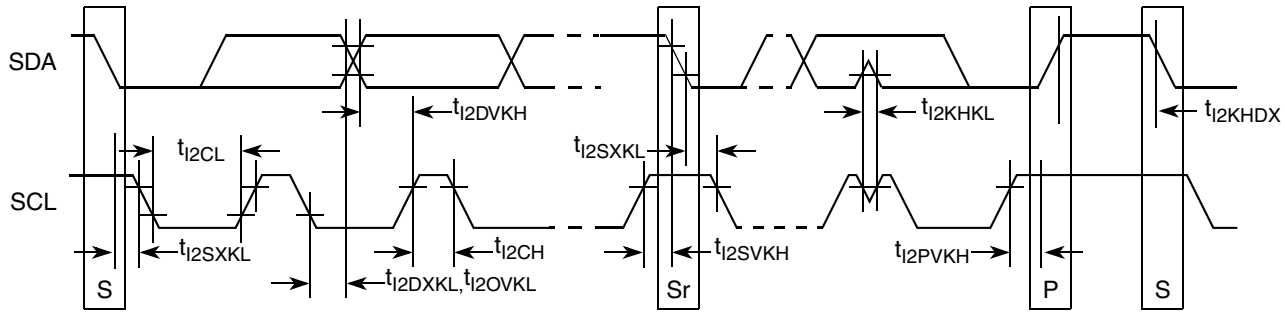


Figure 50. I²C Bus AC Timing Diagram

2.14 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 61. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

Table 62. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	4
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

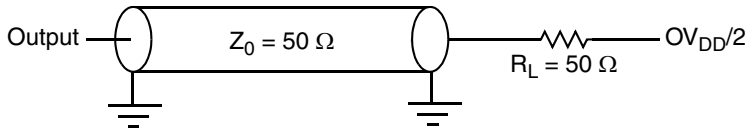


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 81. UTOPIA/POS AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA/POS inputs—External clock input setup time	t_{UEIVKH}	4.0	—	ns
UTOPIA/POS inputs—Internal clock input hold time	t_{UIIXKH}	0	—	ns
UTOPIA/POS inputs—External clock input hold time	t_{UEIXKH}	1.2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA/POS outputs internal timing (UI) for the time t_{Utopia} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the UTOPIA/POS.

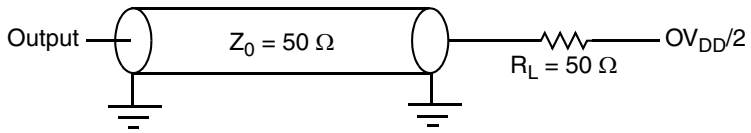


Figure 70. UTOPIA/POS AC Test Load

Figure 71 and Figure 72 represent the AC timing from Table 81. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the UTOPIA/POS timing with external clock.

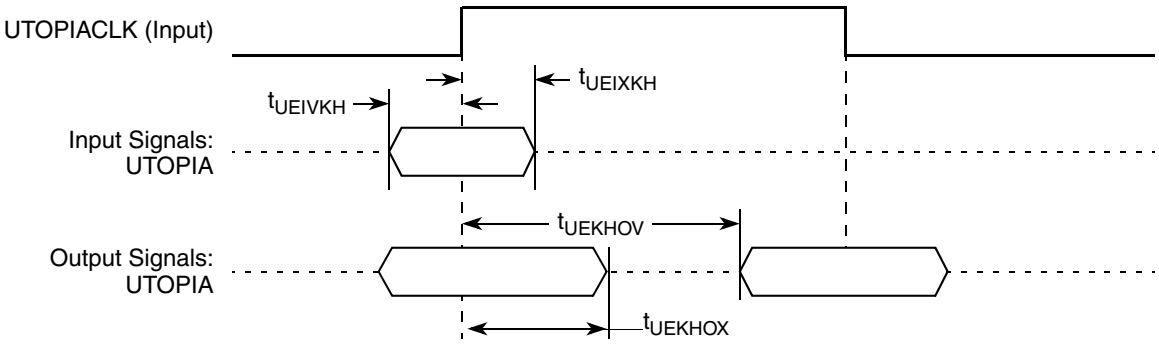


Figure 71. UTOPIA/POS AC Timing (External Clock) Diagram