Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569evjankgb

Table of Contents

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PC25	P3	I/O	$LV_{DD}1$	—
QE_PC26	W8	I/O	OV_{DD}	—
QE_PC27	W9	I/O	OV_{DD}	—
QE_PC28	AF13	I/O	OV_{DD}	—
QE_PC29	V7	I/O	OV_{DD}	—
QE_PC30	AA14	I/O	OV_{DD}	—
QE_PC31	AA13	I/O	OV_{DD}	—
QE_PD0	AH6	I/O	OV_{DD}	11
QE_PD1	AF6	I/O	OV_{DD}	—
QE_PD2	AG6	I/O	OV_{DD}	—
QE_PD3	AF5	I/O	OV_{DD}	—
QE_PD4	AE4	I/O	OV_{DD}	22
QE_PD5	AD4	I/O	OV_{DD}	—
QE_PD6	AB6	I/O	OV_{DD}	—
QE_PD7	AD7	I/O	OV_{DD}	—
QE_PD8	AC6	I/O	OV_{DD}	—
QE_PD9	AD6	I/O	OV_{DD}	—
QE_PD10	AB5	I/O	OV_{DD}	—
QE_PD11	AC4	I/O	OV_{DD}	—
QE_PD12	AE5	I/O	OV_{DD}	—
QE_PD13	AE6	I/O	OV_{DD}	—
QE_PD14	AC7	I/O	OV_{DD}	—
QE_PD15	AB7	I/O	OV_{DD}	—
QE_PD16	AB8	I/O	OV_{DD}	—
QE_PD17	AA9	I/O	OV_{DD}	—
QE_PD18	Y8	I/O	OV_{DD}	—
QE_PD19	AA8	I/O	OV_{DD}	—
QE_PD20	AA12	I/O	OV_{DD}	—
QE_PD21	Y11	I/O	OV_{DD}	—
QE_PD22	AA11	I/O	OV_{DD}	—
QE_PD23	AB11	I/O	OV_{DD}	—
QE_PD24	AA7	I/O	OV_{DD}	—
QE_PD25	AB10	I/O	OV_{DD}	—
QE_PD26	Y9	I/O	OV_{DD}	—
QE_PD27	AA10	I/O	OV_{DD}	—

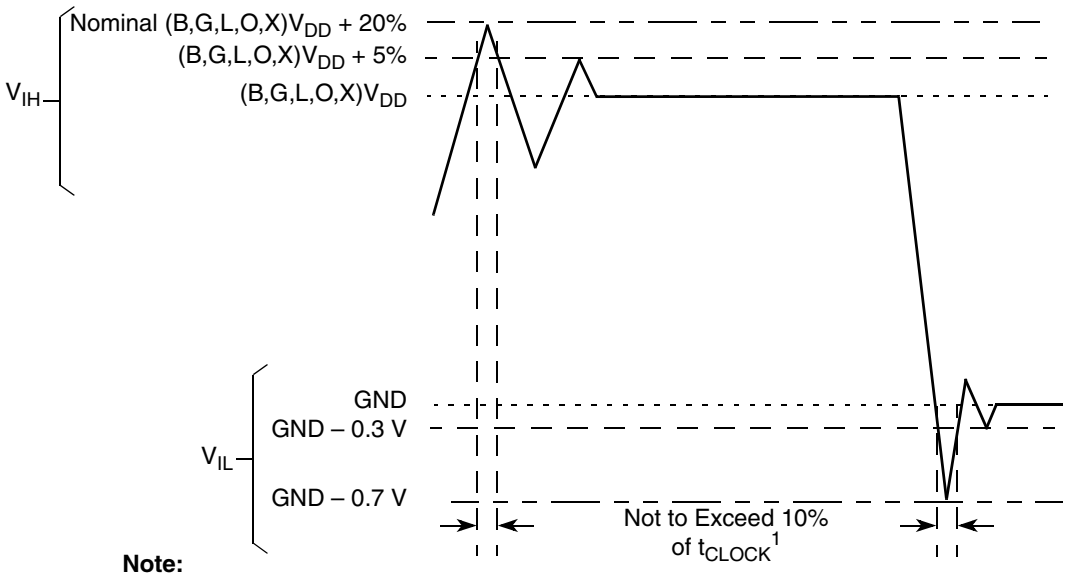
Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD	P14	Core supply sense	V_{DD}	13
XV_{DD}	AA23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AB21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AC24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	R23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	U23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	V21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	W24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	Y22	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
AV_{DD}_CORE	L1	1.0-V/1.1-V AV_{DD} supply for the core PLL	—	12
AV_{DD}_DDR	M28	1.0-V/1.1-V AV_{DD} supply for the DDR PLL	—	12
AV_{DD}_LBIU	AH24	1.0-V/1.1-V AV_{DD} supply for the eLBC PLL	—	12
AV_{DD}_PLAT	N28	1.0-V/1.1-V AV_{DD} supply for the platform PLL	—	12
AV_{DD}_QE	K1	1.0-V/1.1-V AV_{DD} supply for the QUICC Engine block PLL	—	12
AV_{DD}_SRDS	U26	1.0-V/1.1-V AV_{DD} supply for the SerDes PLL	—	12
GND	AA2	—	—	—
GND	AB15	—	—	—
GND	AB17	—	—	—
GND	AB19	—	—	—
GND	AC9	—	—	—
GND	AD5	—	—	—
GND	AE26	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	AF11	—	—	—
GND	AF2	—	—	—
GND	AG15	—	—	—
GND	AG17	—	—	—
GND	AG19	—	—	—
GND	AG21	—	—	—
GND	AG24	—	—	—
GND	AG7	—	—	—
GND	AH23	—	—	—
GND	AH25	—	—	—
GND	B13	—	—	—
GND	B17	—	—	—
GND	B20	—	—	—
GND	B23	—	—	—
GND	B27	—	—	—
GND	B3	—	—	—
GND	B6	—	—	—
GND	B9	—	—	—
GND	C4	—	—	—
GND	D11	—	—	—
GND	D16	—	—	—
GND	D19	—	—	—
GND	D2	—	—	—
GND	D25	—	—	—
GND	D28	—	—	—
GND	D5	—	—	—
GND	E13	—	—	—
GND	F17	—	—	—
GND	F20	—	—	—
GND	F23	—	—	—
GND	F27	—	—	—
GND	F3	—	—	—
GND	F6	—	—	—
GND	F9	—	—	—
GND	H1	—	—	—

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

Table 8. MPC8569E Power Dissipation (continued)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	1333	533	800	667	1.1	65	5.7 W	1, 2
Thermal						105	7.9 W	1, 3
Maximum							8.6 W	1, 4

Note:

1. These values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running the Dhrystone benchmark, using the *nominal* process and *recommended* core voltage (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the maximum power measured while running the Dhrystone benchmark, using the *worst case* process and *recommended* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions that keeps the execution unit maximally busy and a typical workload on platform interfaces, using the *worst case* process and *nominal* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
5. This table includes power numbers for the V_{DD}, AV_{DD}_n, and ScoreVDD rails.

2.3 Input Clocks

The following table provides the system clock (SYSCLK) DC specifications.

Table 9. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	10.5	11.5	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

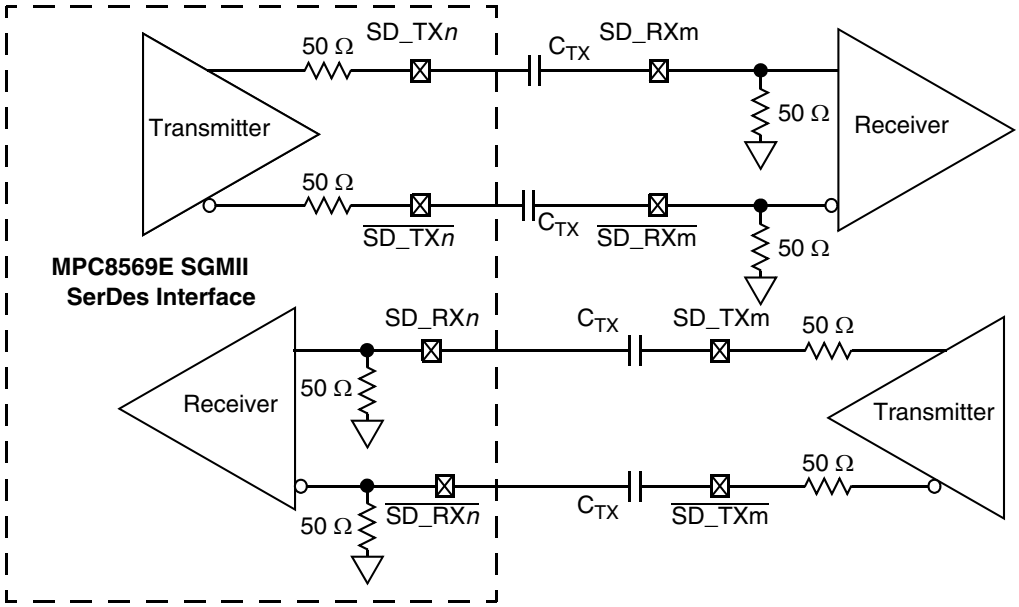


Figure 27. 4-Wire AC-Coupled SGMII Serial Link Connection Example

The following figure shows the SGMII transmitter DC measurement circuit.

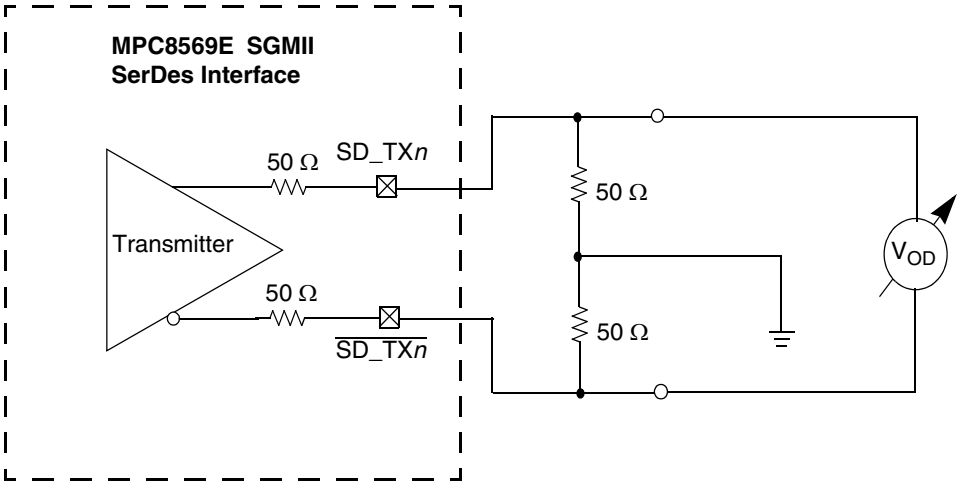


Figure 28. SGMII Transmitter DC Measurement Circuit

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

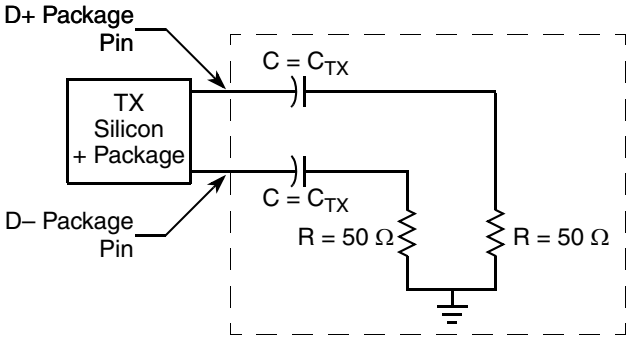


Figure 29. SGMII AC Test/Measurement Load

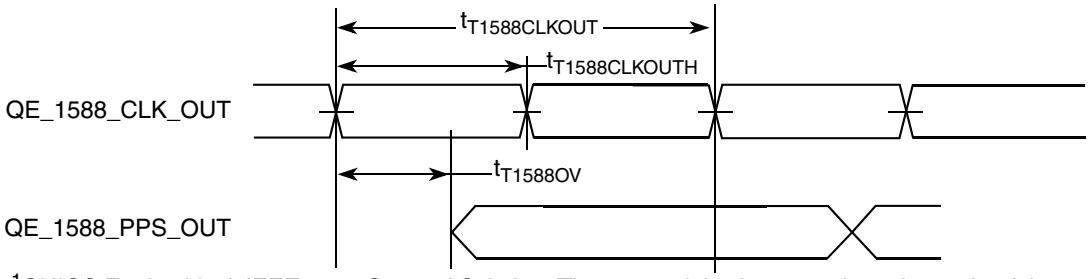
Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2
QE_PTP_SOF_TX_IN pulse width	$t_{T1588TRIGH}$	$T_{TX\_CLK} \times 2$	—	—	ns	4
QE_PTP_SOF_RX_IN pulse width	$t_{T1588TRIGH}$	$T_{RX\_CLK} \times 2$	—	—	ns	4

Notes:

1. T_{RX_CLK} is the max clock period of the QUICC Engine block's receiving clock selected by TMR_CTRL[CKSEL]. See the *QUICC Engine Block with Protocol Interworking Reference Manual,* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QUICC Engine Block with Protocol Interworking Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of t_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ are 2800, 280, and 56 ns, respectively.
4. The minimum value of $t_{TX/RXCLK}$ is defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the value of $t_{TX/RXCLK}$ are 800, 80, and 16 ns, respectively.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the data and command output AC timing diagram.



[1]QUICC Engine block IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T11588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 31. QUICC Engine Block IEEE 1588 Output AC Timing

The following figure shows the data and command input AC timing diagram.

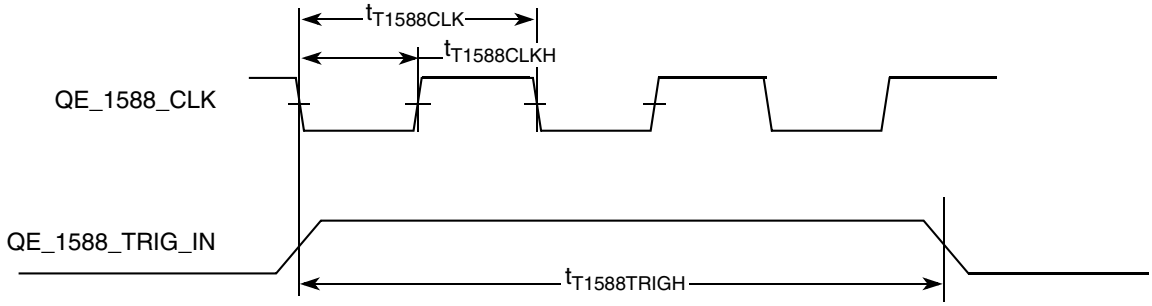


Figure 32. QUICC Engine Block IEEE 1588 Input AC Timing

2.7.1.1 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 43. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} = 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$2\times(t_{plb\_clk}*8)$	—	—	ns	4
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	3, 4, 5
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDCF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the Mgmt Clock CE_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the QUICC Engine block clock/2.
5. MDC to MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time (t_{MDKHDX}).
(Min setup = cycle time – max delay

The following figure shows the MII management AC timing diagram.

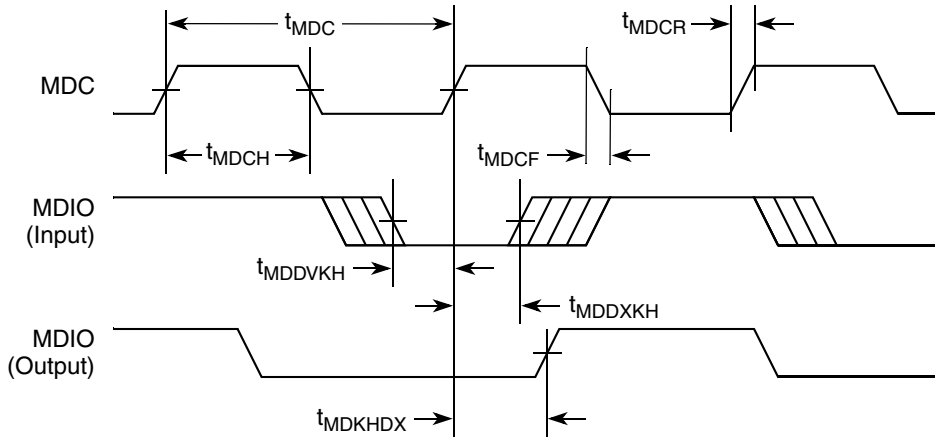


Figure 34. MII Management Interface Timing Diagram

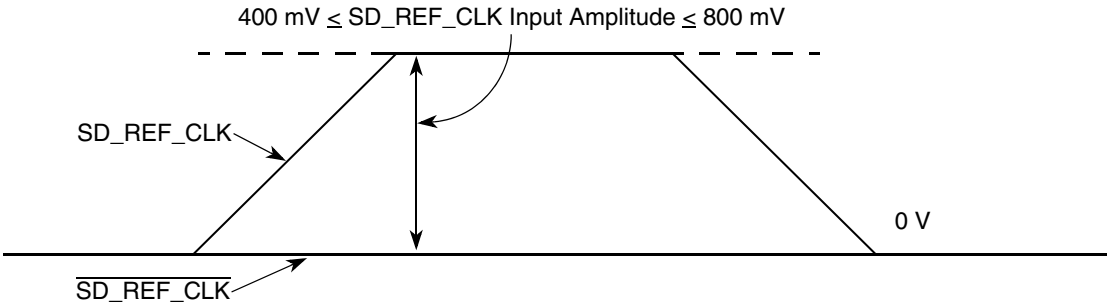


Figure 42. Single-Ended Reference Clock Input DC Requirements

2.9.2.4 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express, SGMII, and Serial RapidIO SerDes reference clocks to be guaranteed by the customer's application design.

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2, 7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3, 7

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

The following table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 52. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 57. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD} (max))	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *MPC8569E PowerQUICC III Integrated Processor Family Reference Manual* for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.12.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface.

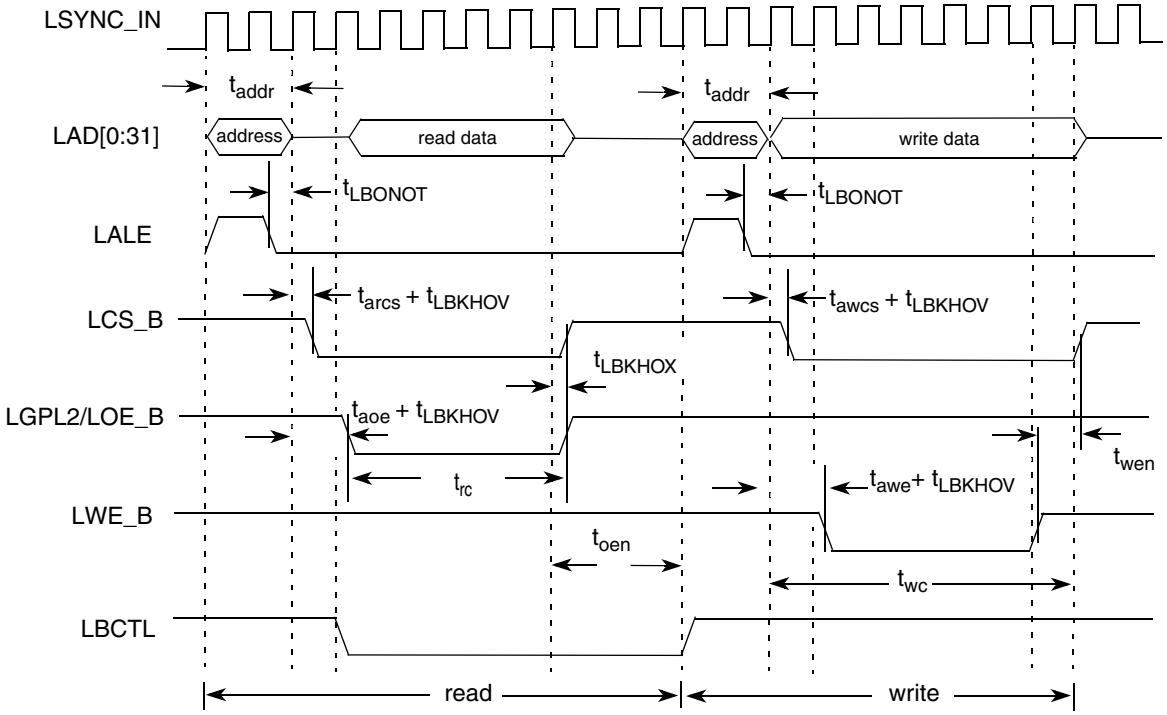
Table 58. I²C AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to reference manual.

Figure 58. GPCM Output Timing Diagram (PLL Enabled)

2.15.2.3 Enhanced Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LUPWAIT/LFRB are relative to the rising edge of LCLKs. LUPWAIT/LFRB are relative to the falling edge of LCLKs.

The following figure shows the AC timing diagram for PLL bypass mode.

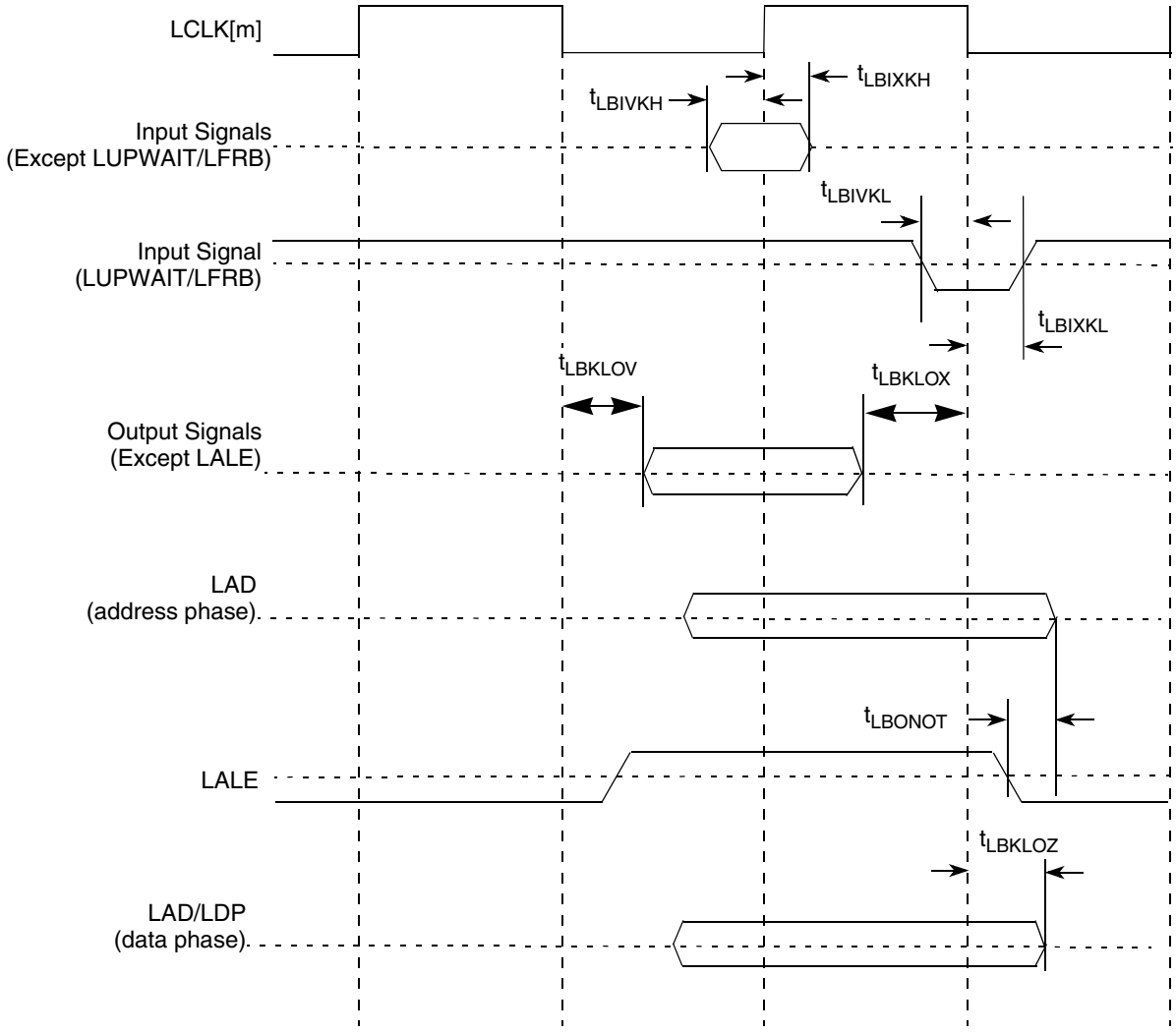


Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

2.18.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 73. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.19 SPI Interface

This section describes the SPI DC and AC electrical specifications of the MPC8569E.

2.19.1 SPI DC Electrical Characteristics

The following table provides the SPI DC electrical characteristics.

Table 74. SPI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 75. SPI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	9	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2

Table 77. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

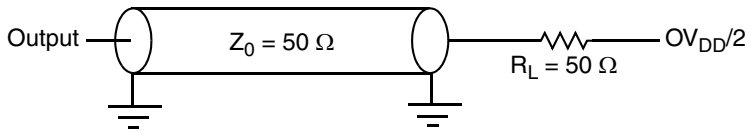
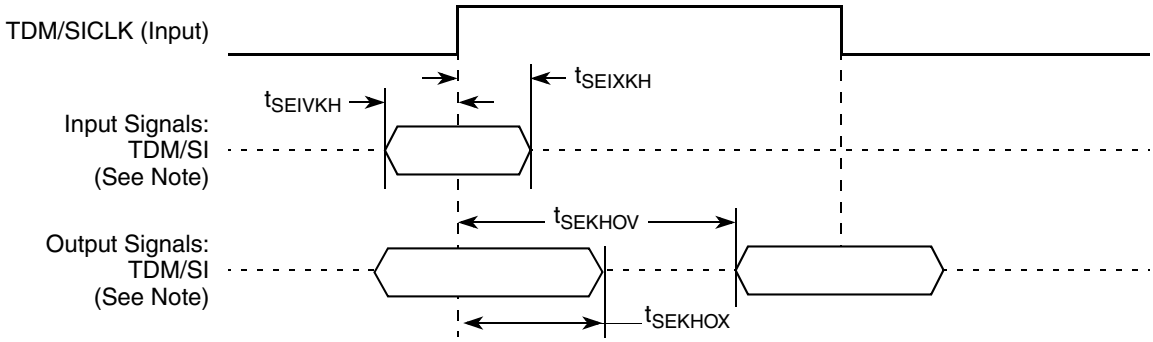


Figure 67. TDM/SI AC Test Load

The below figure represents the AC timing from Table 77. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. The following figure shows the TDM/SI timing with external clock.

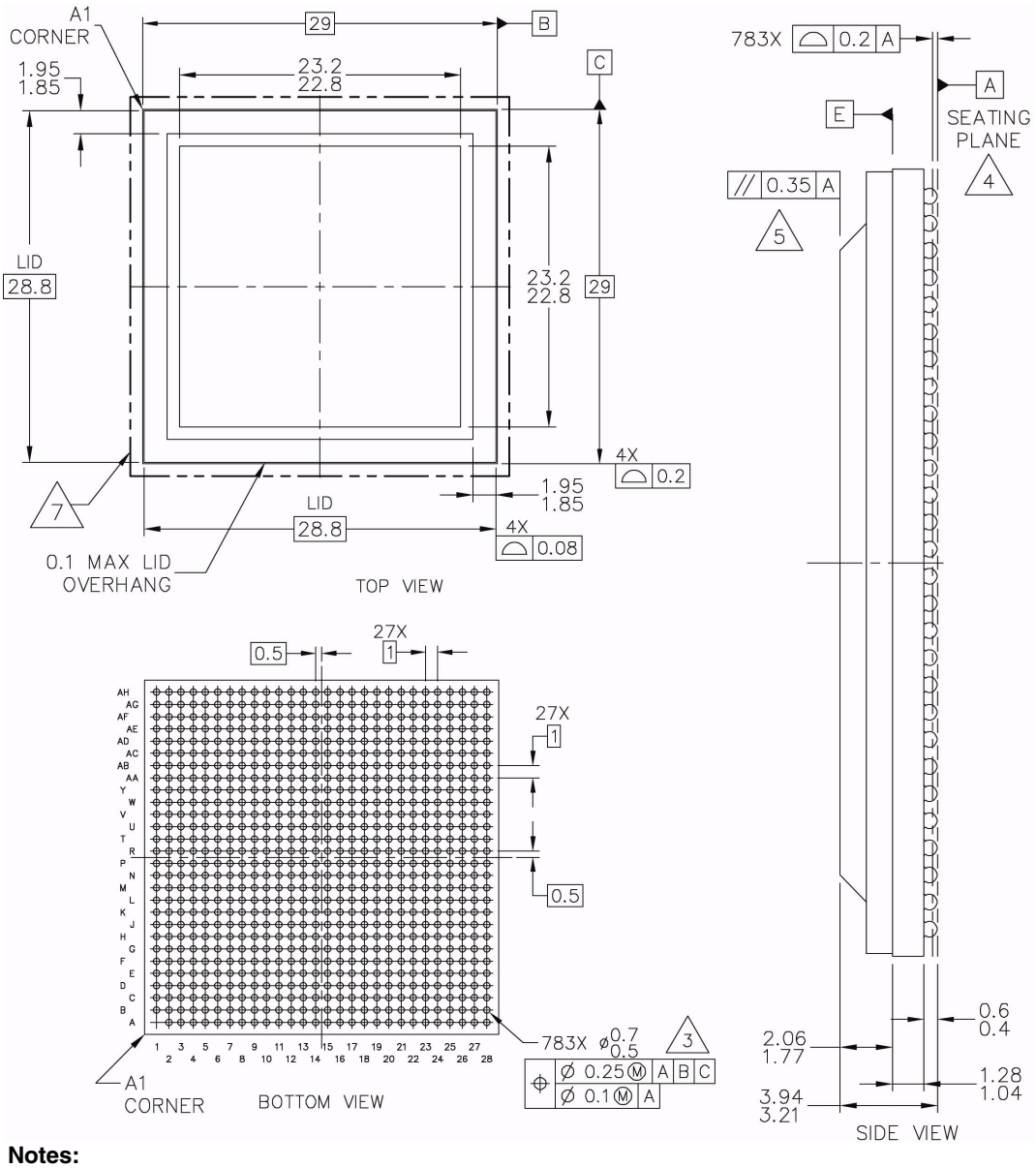


Note: The clock edge is selectable on TDM/SI.

Figure 68. TDM/SI AC Timing (External Clock) Diagram

4.2 Mechanical Dimensions of the FC-PBGA with Full Lid

The following figure shows the mechanical dimensions and bottom surface nomenclature for the MPC8569E FC-PBGA package with full lid.



Notes:

[1]All dimensions are in millimeters.
[2]Dimensions and tolerances per ASME Y14.5M-1994.
[3]Maximum solder ball diameter measured parallel to datum A.
[4]Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
[5]Parallelism measurement shall exclude any effect of mark on top surface of package.
[6]All dimensions are symmetric across the package center lines unless dimensioned otherwise.
[7]29.2 mm maximum package assembly (lid and laminate) x and y.

Figure 75. MPC8569E FC-PBGA Package with Full Lid

5 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

Ordering information for the parts fully covered by this specification document is provided in Section 5.1, "Part Numbers Fully Addressed by This Document."

5.1 Part Numbers Fully Addressed by This Document

The following table shows the device nomenclature.

Table 84. Device Nomenclature

MPC	nnnn	E	C	Vx	AA	X	G	R
Product Code[1]	**Part Identifier**	**Security Engine**	**Temperature Range**	**Package** [2]	**Processor Frequency** [3]	**DDR Frequency**[4]	**QE Frequency**	**Revision Level**
MPC PPC	8569	E = included	Blank = 0° to 105°C C = –40° to 105°C	VT = FC-PBGA, Pb free, C5 spheres VJ = FC-PBGA, Pb free C4 bumps and pb free C5 spheres	AN = 800 MHz AQ = 1067 MHz AU = 1333 MHz	K = 600 MHz L = 667 MHz N = 800 MHz	G = 400 MHz J = 533 MHz L = 667 MHz	Blank = Rev. 1.0 (SVR = 0x8088_0010 A = Rev. 2.0 (SVR = 0x8088_0020 B = Rev. 2.1 (SVR = 0x8088_0021
		Blank = not included						A = Rev. 2.0 (SVR = 0x8080_0020 B = Rev. 2.1 (SVR = 0x8080_0021

Notes:

1. MPC stands for "qualified." PPC stands for pre-production samples.
2. See Section 4, "Package Description," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
4. See Table 85 for the corresponding maximum platform frequency.
5. C5 spheres are used by customer to attach to pcb. C4 bumps are bumps used on die of the device to connect between die and package substrate.