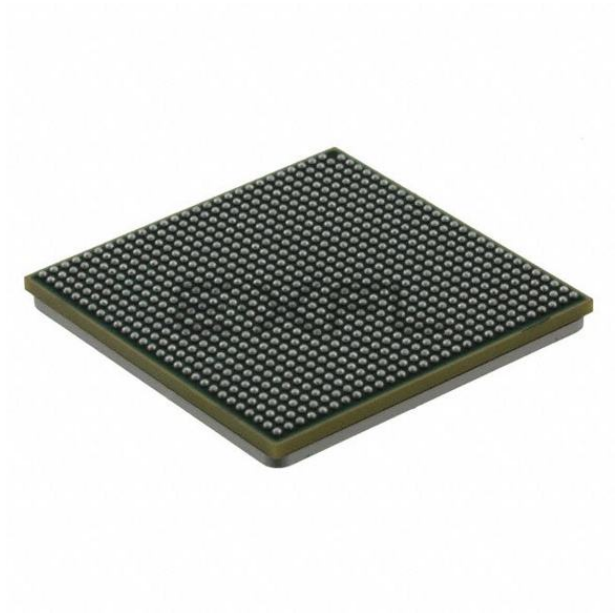

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569evjaqljb

NOTE

The MPC8569E is also available without a security engine in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

The following figure shows the major functional units within the MPC8569E.

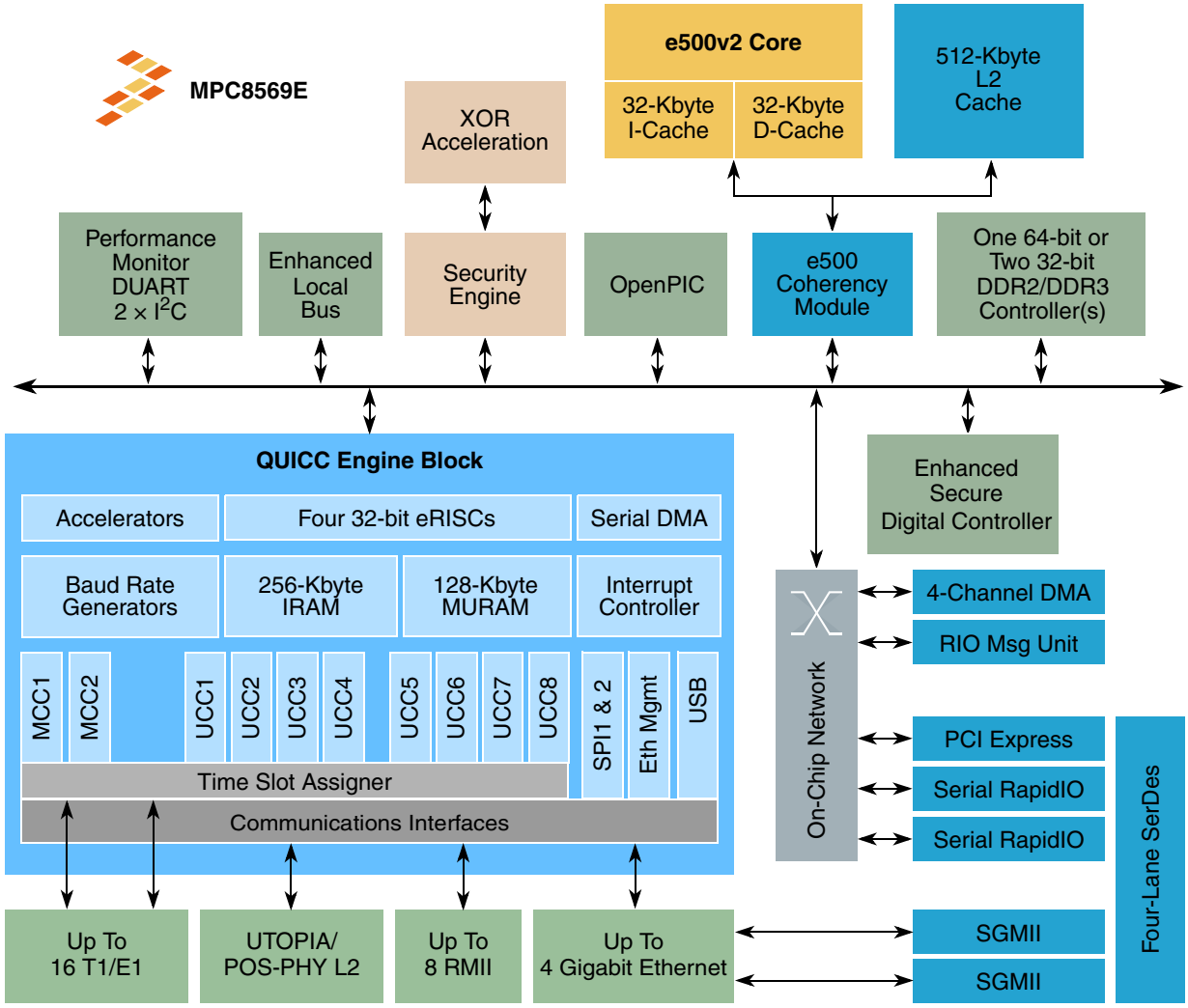


Figure 1. MPC8569E Block Diagram

The following figure provides detailed view C of the MPC8569E 783-pin BGA ball map diagram.

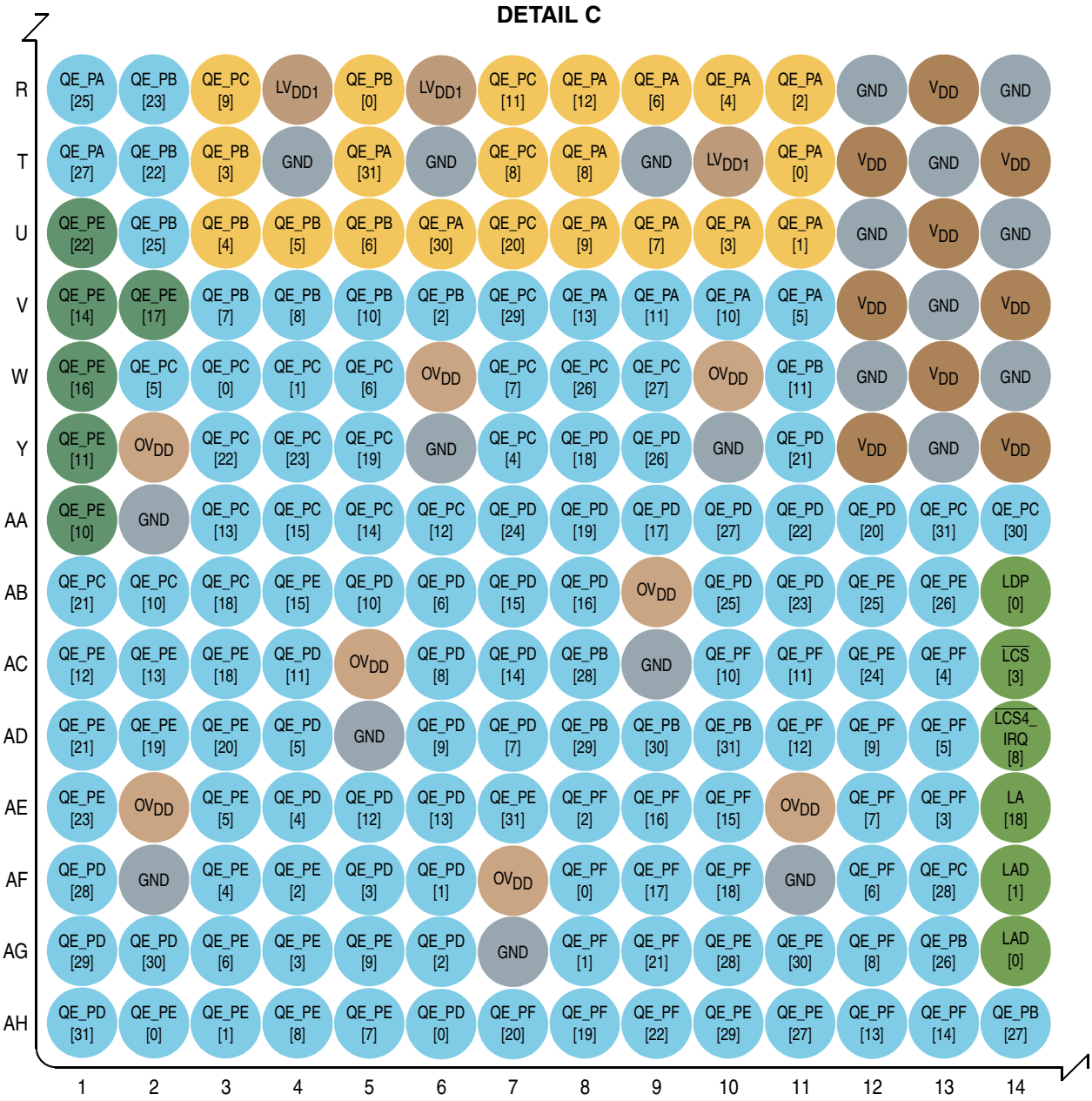


Figure 5. MPC8569E Detail C Ball Map

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	P18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W19	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD	P14	Core supply sense	V_{DD}	13
XV_{DD}	AA23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AB21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AC24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	R23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	U23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	V21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	W24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	Y22	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
AV_{DD}_CORE	L1	1.0-V/1.1-V AV_{DD} supply for the core PLL	—	12
AV_{DD}_DDR	M28	1.0-V/1.1-V AV_{DD} supply for the DDR PLL	—	12
AV_{DD}_LBIU	AH24	1.0-V/1.1-V AV_{DD} supply for the eLBC PLL	—	12
AV_{DD}_PLAT	N28	1.0-V/1.1-V AV_{DD} supply for the platform PLL	—	12
AV_{DD}_QE	K1	1.0-V/1.1-V AV_{DD} supply for the QUICC Engine block PLL	—	12
AV_{DD}_SRDS	U26	1.0-V/1.1-V AV_{DD} supply for the SerDes PLL	—	12
GND	AA2	—	—	—
GND	AB15	—	—	—
GND	AB17	—	—	—
GND	AB19	—	—	—
GND	AC9	—	—	—
GND	AD5	—	—	—
GND	AE26	—	—	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

Table 33. TBI Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns	—
PMA_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns	2
PMA_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

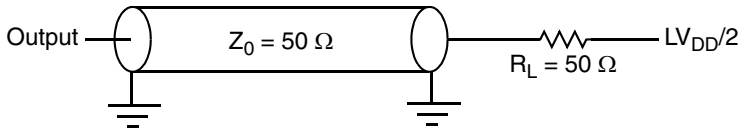


Figure 23. AC Test Load

The following figure shows the TBI receive AC timing diagram.

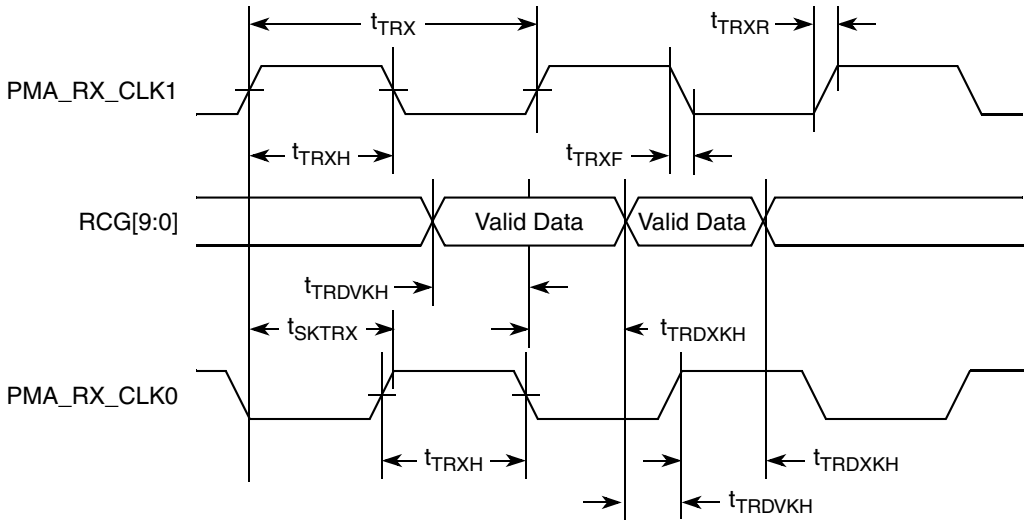


Figure 24. TBI Receive AC Timing Diagram

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.6.4.1.2 SGMII Transmit DC Timing Specifications

Table 36 and Table 37 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs, SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*], as shown in Figure 28.

Table 36. SGMII DC Transmitter Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	320.0	500.0	725.0	mV	Equalization setting: 1.0×
		293.8	459.0	665.6		Equalization setting: 1.09×
		266.9	417.0	604.7		Equalization setting: 1.2×
		240.6	376.0	545.2		Equalization setting: 1.33×
		213.1	333.0	482.9		Equalization setting: 1.5×
		186.9	292.0	423.4		Equalization setting: 1.71×
		160.0	250.0	362.5		Equalization setting: 2.0×

2.6.5 QUICC Engine Block IEEE 1588 Electrical Characteristics

2.6.5.1 QUICC Engine Block IEEE 1588 DC Specifications

The following table shows the QUICC Engine block IEEE 1588 DC specifications when operating from a 3.3 V supply.

Table 40. QUICC Engine Block IEEE 1588 DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = OV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbols referenced in Table 2 and Table 3.

2.6.5.2 QUICC Engine Block IEEE 1588 AC Specifications

The following table provides the QUICC Engine block IEEE 1588 AC timing specifications.

Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 7$	ns	1, 3
QE_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	5
QE_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	5
Rise time QE_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	5
Fall time QE_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	5
QE_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
QE_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
QE_1588_PPS_OUT	$t_{T1588OV}$	0.5	—	4.0	ns	—

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1.3	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 46. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

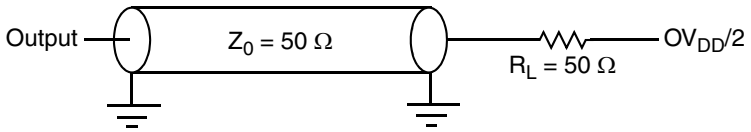


Figure 35. AC Test Load

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD*n*_REF_CLK) to falling edge rate (SD*n*_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6, 7

Notes:
1. **Caution:** Only 100 and 125 have been tested. In-between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 43.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 44.
7. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

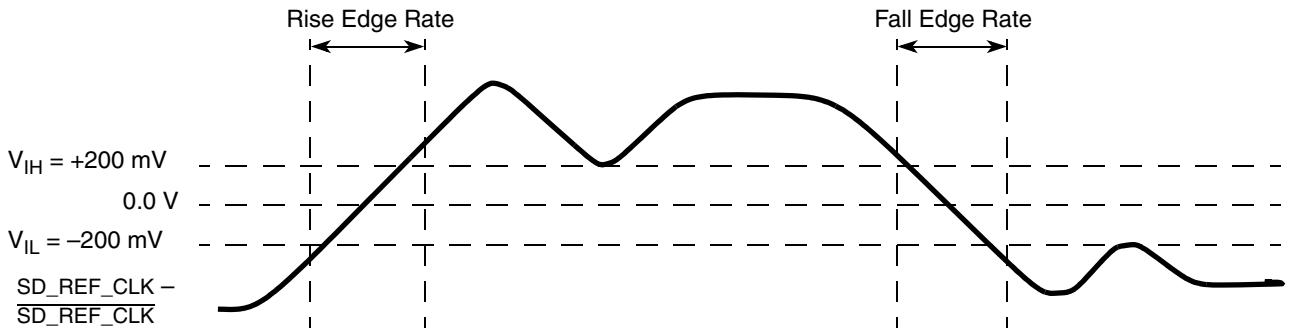


Figure 43. Differential Measurement Points for Rise and Fall Time

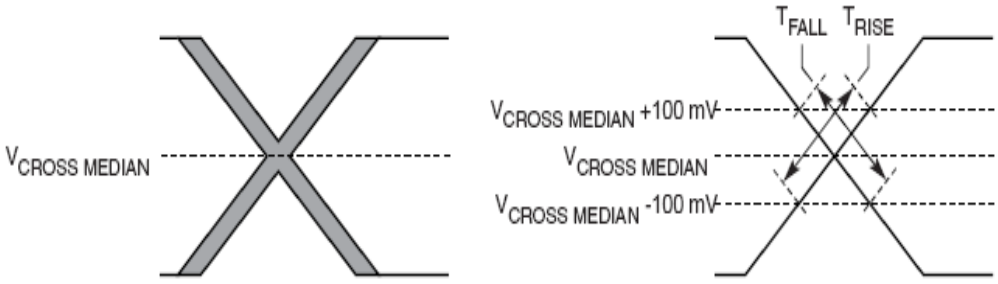


Figure 44. Single-Ended Measurement Points for Rise and Fall Time Matching

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

2.11.4.2 AC Requirements for Serial RapidIO Transmitter

The following table defines the transmitter AC specifications for the Serial RapidIO. The AC timing specifications do not include RefClk jitter

Table 55. SRIO Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

The following table defines the receiver AC specifications for Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 56. SRIO Receiver AC Timing Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1, 3
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1, 3
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1, 3
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 48. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.
3. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

2.15.2.2 Enhanced Local Bus AC Timing Specifications for PLL Enable Mode

For PLL enable mode, all timings are relative to the rising edge of LSYNC_IN.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3 V, 2.5 V and 1.8 V for PLL enable mode.

Table 66. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V 2.5 V and 1.8 V) —PLL Enabled Mode

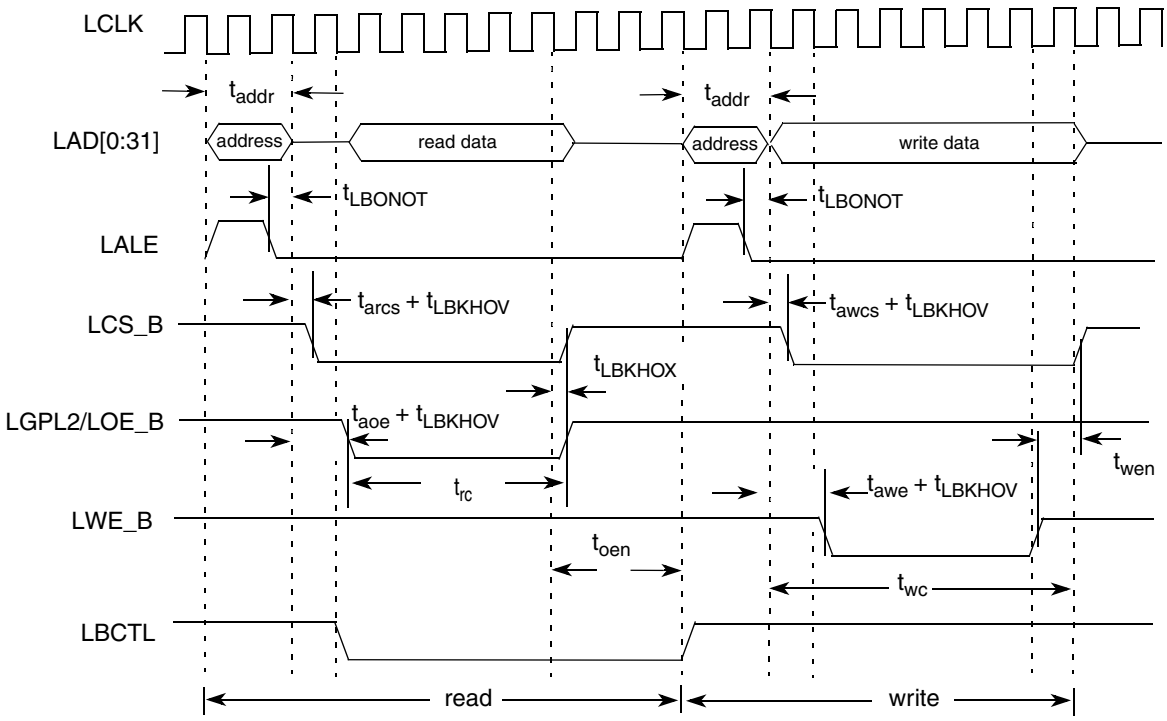
For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	7.5	12	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	5
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	680	ps	2
Input setup	t_{LBIVKH}	2	—	ns	—
Input hold	t_{LBIXKH}	1.0	—	ns	—
Output delay (Except LALE)	t_{LBKHOV}	—	3.8	ns	—
Output hold (Except LALE)	t_{LBKHOX}	0.6	—	ns	—
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 0.475 ns (LBCR[AHD]=0) ½ – 0.475 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle. The eLBC controller clock refers to the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows how the AC timing diagram applies to GPCM in PLL bypass mode. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to the MPC8569E reference manual.

Figure 60. GPCM Output Timing Diagram (PLL Bypass Mode)

2.16 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the MPC8569E.

2.16.1 eSDHC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the eSDHC interface of the MPC8569E.

Table 68. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 × OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × OV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 µA at OV_{DD} min	0.75 × OV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 µA at OV_{DD} min	—	0.125 × OV_{DD}	V	—

The following figure provides the eSDHC clock input timing diagram.

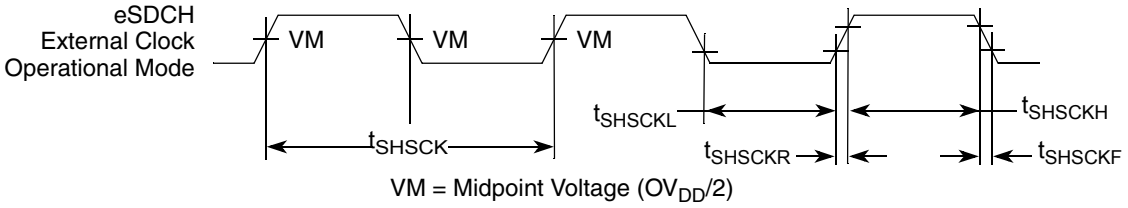


Figure 61. eSDHC Clock Input Timing Diagram

The following figure provides the data and command input/output timing diagram.

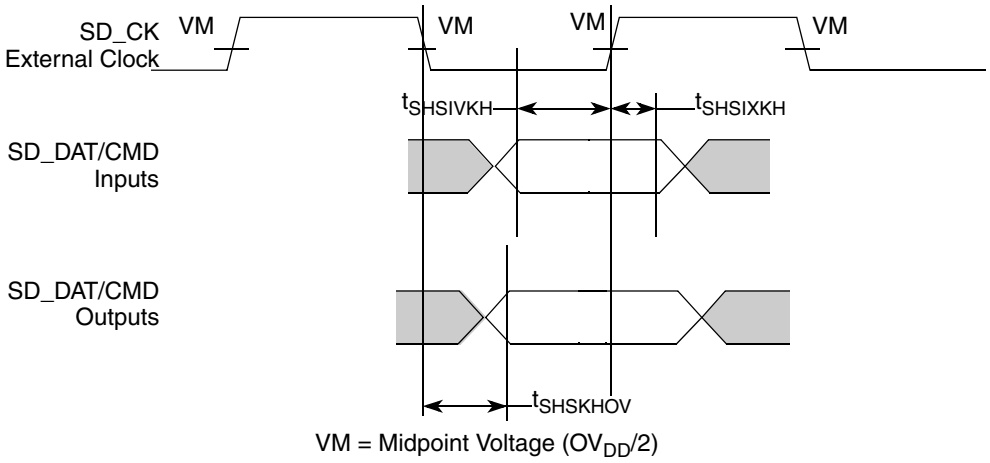


Figure 62. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8569E.

2.17.1 Timers DC Electrical Characteristics

The following table provides the timers DC electrical characteristics.

Table 70. Timers DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OVIN = 0 V or OVIN = OVDD)	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

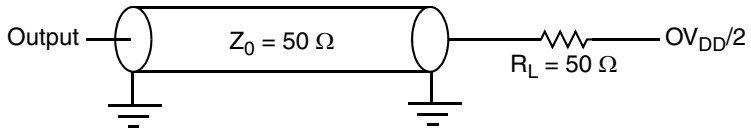


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

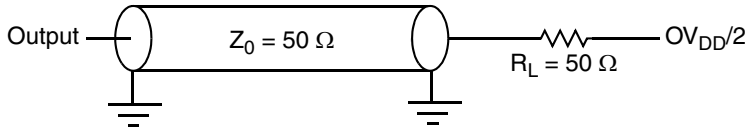
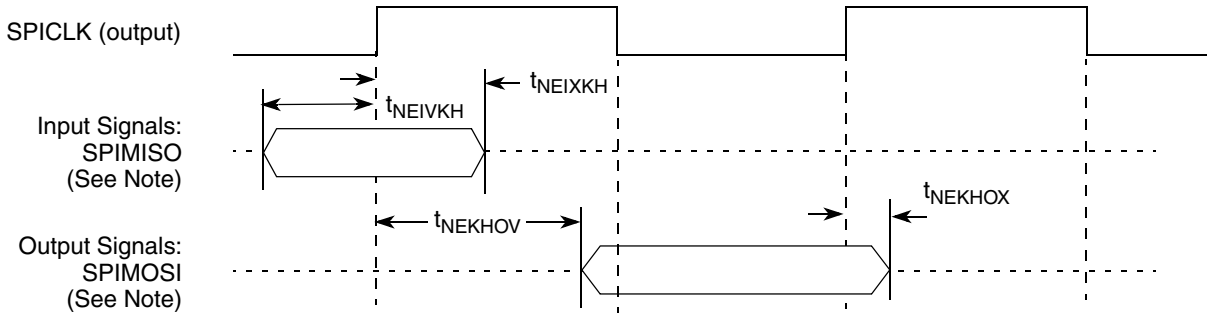


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the SPI timing in slave mode (external clock).

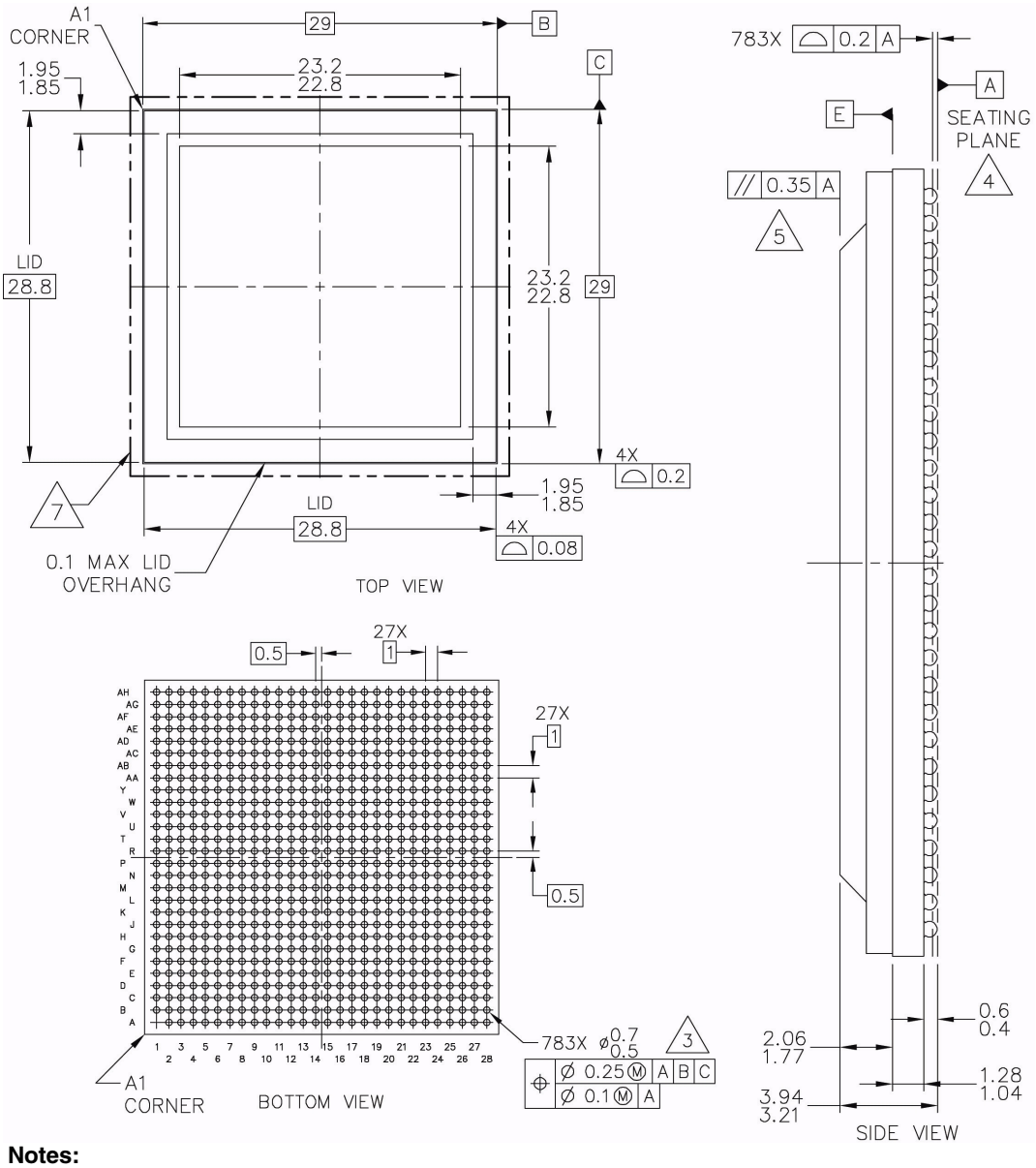


Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

4.2 Mechanical Dimensions of the FC-PBGA with Full Lid

The following figure shows the mechanical dimensions and bottom surface nomenclature for the MPC8569E FC-PBGA package with full lid.



Notes:

[1]All dimensions are in millimeters.
[2]Dimensions and tolerances per ASME Y14.5M-1994.
[3]Maximum solder ball diameter measured parallel to datum A.
[4]Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
[5]Parallelism measurement shall exclude any effect of mark on top surface of package.
[6]All dimensions are symmetric across the package center lines unless dimensioned otherwise.
[7]29.2 mm maximum package assembly (lid and laminate) x and y.

Figure 75. MPC8569E FC-PBGA Package with Full Lid