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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569evjaunlb

1.2 Pinout List

The following table provides the pinout listing for the MPC8569E 783 FC-PBGA package.

Table 1. MPC8569E Pinout Listing

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Clocks				
RTC	M25	I	OV_{DD}	—
SYSCLK	P25	I	OV_{DD}	—
DDR SDRAM Memory Interface				
D1_MA0	E18	O	GV_{DD}	—
D1_MA1	A18	O	GV_{DD}	—
D1_MA2	H19	O	GV_{DD}	—
D1_MA3	G20	O	GV_{DD}	—
D1_MA4	B18	O	GV_{DD}	—
D1_MA5	H18	O	GV_{DD}	—
D1_MA6	C18	O	GV_{DD}	—
D1_MA7	J21	O	GV_{DD}	—
D1_MA8	E19	O	GV_{DD}	—
D1_MA9	G19	O	GV_{DD}	—
D1_MA10	J18	O	GV_{DD}	—
D1_MA11	A19	O	GV_{DD}	—
D1_MA12	J22	O	GV_{DD}	—
D1_MA13	A15	O	GV_{DD}	—
D1_MA14	D20	O	GV_{DD}	—
D1_MA15	C15	O	GV_{DD}	—
D1_MBA0	K17	O	GV_{DD}	—
D1_MBA1	F18	O	GV_{DD}	—
D1_MBA2	E20	O	GV_{DD}	—
$\overline{\text{D1\_MCAS}}$	J17	O	GV_{DD}	—
D1_MCK0	E24	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	E23	O	GV_{DD}	—
D1_MCK1	J24	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	J23	O	GV_{DD}	—
D1_MCK2	C20	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	C19	O	GV_{DD}	—
D1_MCKE0	G21	O	GV_{DD}	—
D1_MCKE1	J20	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	AF11	—	—	—
GND	AF2	—	—	—
GND	AG15	—	—	—
GND	AG17	—	—	—
GND	AG19	—	—	—
GND	AG21	—	—	—
GND	AG24	—	—	—
GND	AG7	—	—	—
GND	AH23	—	—	—
GND	AH25	—	—	—
GND	B13	—	—	—
GND	B17	—	—	—
GND	B20	—	—	—
GND	B23	—	—	—
GND	B27	—	—	—
GND	B3	—	—	—
GND	B6	—	—	—
GND	B9	—	—	—
GND	C4	—	—	—
GND	D11	—	—	—
GND	D16	—	—	—
GND	D19	—	—	—
GND	D2	—	—	—
GND	D25	—	—	—
GND	D28	—	—	—
GND	D5	—	—	—
GND	E13	—	—	—
GND	F17	—	—	—
GND	F20	—	—	—
GND	F23	—	—	—
GND	F27	—	—	—
GND	F3	—	—	—
GND	F6	—	—	—
GND	F9	—	—	—
GND	H1	—	—	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Range	Unit	Notes
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	–0.3 to 3.63 –0.3 to 2.75	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Ethernet signals	LV_{IN}	–0.3 to ($LV_{DD}n$ + 0.3)	V	3
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

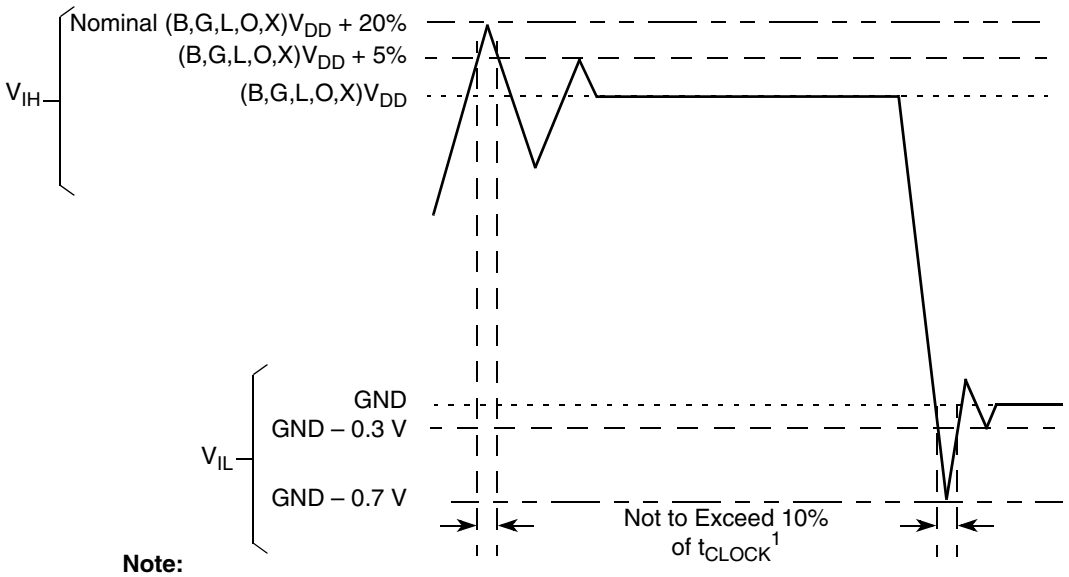
2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
PLL supply voltage	AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	1.0 V ± 30 mV 1.1 V ± 33 mV	V	2

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.4 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 7. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OVDD/CVDD/GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range may falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.2 Power Characteristics

The following table shows the power dissipations of the V_{DD} supply for various operating core complex bus clock (CCB_clk) frequencies versus the core, DDR data rate, and QUICC Engine block frequencies. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 8. MPC8569E Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	800	400	600	400	1.0	65	3.4 W	1, 2
Thermal						105	4.9 W	1, 3
Maximum							5.4 W	1, 4
Typical	1067	533	667	533	1.0	65	3.9 W	1, 2
Thermal						105	5.4 W	1, 3
Maximum							6.0 W	1, 4

The following table provides the system clock (SYSCLK) AC timing specifications.

Table 10. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15.15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.3.1 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in below table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the MPC8569E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the MPC8569E is compatible with spread spectrum sources if the recommendations listed in the following table are observed.

Table 11. Spread Spectrum Clock Source Recommendations

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 10.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.4.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Table 13. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.125	—	V	5
Input low voltage	V_{IL}	—	MVREF*n* – 0.125	V	5
Output high current (V_{OUT} = 1.320 V)	I_{OH}	—	–13.4	mA	6, 7
Output low current (V_{OUT} = 0.380 V)	I_{OL}	13.4	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±2% of GV_{DD} (that is, ± 36 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 16.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. I_{OH} and I_{OL} are measured at GV_{DD} = 1.7 V.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 14. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4

2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	—
RX_CLK clock rise time (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

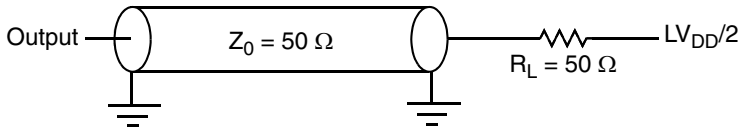


Figure 13. GMII AC Test Load

The following figure shows the GMII receive AC timing diagram.

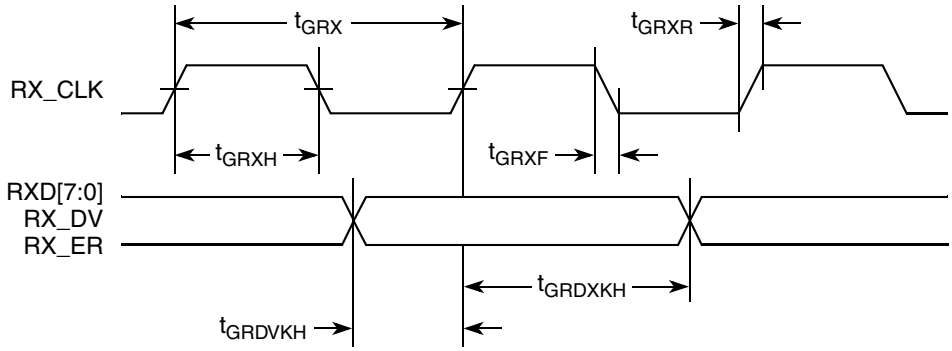


Figure 14. GMII Receive AC Timing Diagram

2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.6.3.2.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

The following figure shows the MII transmit AC timing diagram.

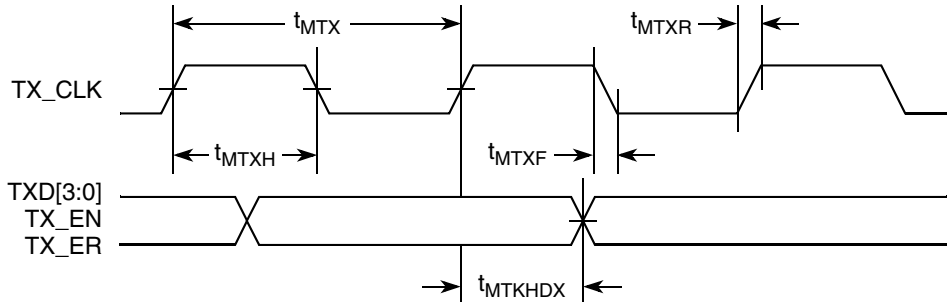


Figure 15. MII Transmit AC Timing Diagram

2.6.3.2.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns	1
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns	1
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	2
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 33. TBI Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns	—
PMA_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns	2
PMA_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

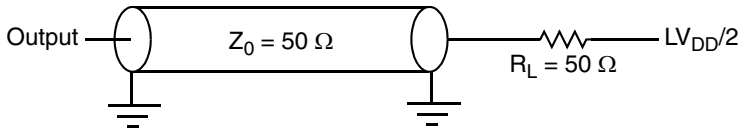


Figure 23. AC Test Load

The following figure shows the TBI receive AC timing diagram.

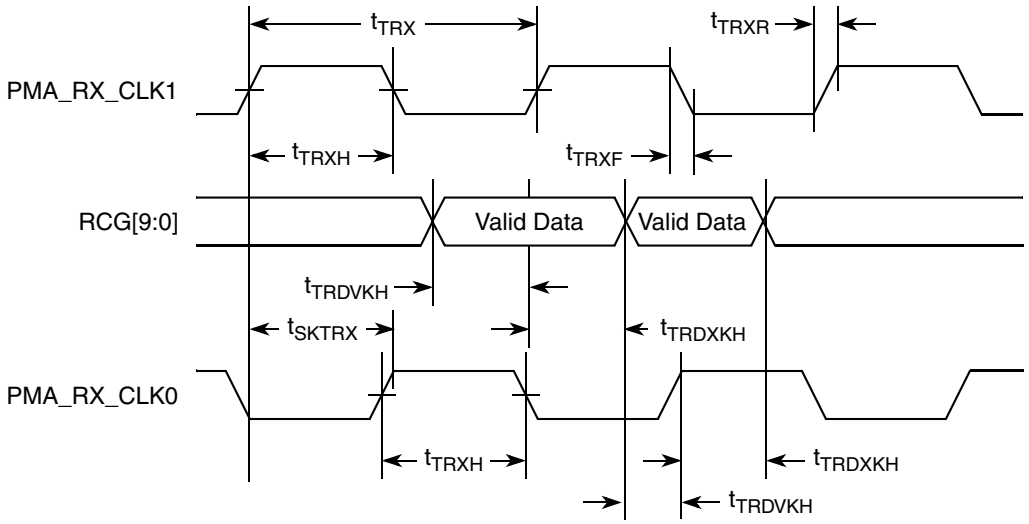


Figure 24. TBI Receive AC Timing Diagram

The following figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

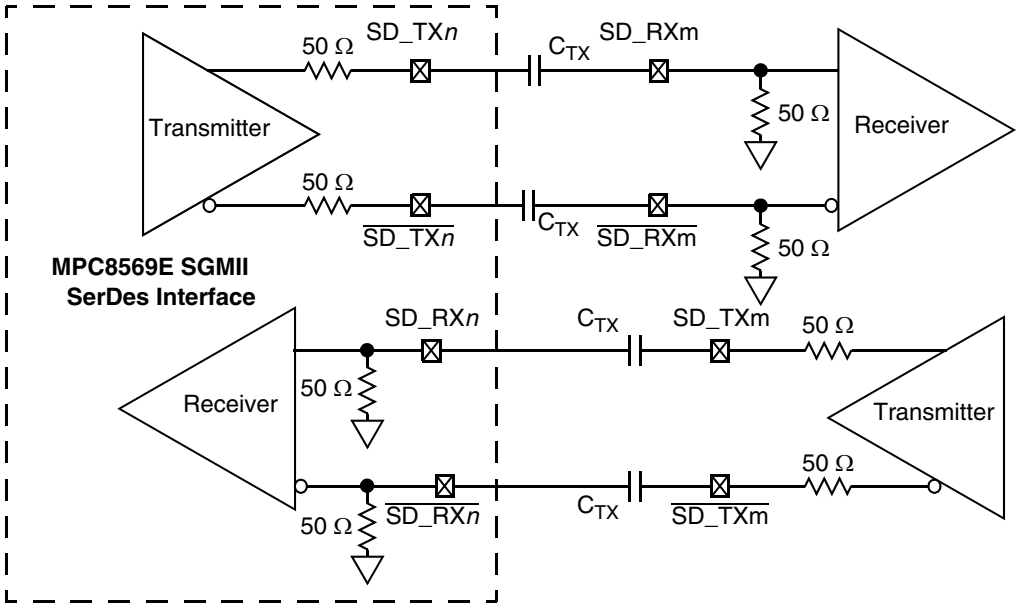


Figure 27. 4-Wire AC-Coupled SGMII Serial Link Connection Example

The following figure shows the SGMII transmitter DC measurement circuit.

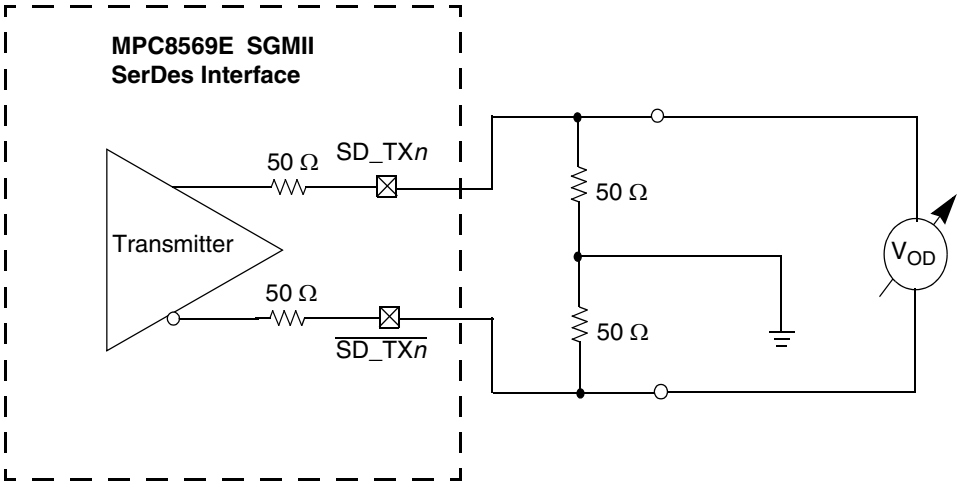


Figure 28. SGMII Transmitter DC Measurement Circuit

The following figure shows the data and command input AC timing diagram.

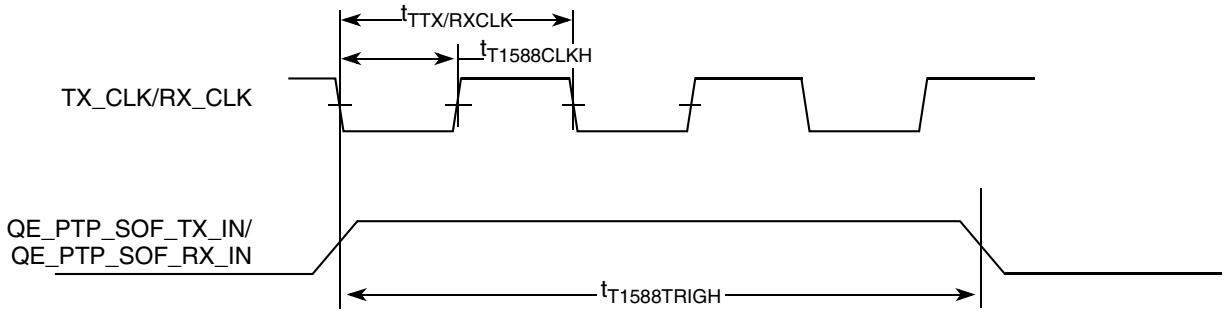


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes.The SerDes reference clock inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express, Serial RapidIO, and SGMII interface, respectively.

The following sections describe the SerDes reference clock requirements and provide application information.

2.9.2.1 SerDes Spread Spectrum Clock Source Recommendations

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are designed to work with spread spectrum clock for PCI Express protocol only with the spreading specification defined in Table 47. When using spread spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The spread spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread spectrum supported protocols. For example, if the spread spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII/SRIO due to the SerDes lane usage mapping option, spread spectrum clocking cannot be used at all.

Table 47. SerDes Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	–0.5	%	1

Note:

1. Only down spreading is allowed.

2.9.2.2 SerDes Reference Clock Receiver Characteristics

The following figure shows a receiver reference diagram of the SerDes reference clocks.

The following table defines the serial RapidIO receiver DC specifications.

Table 54. SRIO Receiver DC Timing Specifications—1.25 GBaud, 2.5 GBaud, 3.125 GBaud

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:
1. Measured at receiver

2.11.4 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.11.4.1 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the Serial RapidIO clock requirements for SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, “AC Requirements for SerDes Reference Clocks.”

The following figure provides the boundary-scan timing diagram.

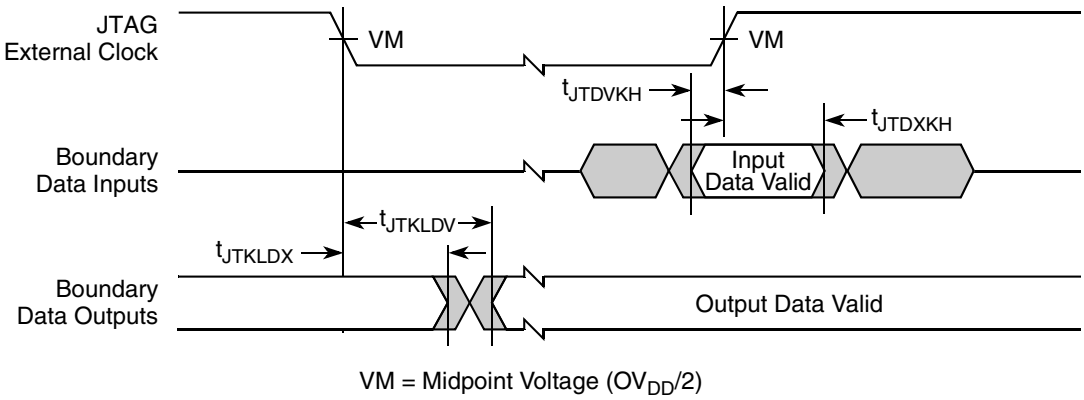


Figure 55. Boundary-Scan Timing Diagram

2.15 Enhanced Local Bus Controller

This section describes the DC and AC electrical specifications for the enhanced local bus interface of the MPC8569E.

2.15.1 Enhanced Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 3.3 V DC.

Table 63. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, “Recommended Operating Conditions.”

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3, 2.5, and 1.8 V DC with PLL disabled.

Table 67. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)—PLL Bypassed

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	12	—	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	6
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LUPWAIT/LFRB)	t_{LBIVKH}	6.5	—	ns	—
Input hold (except LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LUPWAIT/LFRB)	t_{LBIVKL}	6.5	—	ns	—
Input hold (for LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 1 ns (LBCR[AHD] = 0) 1/2 – 1 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (=1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

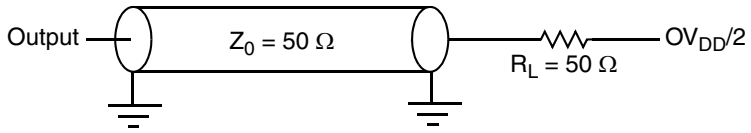


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

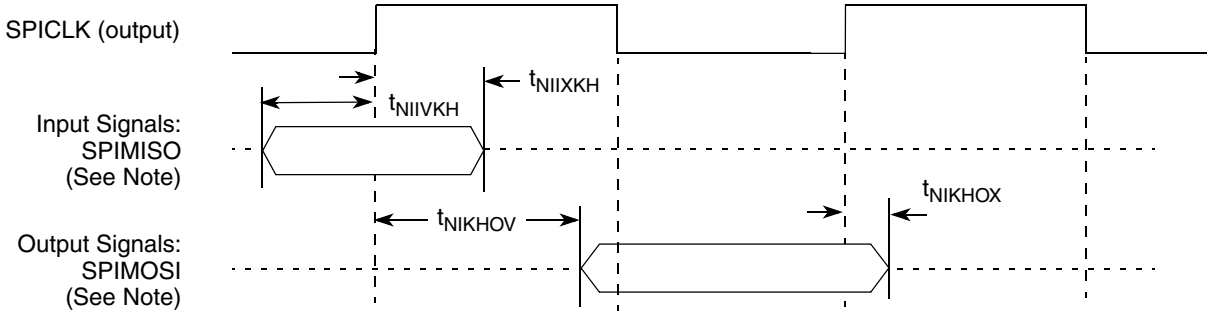
Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

2.21 USB Interface

This section provides the AC and DC electrical specifications for the USB interface of the MPC8569E.

2.21.1 USB DC Electrical Characteristics

The following table provides the USB DC electrical characteristics.

Table 78. USB DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—
Differential input sensitivity	V_{DI}	0.2	—	V	3
Differential common mode range	V_{CM}	0.8	2.5	V	3

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.
3. Applies to low/full speed

2.21.2 USB AC Electrical Specifications

The following table describes the general USB timing specifications.

Table 79. USB General Timing Parameters

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	2
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full-speed transitions, 2
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low-speed transitions, 2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

5 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

Ordering information for the parts fully covered by this specification document is provided in Section 5.1, "Part Numbers Fully Addressed by This Document."

5.1 Part Numbers Fully Addressed by This Document

The following table shows the device nomenclature.

Table 84. Device Nomenclature

MPC	nnnn	E	C	Vx	AA	X	G	R
Product Code[1]	**Part Identifier**	**Security Engine**	**Temperature Range**	**Package** [2]	**Processor Frequency** [3]	**DDR Frequency**[4]	**QE Frequency**	**Revision Level**
MPC PPC	8569	E = included	Blank = 0° to 105°C C = –40° to 105°C	VT = FC-PBGA, Pb free, C5 spheres VJ = FC-PBGA, Pb free C4 bumps and pb free C5 spheres	AN = 800 MHz AQ = 1067 MHz AU = 1333 MHz	K = 600 MHz L = 667 MHz N = 800 MHz	G = 400 MHz J = 533 MHz L = 667 MHz	Blank = Rev. 1.0 (SVR = 0x8088_0010 A = Rev. 2.0 (SVR = 0x8088_0020 B = Rev. 2.1 (SVR = 0x8088_0021
		Blank = not included						A = Rev. 2.0 (SVR = 0x8080_0020 B = Rev. 2.1 (SVR = 0x8080_0021

Notes:

1. MPC stands for "qualified." PPC stands for pre-production samples.
2. See Section 4, "Package Description," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
4. See Table 85 for the corresponding maximum platform frequency.
5. C5 spheres are used by customer to attach to pcb. C4 bumps are bumps used on die of the device to connect between die and package substrate.