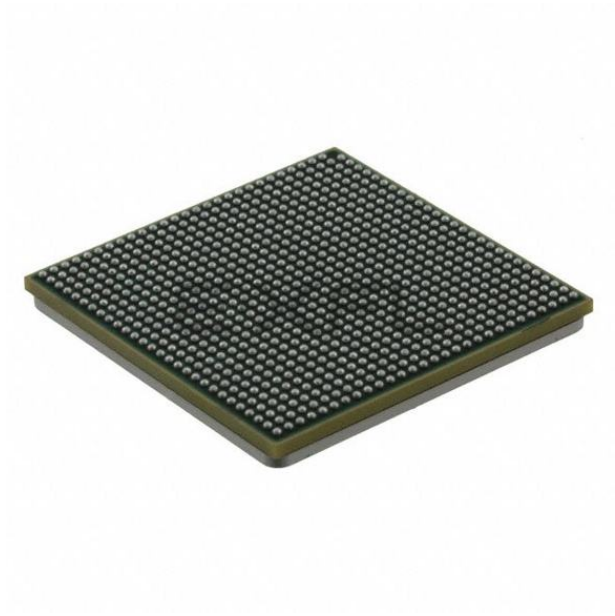

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569evtankgb

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MCKE2	C17	O	GV_{DD}	—
D1_MCKE3	A16	O	GV_{DD}	—
$\overline{\text{D1\_MCS0}}$	D17	O	GV_{DD}	—
$\overline{\text{D1\_MCS1}}$	K16	O	GV_{DD}	—
$\overline{\text{D1\_MCS2}}$	K20	O	GV_{DD}	—
$\overline{\text{D1\_MCS3}}$	G16	O	GV_{DD}	—
D1_MDIC0	A20	I/O	GV_{DD}	27
D1_MDIC1	A17	I/O	GV_{DD}	27
D1_MDM0	A27	I/O	GV_{DD}	—
D1_MDM1	E27	I/O	GV_{DD}	—
D1_MDM2	J27	I/O	GV_{DD}	—
D1_MDM3	A23	I/O	GV_{DD}	—
D1_MDM8	E22	I/O	GV_{DD}	—
D1_MDQ0	C28	I/O	GV_{DD}	—
D1_MDQ1	C27	I/O	GV_{DD}	—
D1_MDQ2	C25	I/O	GV_{DD}	—
D1_MDQ3	B25	I/O	GV_{DD}	—
D1_MDQ4	B28	I/O	GV_{DD}	—
D1_MDQ5	A28	I/O	GV_{DD}	—
D1_MDQ6	A26	I/O	GV_{DD}	—
D1_MDQ7	A25	I/O	GV_{DD}	—
D1_MDQ8	G28	I/O	GV_{DD}	—
D1_MDQ9	G27	I/O	GV_{DD}	—
D1_MDQ10	G25	I/O	GV_{DD}	—
D1_MDQ11	F25	I/O	GV_{DD}	—
D1_MDQ12	F28	I/O	GV_{DD}	—
D1_MDQ13	E28	I/O	GV_{DD}	—
D1_MDQ14	E26	I/O	GV_{DD}	—
D1_MDQ15	E25	I/O	GV_{DD}	—
D1_MDQ16	L27	I/O	GV_{DD}	—
D1_MDQ17	L26	I/O	GV_{DD}	—
D1_MDQ18	K23	I/O	GV_{DD}	—
D1_MDQ19	K25	I/O	GV_{DD}	—
D1_MDQ20	K28	I/O	GV_{DD}	—
D1_MDQ21	J28	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PA19	P1	I/O	OV_{DD}	—
QE_PA20	M5	I/O	$LV_{DD}2$	—
QE_PA21	N5	I/O	$LV_{DD}2$	—
QE_PA22	L4	I/O	$LV_{DD}2$	—
QE_PA23	M4	I/O	$LV_{DD}2$	—
QE_PA24	N1	I/O	OV_{DD}	—
QE_PA25	R1	I/O	OV_{DD}	—
QE_PA26	N4	I/O	$LV_{DD}2$	—
QE_PA27	T1	I/O	OV_{DD}	—
QE_PA28	N2	I/O	OV_{DD}	—
QE_PA29	P6	I/O	$LV_{DD}1$	—
QE_PA30	U6	I/O	$LV_{DD}1$	—
QE_PA31	T5	I/O	$LV_{DD}1$	—
QE_PB0	R5	I/O	$LV_{DD}1$	—
QE_PB1	P5	I/O	$LV_{DD}1$	—
QE_PB2	V6	I/O	OV_{DD}	—
QE_PB3	T3	I/O	$LV_{DD}1$	—
QE_PB4	U3	I/O	$LV_{DD}1$	—
QE_PB5	U4	I/O	$LV_{DD}1$	—
QE_PB6	U5	I/O	$LV_{DD}1$	—
QE_PB7	V3	I/O	OV_{DD}	11
QE_PB8	V4	I/O	OV_{DD}	—
QE_PB9	P4	I/O	$LV_{DD}1$	—
QE_PB10	V5	I/O	OV_{DD}	—
QE_PB11	W11	I/O	OV_{DD}	—
QE_PB12	L11	I/O	$LV_{DD}2$	—
QE_PB13	M11	I/O	$LV_{DD}2$	—
QE_PB14	N11	I/O	$LV_{DD}2$	—
QE_PB15	P11	I/O	$LV_{DD}2$	—
QE_PB16	P10	I/O	$LV_{DD}2$	—
QE_PB17	P2	I/O	OV_{DD}	—
QE_PB18	L10	I/O	$LV_{DD}2$	—
QE_PB19	M9	I/O	$LV_{DD}2$	—
QE_PB20	N9	I/O	$LV_{DD}2$	—
QE_PB21	P9	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y18	1.0-V/1.1-V core power supply	V_{DD}	—
BV_{DD}	AC15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
GV_{DD}	B12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B2	1.8-/1.5-V DDR power supply	GV_{DD}	—

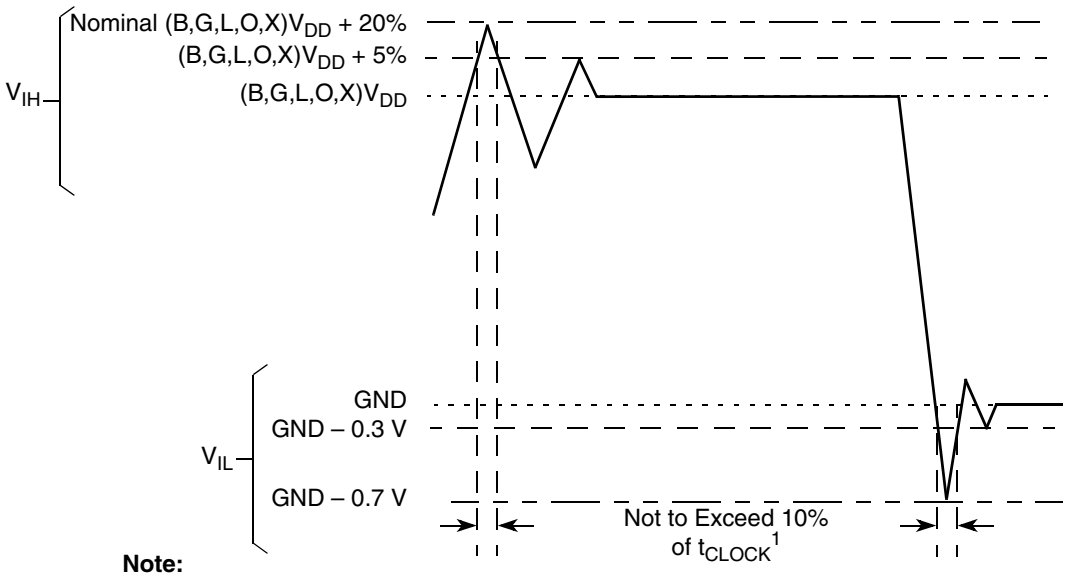
Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	Y13	—	—	—
GND	Y15	—	—	—
GND	Y16	—	—	—
GND	Y17	—	—	—
GND	Y19	—	—	—
GND	V20	—	—	—
GND	T20	—	—	—
GND	W20	—	—	—
GND	Y20	—	—	—
SENSEVSS	P15	Ground sense	—	13
SCOREGND	AA27	SerDes Core Logic GND	—	—
SCOREGND	AB26	SerDes Core Logic GND	—	—
SCOREGND	AC28	SerDes Core Logic GND	—	—
SCOREGND	R28	SerDes Core Logic GND	—	—
SCOREGND	T26	SerDes Core Logic GND	—	—
SCOREGND	U27	SerDes Core Logic GND	—	—
SCOREGND	V25	SerDes Core Logic GND	—	—
SCOREGND	W28	SerDes Core Logic GND	—	—
SCOREGND	Y26	SerDes Core Logic GND	—	—
XGND	AA24	SerDes Transceiver Pad GND	—	—
XGND	AB22	SerDes Transceiver Pad GND	—	—
XGND	AB25	SerDes Transceiver Pad GND	—	—
XGND	AC23	SerDes Transceiver Pad GND	—	—
XGND	R24	SerDes Transceiver Pad GND	—	—

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

The following table provides the system clock (SYSCLK) AC timing specifications.

Table 10. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15.15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.3.1 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in below table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the MPC8569E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the MPC8569E is compatible with spread spectrum sources if the recommendations listed in the following table are observed.

Table 11. Spread Spectrum Clock Source Recommendations

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 10.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	—
RX_CLK clock rise time (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

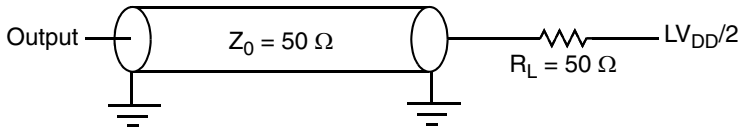


Figure 13. GMII AC Test Load

The following figure shows the GMII receive AC timing diagram.

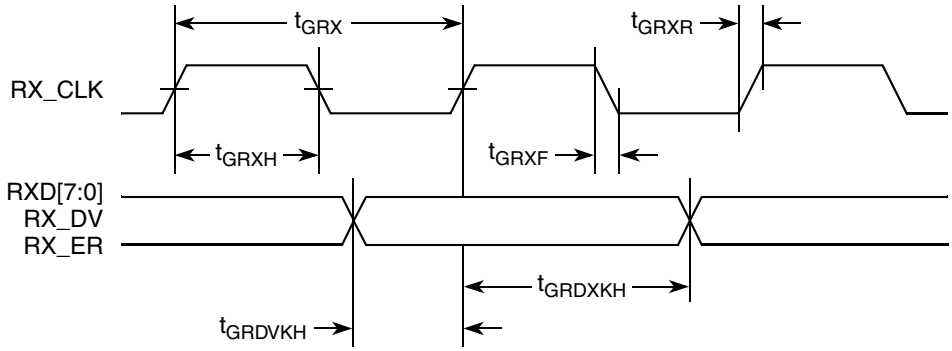


Figure 14. GMII Receive AC Timing Diagram

2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

The following figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

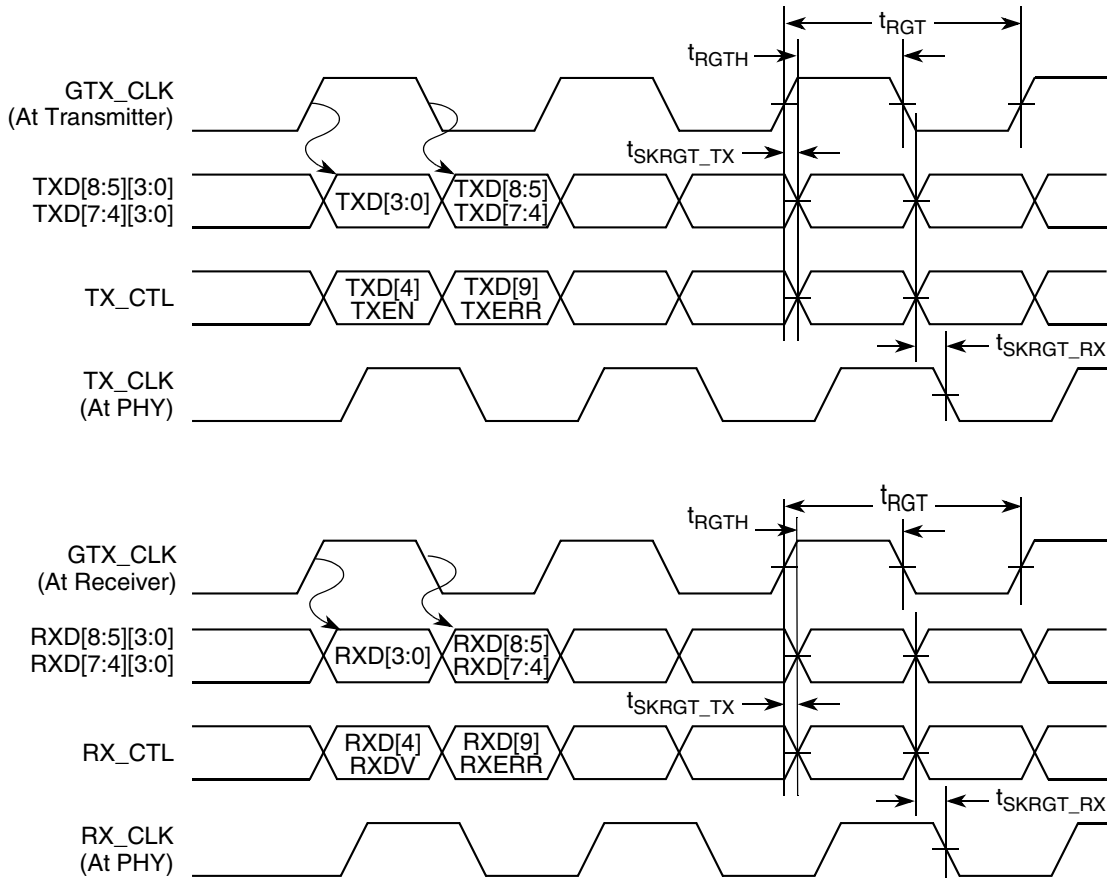


Figure 26. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.6.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of MPC8569E as shown in Figure 27, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 45.

2.6.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.6.4.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.9.2.3, “DC Level Requirement for SerDes Reference Clocks.”

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1.3	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 46. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

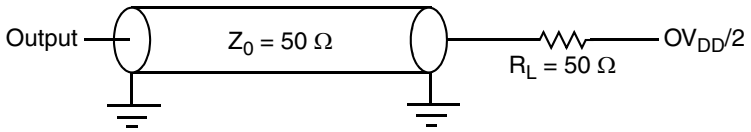


Figure 35. AC Test Load

2.13 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.13.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the GPIO interface when operating from a 3.3 V supply

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.13.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

The following figure provides the AC test load for the GPIO.

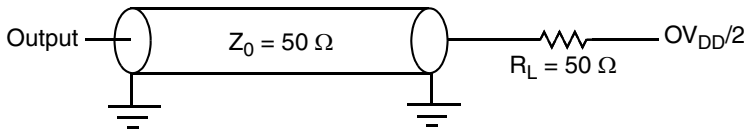


Figure 51. GPIO AC Test Load

Table 62. JTAG AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times: Boundary-scan data TDO	t_{JTKLDV}	 — —	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the AC test load for TDO and the boundary-scan outputs of the device.

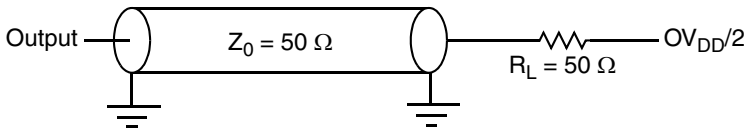


Figure 52. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

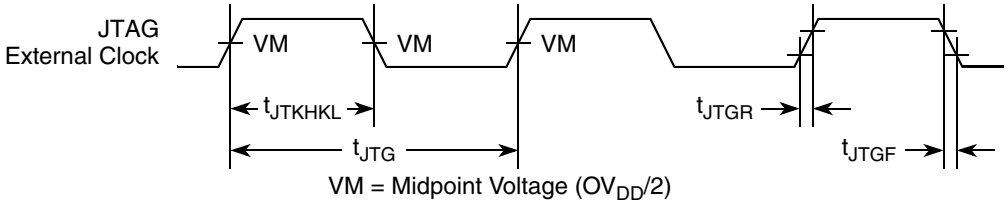


Figure 53. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

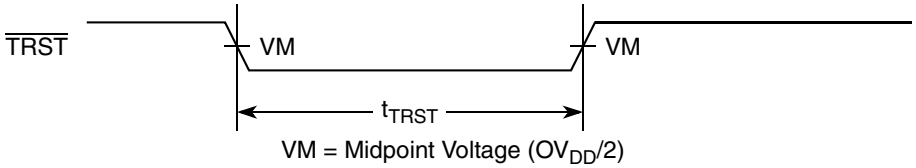


Figure 54. $\overline{\text{TRST}}$ Timing Diagram

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 2.5 V DC.

Table 64. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 1.8 V DC.

Table 65. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

2.15.2 Enhanced Local Bus AC Electrical Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.15.2.1 Test Condition

The following figure provides the AC test load for the enhanced local bus.

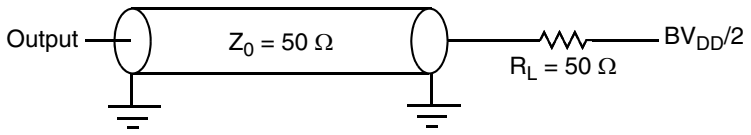


Figure 56. Enhanced Local Bus AC Test Load

The following figure shows the AC timing diagram for PLL-enabled mode.

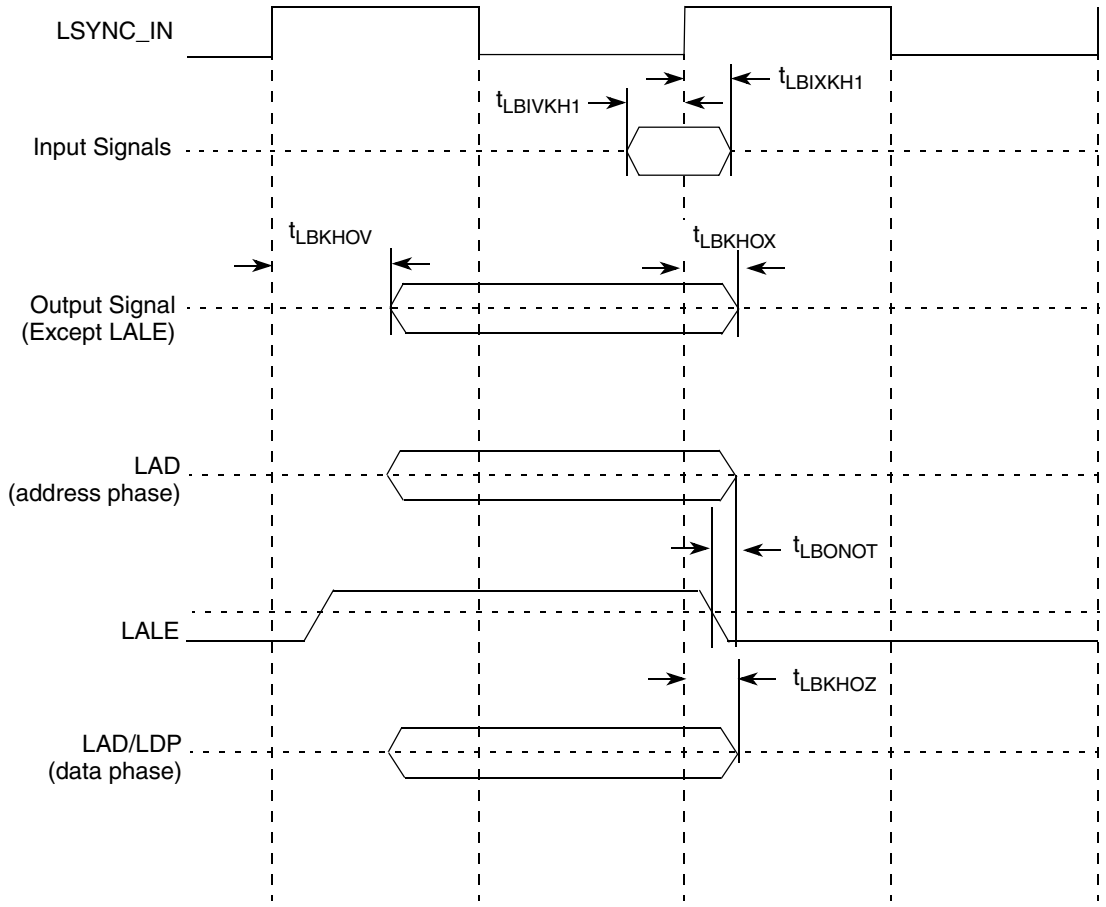


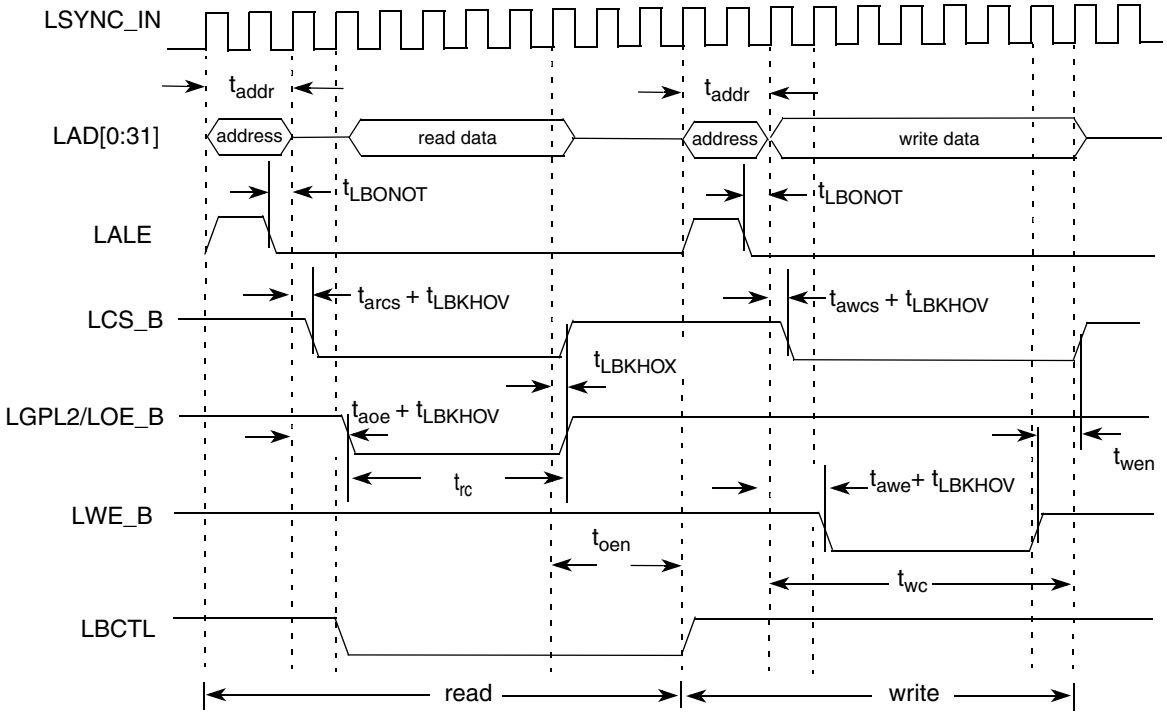
Figure 57. Local Bus AC Timing Diagram (PLL Enabled)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to reference manual.

Figure 58. GPCM Output Timing Diagram (PLL Enabled)

2.15.2.3 Enhanced Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LUPWAIT/LFRB are relative to the rising edge of LCLKs. LUPWAIT/LFRB are relative to the falling edge of LCLKs.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3, 2.5, and 1.8 V DC with PLL disabled.

Table 67. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)—PLL Bypassed

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	12	—	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	6
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LUPWAIT/LFRB)	t_{LBIVKH}	6.5	—	ns	—
Input hold (except LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LUPWAIT/LFRB)	t_{LBIVKL}	6.5	—	ns	—
Input hold (for LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 1 ns (LBCR[AHD] = 0) 1/2 – 1 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (=1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.18.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 73. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.19 SPI Interface

This section describes the SPI DC and AC electrical specifications of the MPC8569E.

2.19.1 SPI DC Electrical Characteristics

The following table provides the SPI DC electrical characteristics.

Table 74. SPI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 75. SPI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	9	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

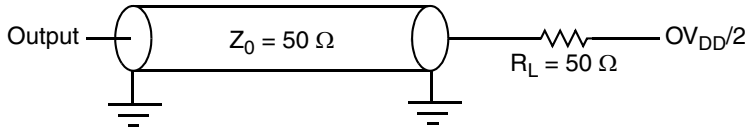
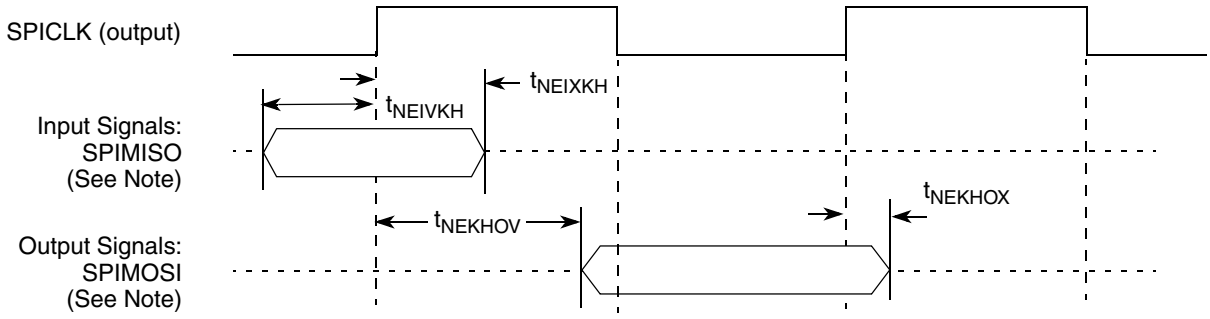


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

3.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the package. This spring force should not exceed 10 pounds force (45 Newtons).

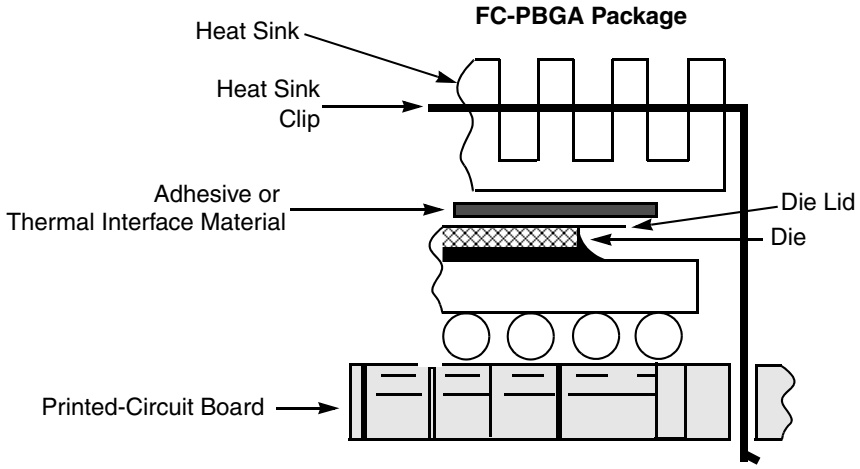


Figure 73. Package Exploded Cross-Sectional View

The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.3.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

5.2 Part Marking

Parts are marked as the example shown in the following figure.

FC-PBGA

Notes:
MPC8569xxxxxx is the orderable part number.
MMMMM is the mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
ATWLYYWW is the traceability code.

Figure 76. Part Marking for FC-PBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8569E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8569ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)
- *QUICC Engine Block Reference Manual with Protocol Interworking* (document number: QEIWRM)

7 Document Revision History

The following table provides a revision history for this document.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
2	10/2013	• Added footnote 5 and added new VJ package description in Table 84, “Device Nomenclature.
1	02/2012	• In Table 1, “MPC8569E Pinout Listing,” updated pin U20 from Reserved to THERM1 (internal thermal diode anode) and pin U21 from Reserved to THERM0 (internal thermal diode cathode). Removed note 9 and added note 32 to pins U20 and U21. • In Table 38, “SGMII Transmit AC Timing Specifications,” updated min and typical values for the AC coupling capacitor parameter. • In Table 48, “SD_REF_CLK and SD_REF_CLK Input Clock Requirements,” removed the condition that the reference clock duty cycle should be measured at 1.6 V. • Added Section 2.6.5.1, “QUICC Engine Block IEEE 1588 DC Specifications.” • Added Section 3.3.3, “Temperature Diode.”
0	06/2011	Initial public release