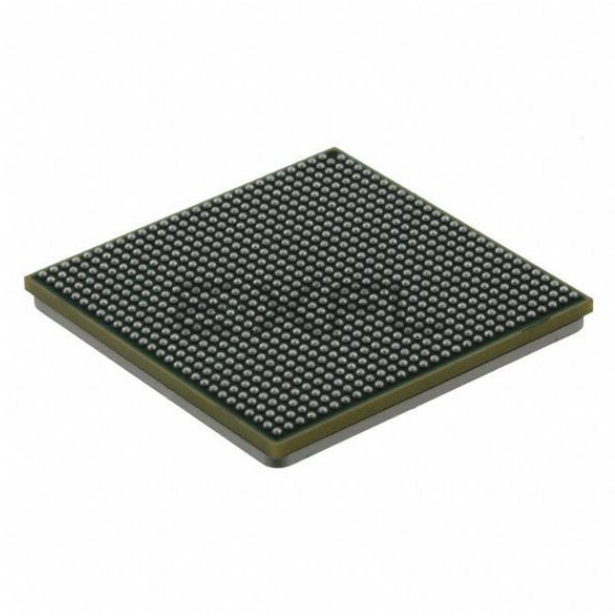

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569evtaqljb

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

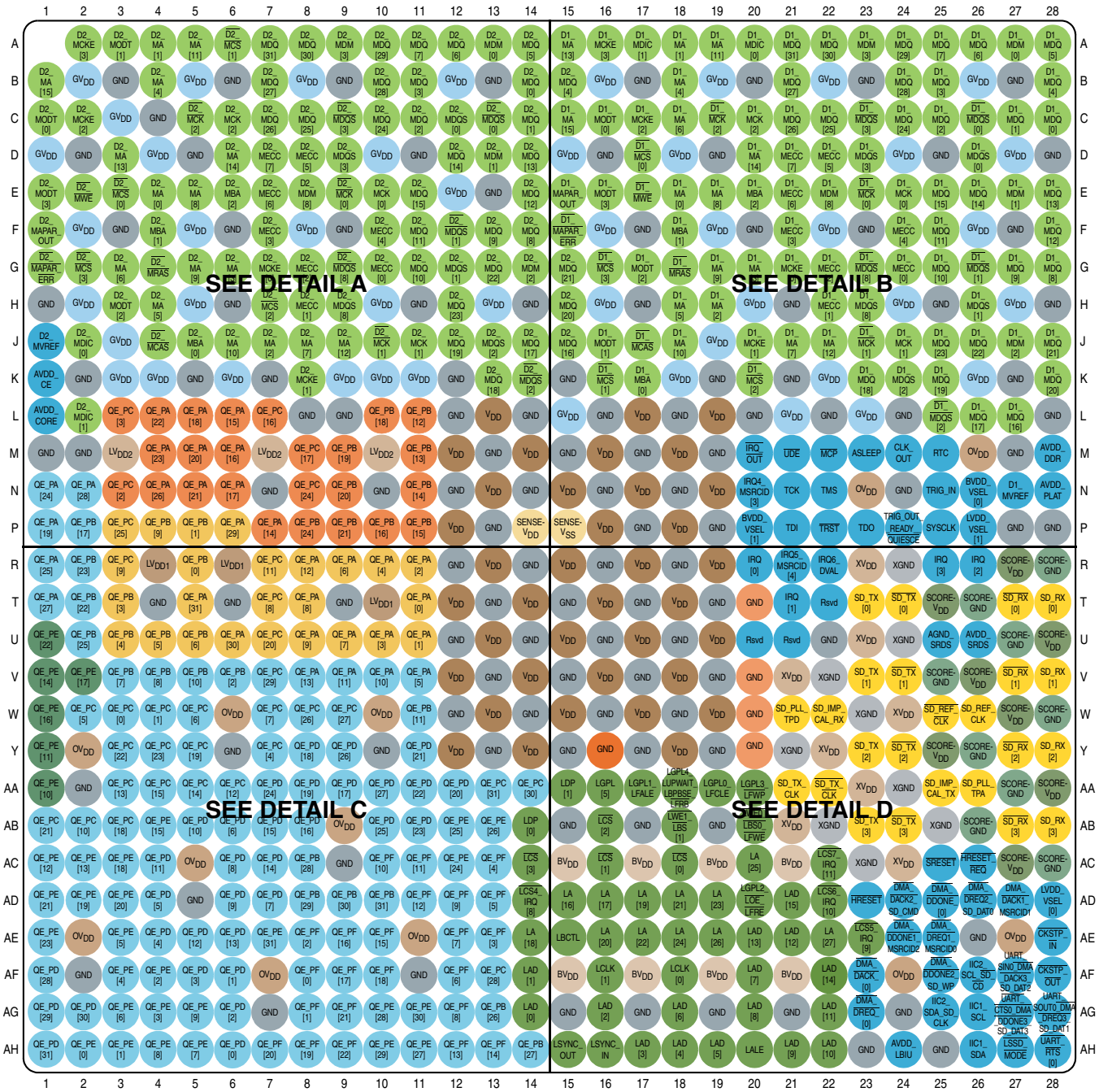


Figure 2. MPC8569E Top View Ballmap

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{D1\_MWE}}$	E17	O	GV_{DD}	—
D2_MA0	E4	O	GV_{DD}	—
D2_MA1	A4	O	GV_{DD}	—
D2_MA2	J7	O	GV_{DD}	—
D2_MA3	G6	O	GV_{DD}	—
D2_MA4	B4	O	GV_{DD}	—
D2_MA5	H4	O	GV_{DD}	—
D2_MA6	G3	O	GV_{DD}	—
D2_MA7	J8	O	GV_{DD}	—
D2_MA8	E5	O	GV_{DD}	—
D2_MA9	G5	O	GV_{DD}	—
D2_MA10	J6	O	GV_{DD}	—
D2_MA11	A5	O	GV_{DD}	—
D2_MA12	J9	O	GV_{DD}	—
D2_MA13	D3	O	GV_{DD}	—
D2_MA14	D6	O	GV_{DD}	—
D2_MA15	B1	O	GV_{DD}	—
D2_MBA0	J5	O	GV_{DD}	—
D2_MBA1	F4	O	GV_{DD}	—
D2_MBA2	E6	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	J4	O	GV_{DD}	—
D2_MCK0	E10	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	E9	O	GV_{DD}	—
D2_MCK1	J11	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	J10	O	GV_{DD}	—
D2_MCK2	C6	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	C5	O	GV_{DD}	—
D2_MCKE0	G7	O	GV_{DD}	—
D2_MCKE1	K8	O	GV_{DD}	—
D2_MCKE2	C2	O	GV_{DD}	—
D2_MCKE3	A2	O	GV_{DD}	—
$\overline{\text{D2\_MCS0}}$	E3	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	A6	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	H7	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	G2	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PD28	AF1	I/O	OV_{DD}	—
QE_PD29	AG1	I/O	OV_{DD}	—
QE_PD30	AG2	I/O	OV_{DD}	—
QE_PD31	AH1	I/O	OV_{DD}	—
QE_PE0	AH2	I/O	OV_{DD}	—
QE_PE1	AH3	I/O	OV_{DD}	—
QE_PE2	AF4	I/O	OV_{DD}	—
QE_PE3	AG4	I/O	OV_{DD}	—
QE_PE4	AF3	I/O	OV_{DD}	—
QE_PE5	AE3	I/O	OV_{DD}	—
QE_PE6	AG3	I/O	OV_{DD}	—
QE_PE7	AH5	I/O	OV_{DD}	—
QE_PE8	AH4	I/O	OV_{DD}	—
QE_PE9	AG5	I/O	OV_{DD}	—
QE_PE10	AA1	I/O	OV_{DD}	—
QE_PE11	Y1	I/O	OV_{DD}	—
QE_PE12	AC1	I/O	OV_{DD}	—
QE_PE13	AC2	I/O	OV_{DD}	—
QE_PE14	V1	I/O	OV_{DD}	—
QE_PE15	AB4	I/O	OV_{DD}	—
QE_PE16	W1	I/O	OV_{DD}	—
QE_PE17	V2	I/O	OV_{DD}	—
QE_PE18	AC3	I/O	OV_{DD}	—
QE_PE19	AD2	I/O	OV_{DD}	—
QE_PE20	AD3	I/O	OV_{DD}	—
QE_PE21	AD1	I/O	OV_{DD}	—
QE_PE22	U1	I/O	OV_{DD}	—
QE_PE23	AE1	I/O	OV_{DD}	—
QE_PE24	AC12	I/O	OV_{DD}	11
QE_PE25	AB12	I/O	OV_{DD}	2
QE_PE26	AB13	I/O	OV_{DD}	11
QE_PE27	AH11	I/O	OV_{DD}	19
QE_PE28	AG10	I/O	OV_{DD}	19

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y18	1.0-V/1.1-V core power supply	V_{DD}	—
BV_{DD}	AC15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
GV_{DD}	B12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B2	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

2.1.4 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 7. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OVDD/CVDD/GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range may falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.2 Power Characteristics

The following table shows the power dissipations of the V_{DD} supply for various operating core complex bus clock (CCB_clk) frequencies versus the core, DDR data rate, and QUICC Engine block frequencies. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 8. MPC8569E Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	800	400	600	400	1.0	65	3.4 W	1, 2
Thermal						105	4.9 W	1, 3
Maximum							5.4 W	1, 4
Typical	1067	533	667	533	1.0	65	3.9 W	1, 2
Thermal						105	5.4 W	1, 3
Maximum							6.0 W	1, 4

Table 8. MPC8569E Power Dissipation (continued)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	1333	533	800	667	1.1	65	5.7 W	1, 2
Thermal						105	7.9 W	1, 3
Maximum							8.6 W	1, 4

Note:

1. These values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running the Dhrystone benchmark, using the *nominal* process and *recommended* core voltage (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the maximum power measured while running the Dhrystone benchmark, using the *worst case* process and *recommended* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions that keeps the execution unit maximally busy and a typical workload on platform interfaces, using the *worst case* process and *nominal* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
5. This table includes power numbers for the V_{DD}, AV_{DD}_n, and ScoreVDD rails.

2.3 Input Clocks

The following table provides the system clock (SYSCLK) DC specifications.

Table 9. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	10.5	11.5	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table provides the system clock (SYSCLK) AC timing specifications.

Table 10. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15.15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.3.1 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in below table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the MPC8569E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the MPC8569E is compatible with spread spectrum sources if the recommendations listed in the following table are observed.

Table 11. Spread Spectrum Clock Source Recommendations

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 10.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.3.2 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the core complex bus clock (CCB_clk). The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB_clk. That is, minimum clock high time is $2 \times t_{CCB\_clk}$, and minimum clock low time is $2 \times t_{CCB\_clk}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.3.3 Gigabit Ethernet Reference Clock Timing

The following table provides the gigabit Ethernet reference clock (TX_CLK) AC timing specifications.

Table 12. TX_CLK[3,4] AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV / 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
TX_CLK frequency	t_{G125}	—	125	—	MHz	—
TX_CLK cycle time	t_{G125}	—	8	—	ns	—
TX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1, 5
TX_CLK duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 5
TX_CLK jitter	—	—	—	± 150	ps	2, 5

Notes:

1. Rise and fall times for TX_CLK are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V, and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. TX_CLK is used to generate the GTX clock for the UEC transmitter with 2% degradation. The TX_CLK duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the UEC GTX_CLK. See Section 2.6.3.7, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Gigabit transmit 125-MHz source. This signal must be generated externally with a crystal or oscillator, or is sometimes provided by the PHY. TX_CLK is a 125-MHz input into the UCC Ethernet Controller and is used to generate all 125-MHz related signals and clocks in the following modes: GMII, TBI, RTBI, RGMII.
4. For GMII and TBI modes, TX_CLK is provided to UCC1 through QE_PC[8:11,14,15] (CLK9-12,15,16) and to UCC2 through QE_PC[2,3,6,7,15:17](CLK3,4,7,8,16:18). For RGMII and RTBI modes, TX_CLK is provided to UCC1 and UCC3 through QE_PC11(CLK12) and to UCC2 and UCC4 through QE_PC16 (CLK17).
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

2.3.4 Other Input Clocks

A description of the overall clocking of this device is available in the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and Enhanced Local Bus see the specific interface section.

2.4 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8569E. Note that the required GV_{DD}(typ) is 1.8 V for DDR2 SDRAM and GV_{DD}(typ) is 1.5 V for DDR3 SDRAM.

2.4.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

The following table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[*n*] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
≤ 667 MHz		–0.6	0.6		

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

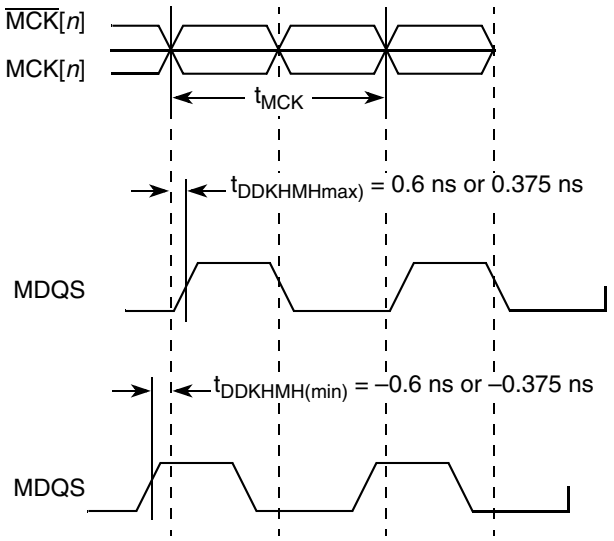


Figure 9. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

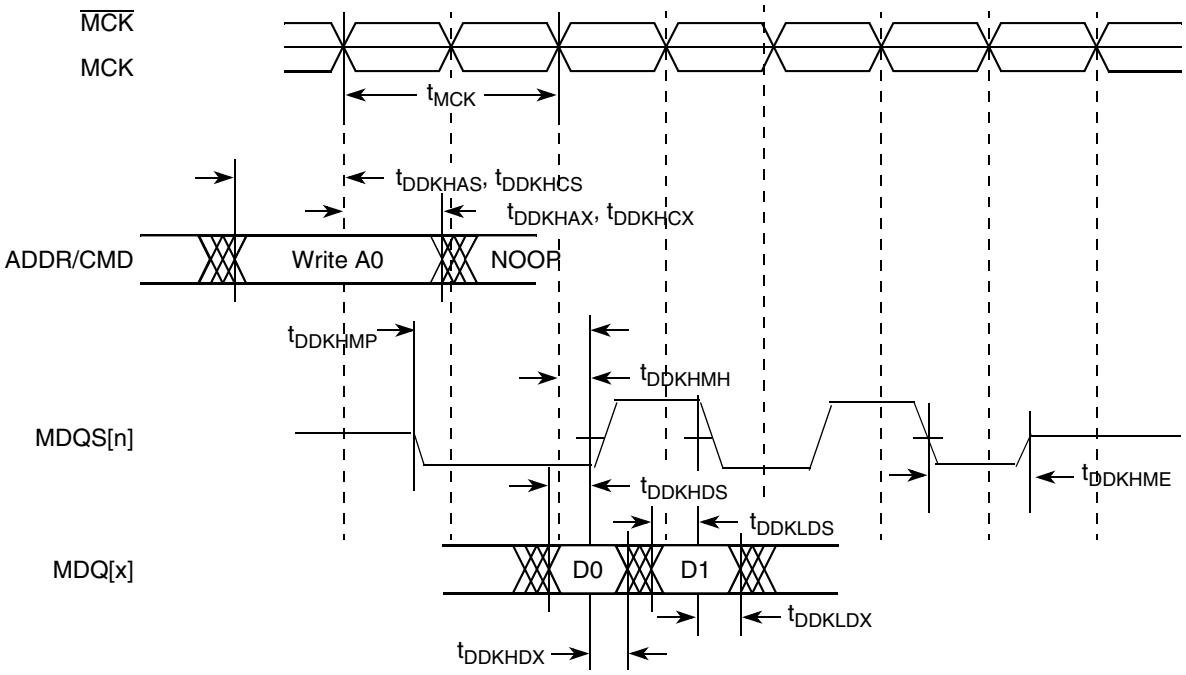


Figure 10. DDR2 and DDR3 Output Timing Diagram

2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	—
RX_CLK clock rise time (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

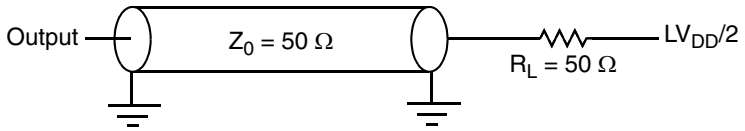


Figure 13. GMII AC Test Load

The following figure shows the GMII receive AC timing diagram.

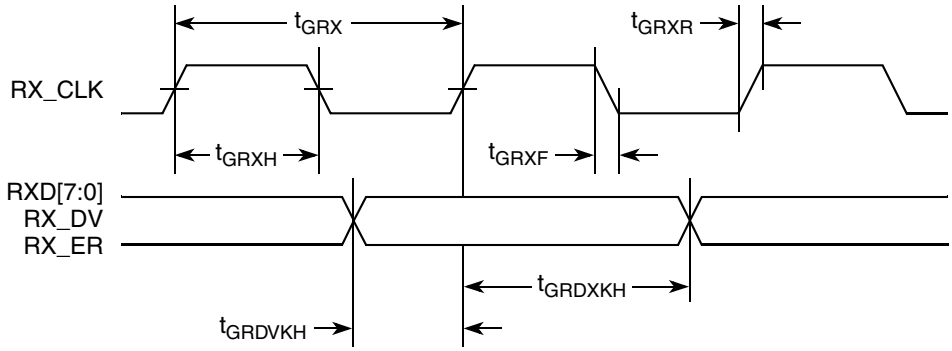


Figure 14. GMII Receive AC Timing Diagram

2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.6.3.4 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.6.3.4.1 RMII Transmit AC Timing Specifications

The following table shows the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMT}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMTH}	35	—	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	4.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	4.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

The following figure shows the RMII transmit AC timing diagram.

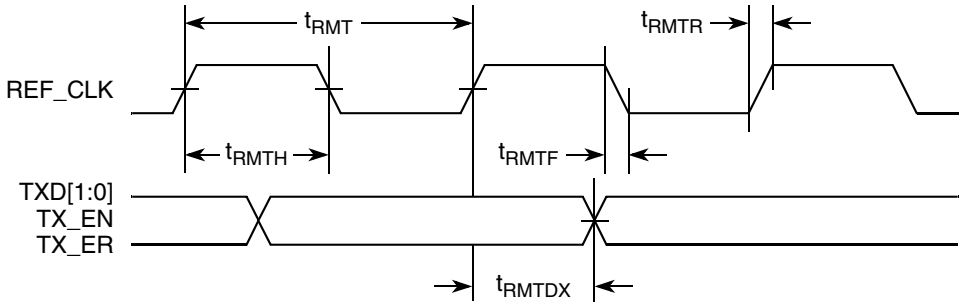


Figure 19. RMII Transmit AC Timing Diagram

2.6.3.4.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMR}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMRH}	35	—	65	%	1
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	1
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1

Table 31. RMII Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	4.0	ns	1
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns	—

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

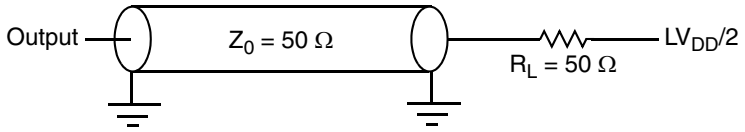


Figure 20. AC Test Load

The following figure shows the RMII receive AC timing diagram.

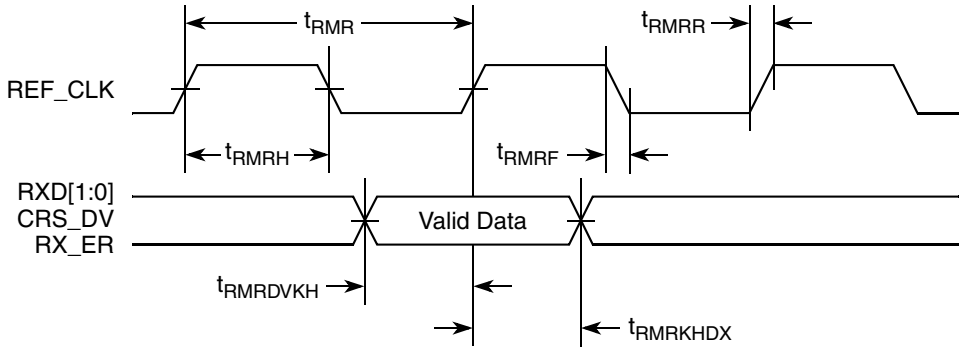


Figure 21. RMII Receive AC Timing Diagram

2.6.3.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

Table 36. SGMII DC Transmitter Electrical Characteristics (continued)

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.1 V)	$\|V_{OD}\|$	352.0	550.0	797.5	mV	Equalization setting: 1.0×
		323.1	504.9	732.1		Equalization setting: 1.09×
		293.6	458.7	665.1		Equalization setting: 1.2×
		264.7	413.6	599.7		Equalization setting: 1.33×
		234.4	366.3	531.1		Equalization setting: 1.5×
		205.6	321.2	465.7		Equalization setting: 1.71×
		176.0	275.0	398.8		Equalization setting: 2.0×
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:

1. This does I not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn} - V_{\overline{SD\_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes lanes 0 & 1) or XMITEQ**EF** (for SerDes lanes 2 & 3) bit field of the MPC8569E SerDes control register:
   - The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD-DIFF-p-p}$ amplitude—power up default);
   - The LSB (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XV_{DD-Typ} = 1.0V and 1.1 V, no common mode offset variation, SerDes transmitter is terminated with 100-Ω differential load between SD_TX[*n*] and $\overline{SD\_TX}$[*n*].

may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes.The SerDes reference clock inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express, Serial RapidIO, and SGMII interface, respectively.

The following sections describe the SerDes reference clock requirements and provide application information.

2.9.2.1 SerDes Spread Spectrum Clock Source Recommendations

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are designed to work with spread spectrum clock for PCI Express protocol only with the spreading specification defined in Table 47. When using spread spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The spread spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread spectrum supported protocols. For example, if the spread spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII/SRIO due to the SerDes lane usage mapping option, spread spectrum clocking cannot be used at all.

Table 47. SerDes Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	–0.5	%	1

Note:

1. Only down spreading is allowed.

2.9.2.2 SerDes Reference Clock Receiver Characteristics

The following figure shows a receiver reference diagram of the SerDes reference clocks.

(RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A – B volts
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts

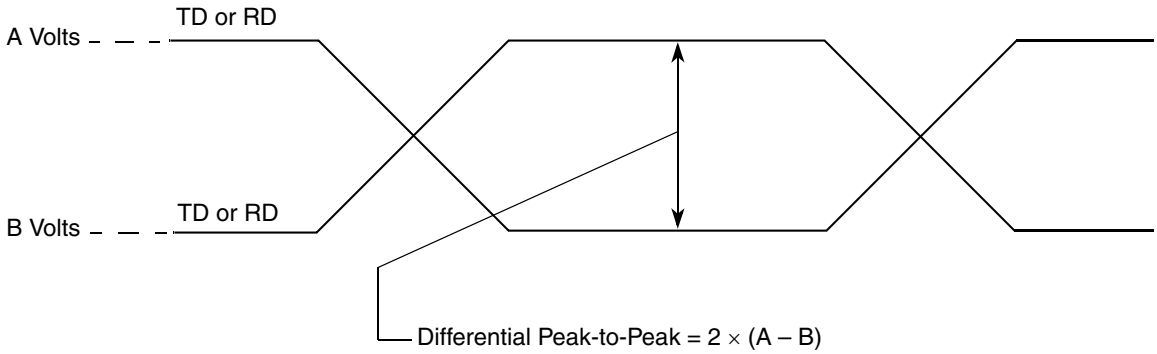


Figure 47. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.11.2 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- Pre-emphasis on the transmitter
- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

The following figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

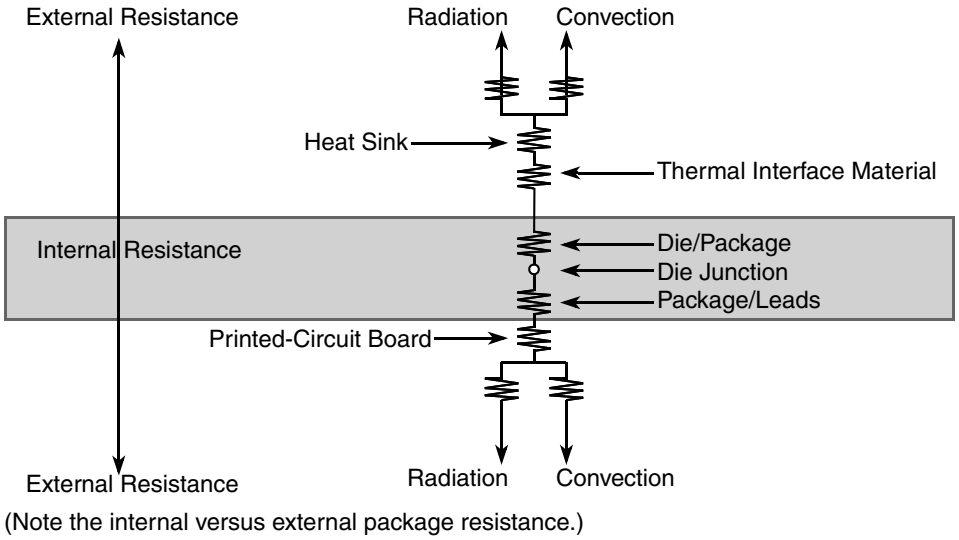


Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and the heat sink attach material (or thermal interface material), and to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 73).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.3.3 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the MPC8569E on-board temperature diode:

Operating range: 10 – 230 μA

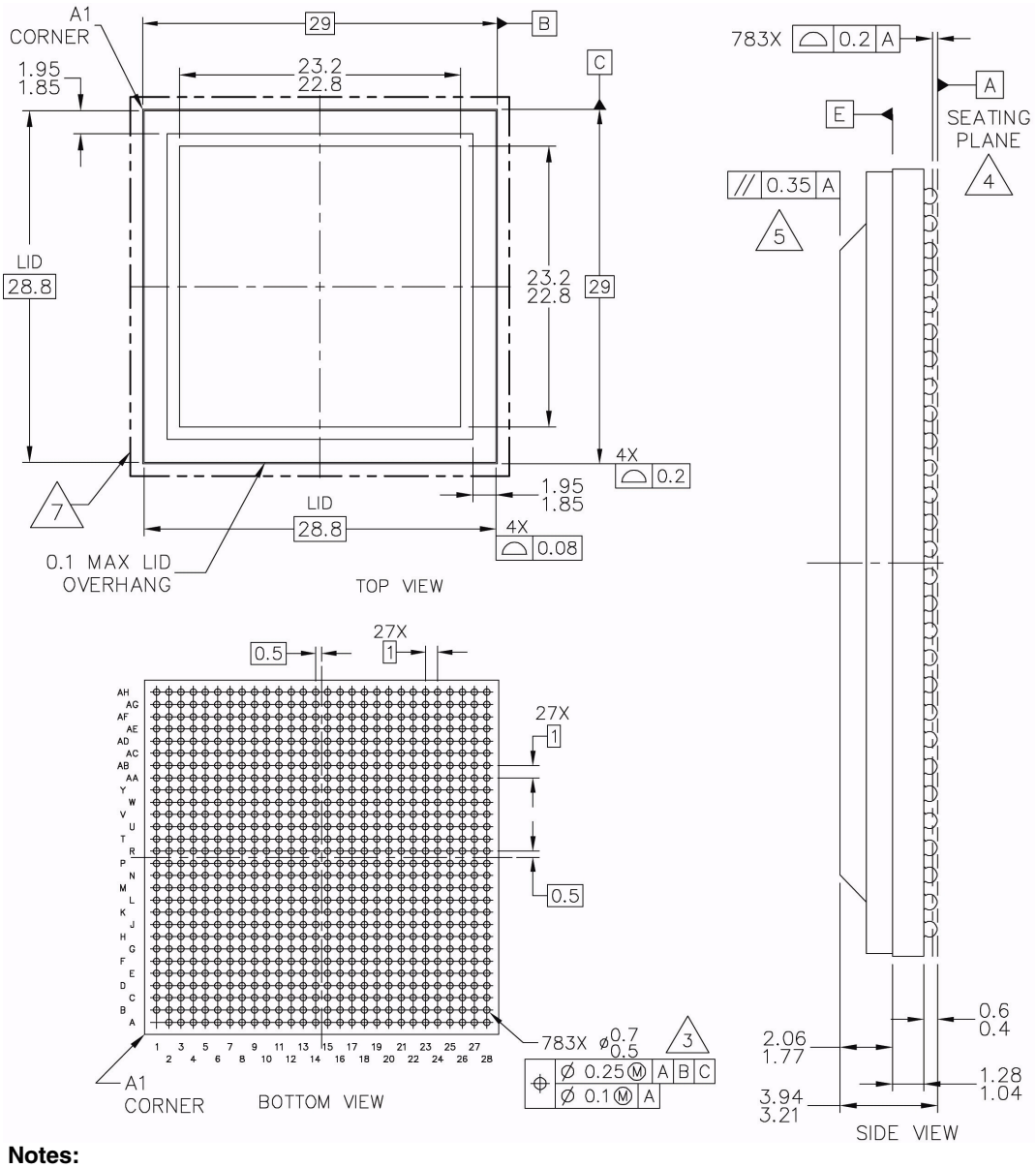
Ideality factor over 13.5 – 220 μA; n = 1.006 +/- 0.008

4 Package Description

The following section describes the detailed content and mechanical description of the package.

4.2 Mechanical Dimensions of the FC-PBGA with Full Lid

The following figure shows the mechanical dimensions and bottom surface nomenclature for the MPC8569E FC-PBGA package with full lid.



Notes:

[1]All dimensions are in millimeters.
[2]Dimensions and tolerances per ASME Y14.5M-1994.
[3]Maximum solder ball diameter measured parallel to datum A.
[4]Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
[5]Parallelism measurement shall exclude any effect of mark on top surface of package.
[6]All dimensions are symmetric across the package center lines unless dimensioned otherwise.
[7]29.2 mm maximum package assembly (lid and laminate) x and y.

Figure 75. MPC8569E FC-PBGA Package with Full Lid