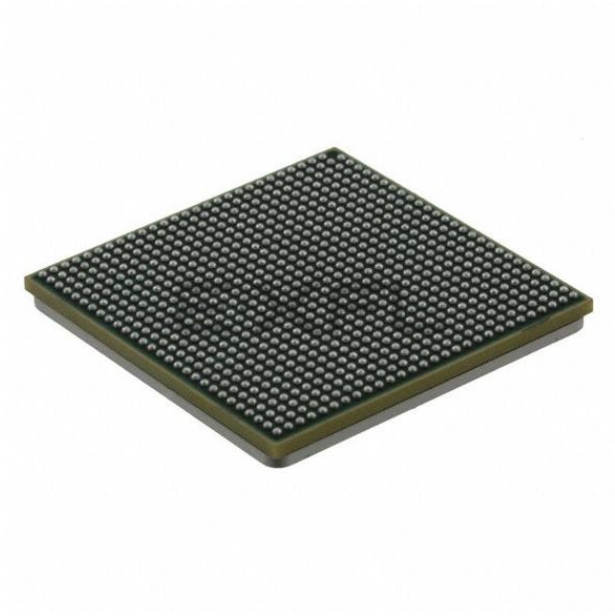

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569evtaunlb

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

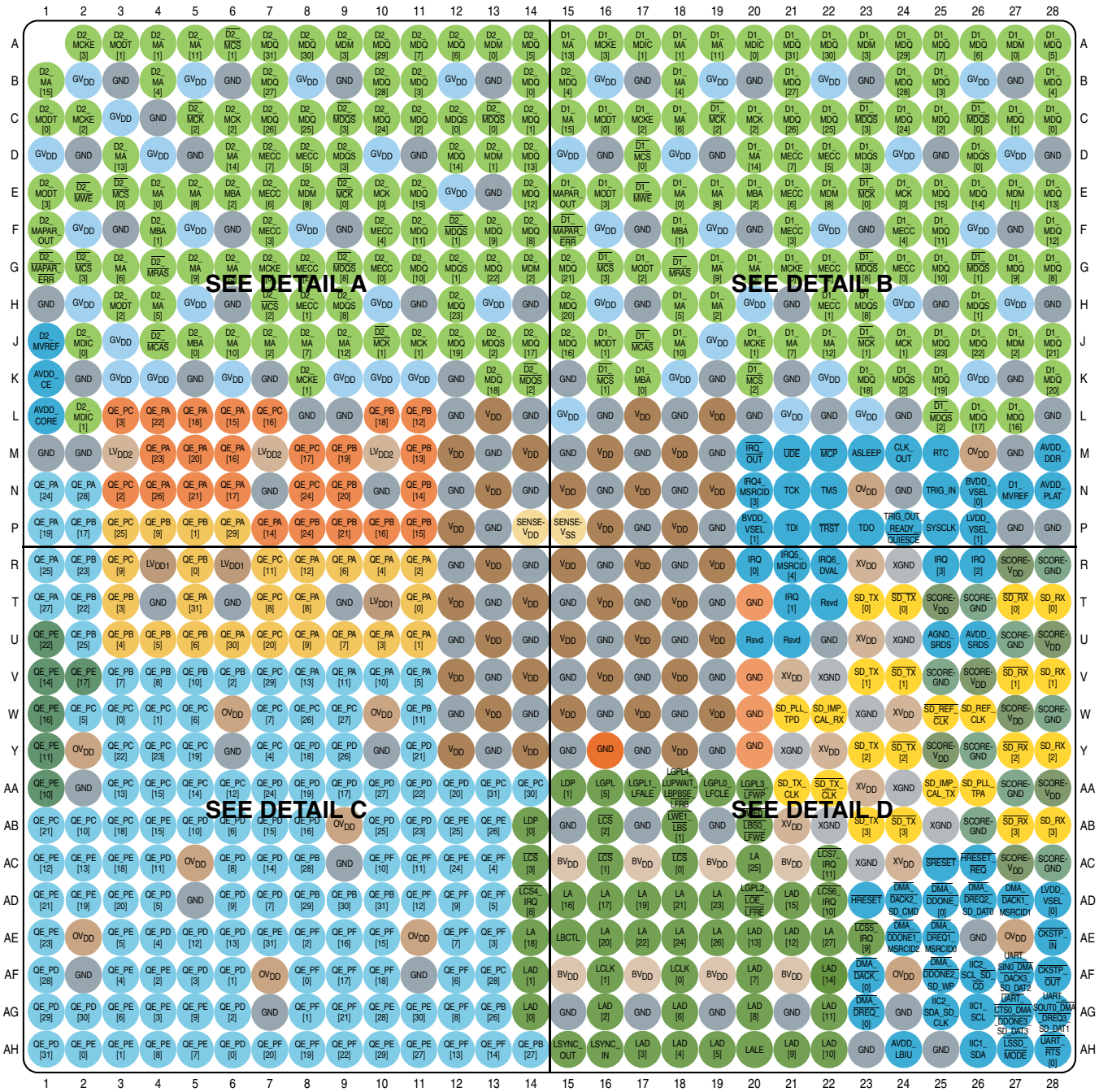
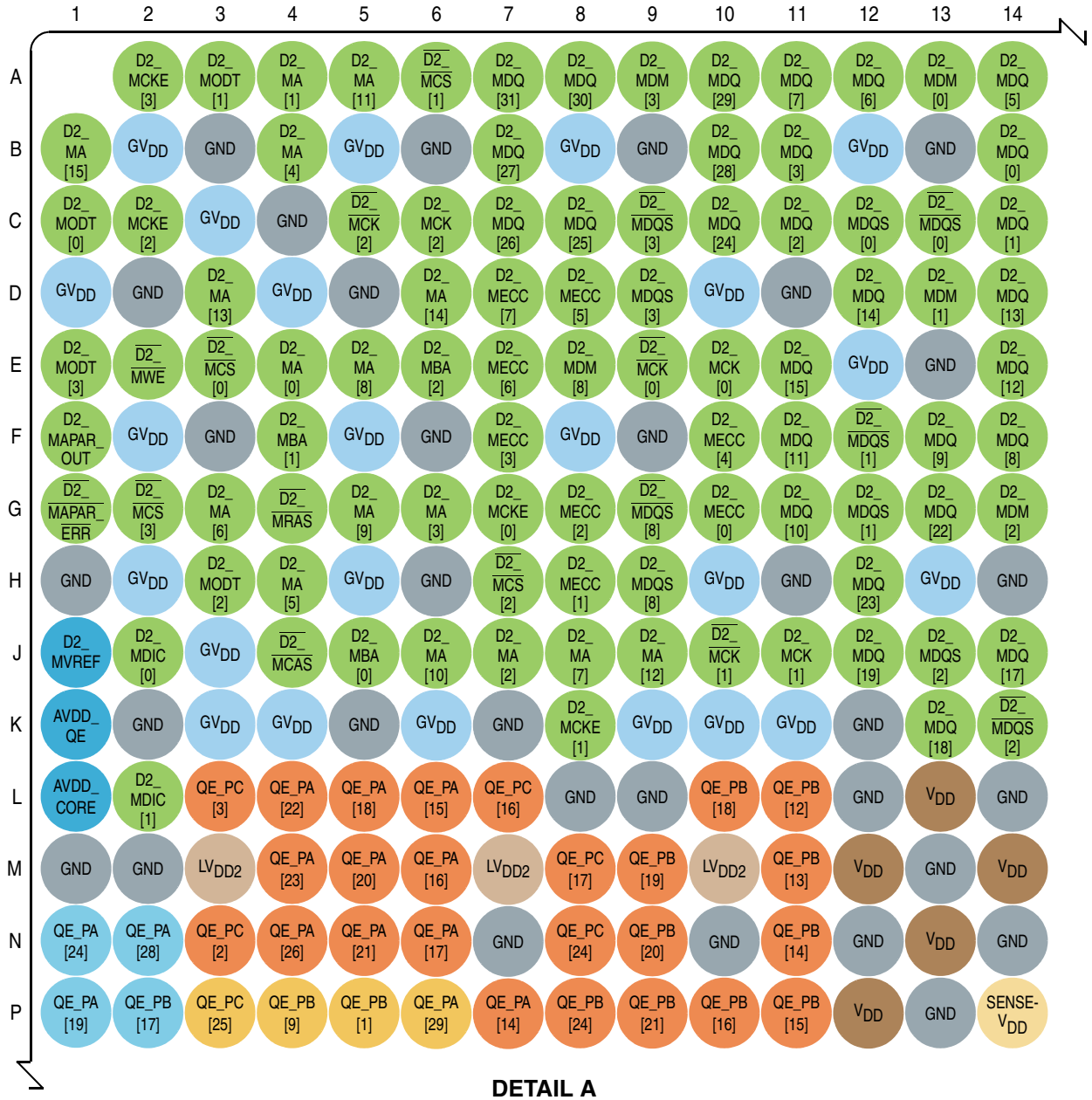


Figure 2. MPC8569E Top View Ballmap

The following figure provides detailed view A of the MPC8569E 783-pin BGA ball map diagram.



DETAIL A

Figure 3. MPC8569E Detail A Ball Map

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MCKE2	C17	O	GV_{DD}	—
D1_MCKE3	A16	O	GV_{DD}	—
$\overline{\text{D1\_MCS0}}$	D17	O	GV_{DD}	—
$\overline{\text{D1\_MCS1}}$	K16	O	GV_{DD}	—
$\overline{\text{D1\_MCS2}}$	K20	O	GV_{DD}	—
$\overline{\text{D1\_MCS3}}$	G16	O	GV_{DD}	—
D1_MDIC0	A20	I/O	GV_{DD}	27
D1_MDIC1	A17	I/O	GV_{DD}	27
D1_MDM0	A27	I/O	GV_{DD}	—
D1_MDM1	E27	I/O	GV_{DD}	—
D1_MDM2	J27	I/O	GV_{DD}	—
D1_MDM3	A23	I/O	GV_{DD}	—
D1_MDM8	E22	I/O	GV_{DD}	—
D1_MDQ0	C28	I/O	GV_{DD}	—
D1_MDQ1	C27	I/O	GV_{DD}	—
D1_MDQ2	C25	I/O	GV_{DD}	—
D1_MDQ3	B25	I/O	GV_{DD}	—
D1_MDQ4	B28	I/O	GV_{DD}	—
D1_MDQ5	A28	I/O	GV_{DD}	—
D1_MDQ6	A26	I/O	GV_{DD}	—
D1_MDQ7	A25	I/O	GV_{DD}	—
D1_MDQ8	G28	I/O	GV_{DD}	—
D1_MDQ9	G27	I/O	GV_{DD}	—
D1_MDQ10	G25	I/O	GV_{DD}	—
D1_MDQ11	F25	I/O	GV_{DD}	—
D1_MDQ12	F28	I/O	GV_{DD}	—
D1_MDQ13	E28	I/O	GV_{DD}	—
D1_MDQ14	E26	I/O	GV_{DD}	—
D1_MDQ15	E25	I/O	GV_{DD}	—
D1_MDQ16	L27	I/O	GV_{DD}	—
D1_MDQ17	L26	I/O	GV_{DD}	—
D1_MDQ18	K23	I/O	GV_{DD}	—
D1_MDQ19	K25	I/O	GV_{DD}	—
D1_MDQ20	K28	I/O	GV_{DD}	—
D1_MDQ21	J28	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
LAD12	AE21	I/O	BV_{DD}	23
LAD13	AE20	I/O	BV_{DD}	23
LAD14	AF22	I/O	BV_{DD}	23
LAD15	AD21	I/O	BV_{DD}	23
LALE	AH20	O	BV_{DD}	20
LBCTL	AE15	O	BV_{DD}	20
LCLK0	AF18	O	BV_{DD}	11
LCLK1	AF16	O	BV_{DD}	11
$\overline{\text{LCS0}}$	AC18	O	BV_{DD}	2
$\overline{\text{LCS1}}$	AC16	O	BV_{DD}	2
$\overline{\text{LCS2}}$	AB16	O	BV_{DD}	2
$\overline{\text{LCS3}}$	AC14	O	BV_{DD}	21
$\overline{\text{LCS4}}$/IRQ8	AD14	I/O	BV_{DD}	21
$\overline{\text{LCS5}}$/IRQ9	AE23	I/O	BV_{DD}	21
$\overline{\text{LCS6}}$/IRQ10	AD22	I/O	BV_{DD}	21
$\overline{\text{LCS7}}$/IRQ11	AC22	I/O	BV_{DD}	21
LDP0	AB14	I/O	BV_{DD}	—
LDP1	AA15	I/O	BV_{DD}	—
LGPL0/LFCLE	AA19	O	BV_{DD}	2
LGPL1/LFALE	AA17	O	BV_{DD}	2
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AD20	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	AA20	O	BV_{DD}	2
LGPL4/LUPWAIT/LBPBSE/$\overline{\text{LFRB}}$	AA18	I/O	BV_{DD}	29
LGPL5	AA16	O	BV_{DD}	2
LSYNC_IN	AH16	I	BV_{DD}	—
LSYNC_OUT	AH15	O	BV_{DD}	—
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$LFWE	AB20	O	BV_{DD}	11
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	AB18	O	BV_{DD}	24
I^2C				
IIC1_SDA	AH26	I/O	OV_{DD}	5, 28
IIC1_SCL	AG26	I/O	OV_{DD}	5, 28
IIC2_SDA/SD_CLK	AG25	I/O	OV_{DD}	3
IIC2_SCL/$\overline{\text{SD\_CD}}$	AF26	I/O	OV_{DD}	3
JTAG				
TCK	N21	I	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	P18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W19	1.0-V/1.1-V core power supply	V_{DD}	—

Table 8. MPC8569E Power Dissipation (continued)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	1333	533	800	667	1.1	65	5.7 W	1, 2
Thermal						105	7.9 W	1, 3
Maximum							8.6 W	1, 4

Note:

1. These values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running the Dhrystone benchmark, using the *nominal* process and *recommended* core voltage (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the maximum power measured while running the Dhrystone benchmark, using the *worst case* process and *recommended* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions that keeps the execution unit maximally busy and a typical workload on platform interfaces, using the *worst case* process and *nominal* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
5. This table includes power numbers for the V_{DD}, AV_{DD}_n, and ScoreVDD rails.

2.3 Input Clocks

The following table provides the system clock (SYSCLK) DC specifications.

Table 9. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	10.5	11.5	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rate and in DDR3 mode to 667 and 800 MHz data rate.
7. DDR3 only
8. DDR2 only

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

The following figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

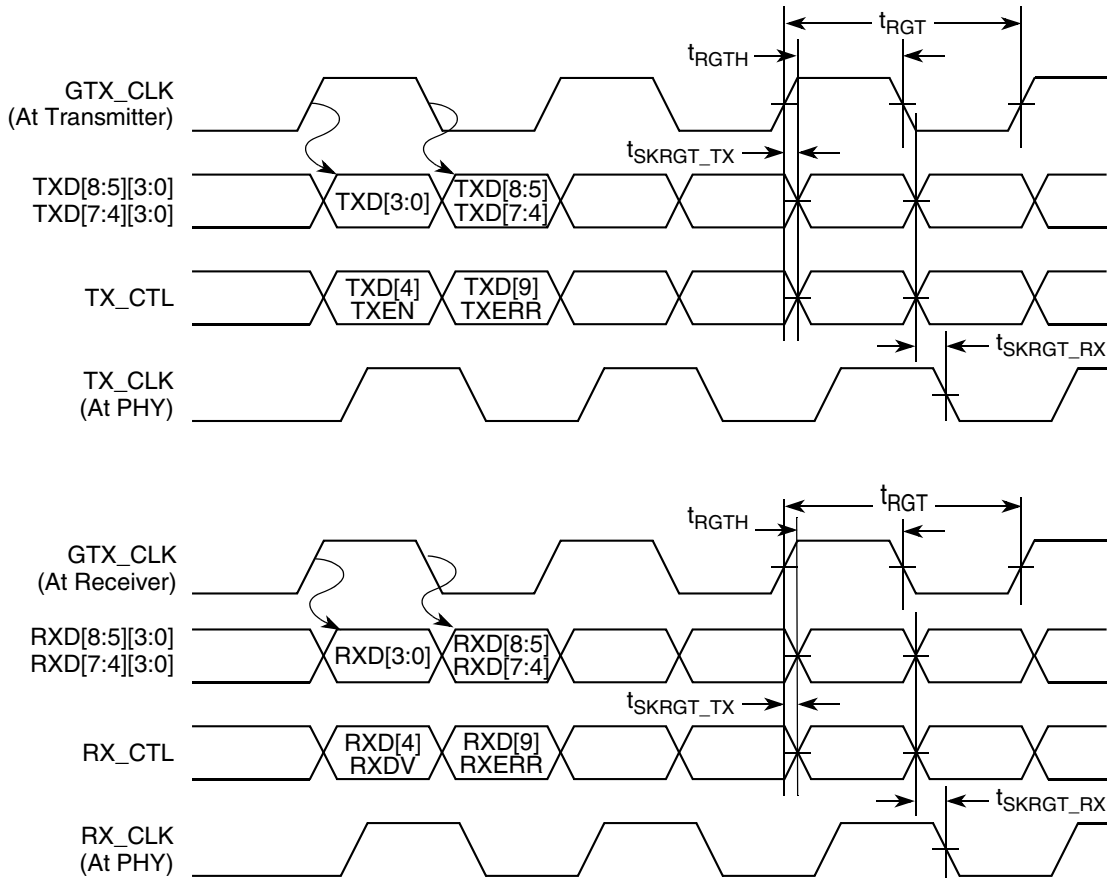


Figure 26. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.6.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of MPC8569E as shown in Figure 27, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 45.

2.6.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.6.4.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.9.2.3, “DC Level Requirement for SerDes Reference Clocks.”

2.6.5 QUICC Engine Block IEEE 1588 Electrical Characteristics

2.6.5.1 QUICC Engine Block IEEE 1588 DC Specifications

The following table shows the QUICC Engine block IEEE 1588 DC specifications when operating from a 3.3 V supply.

Table 40. QUICC Engine Block IEEE 1588 DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = OV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbols referenced in Table 2 and Table 3.

2.6.5.2 QUICC Engine Block IEEE 1588 AC Specifications

The following table provides the QUICC Engine block IEEE 1588 AC timing specifications.

Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 7$	ns	1, 3
QE_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	5
QE_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	5
Rise time QE_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	5
Fall time QE_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	5
QE_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
QE_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
QE_1588_PPS_OUT	$t_{T1588OV}$	0.5	—	4.0	ns	—

The following figure shows the data and command input AC timing diagram.

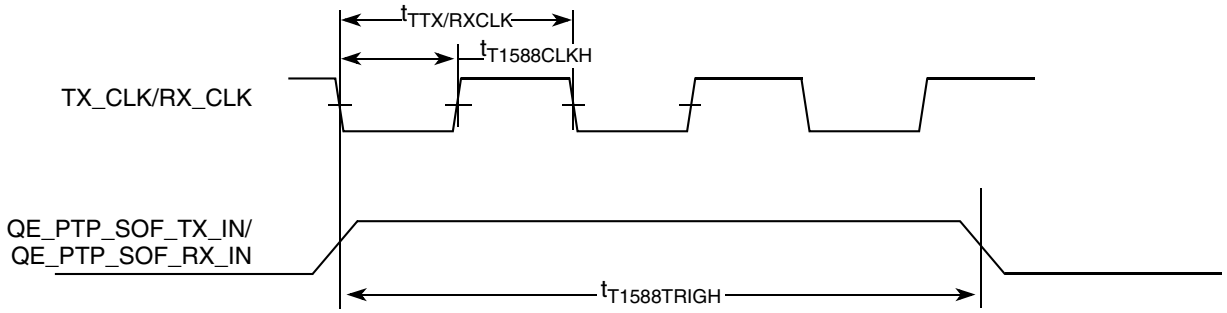


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

2.8 HDLC, BISYNC, Transparent, and Synchronous UART Interfaces

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART interfaces of the MPC8569E.

2.8.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the HDLC, BISYNC, Transparent, and synchronous UART interfaces.

Table 44. HDLC, BISYNC, and Transparent DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.8.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

The following table provides the input and output AC timing specifications for the HDLC, BISYNC, and Transparent protocols.

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	8.4	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	5.5	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	8	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns	—

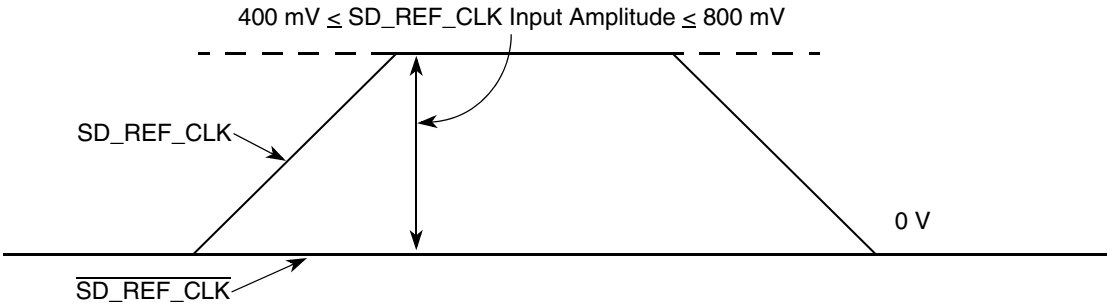


Figure 42. Single-Ended Reference Clock Input DC Requirements

2.9.2.4 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express, SGMII, and Serial RapidIO SerDes reference clocks to be guaranteed by the customer's application design.

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2, 7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3, 7

Table 57. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD} (max))	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *MPC8569E PowerQUICC III Integrated Processor Family Reference Manual* for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.12.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface.

Table 58. I²C AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

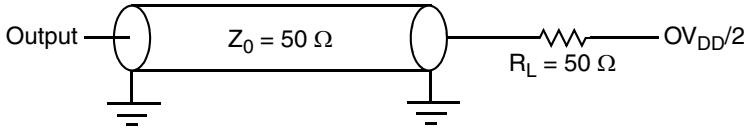


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

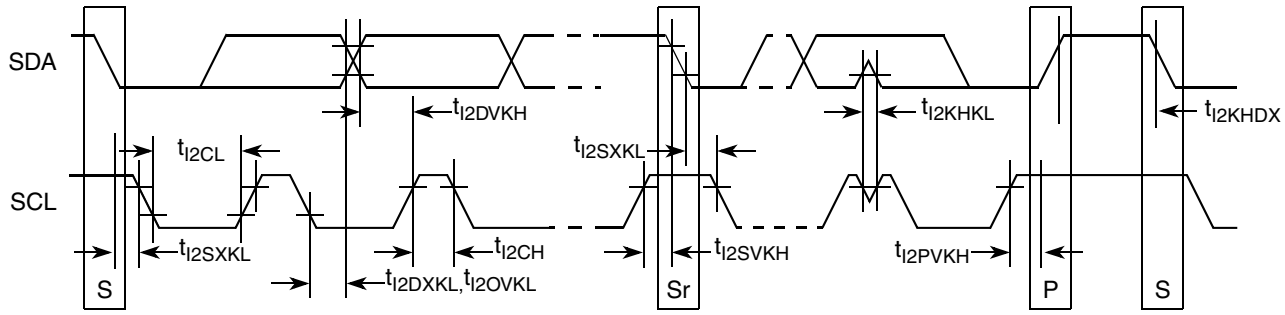


Figure 50. I²C Bus AC Timing Diagram

2.14 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 61. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

Table 62. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	4
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—

2.15.2.2 Enhanced Local Bus AC Timing Specifications for PLL Enable Mode

For PLL enable mode, all timings are relative to the rising edge of LSYNC_IN.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3 V, 2.5 V and 1.8 V for PLL enable mode.

Table 66. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V 2.5 V and 1.8 V) —PLL Enabled Mode

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	7.5	12	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	5
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	680	ps	2
Input setup	t_{LBIVKH}	2	—	ns	—
Input hold	t_{LBIXKH}	1.0	—	ns	—
Output delay (Except LALE)	t_{LBKHOV}	—	3.8	ns	—
Output hold (Except LALE)	t_{LBKHOX}	0.6	—	ns	—
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 0.475 ns (LBCR[AHD]=0) ½ – 0.475 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle. The eLBC controller clock refers to the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

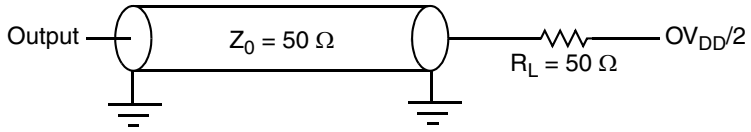
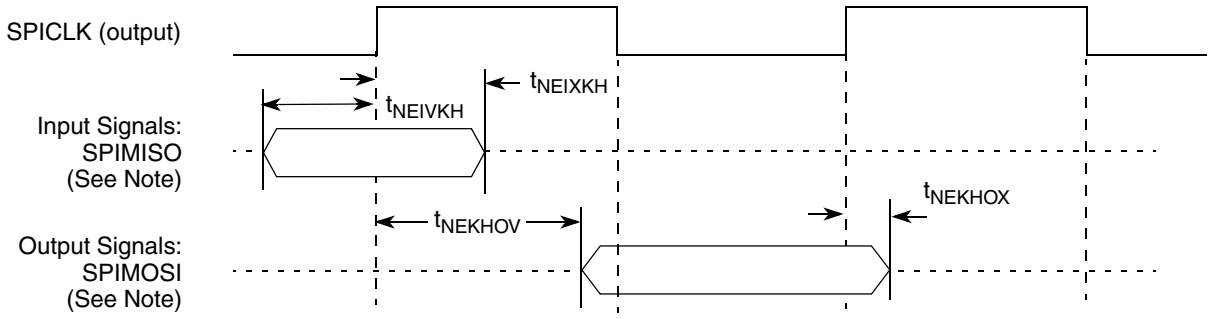


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

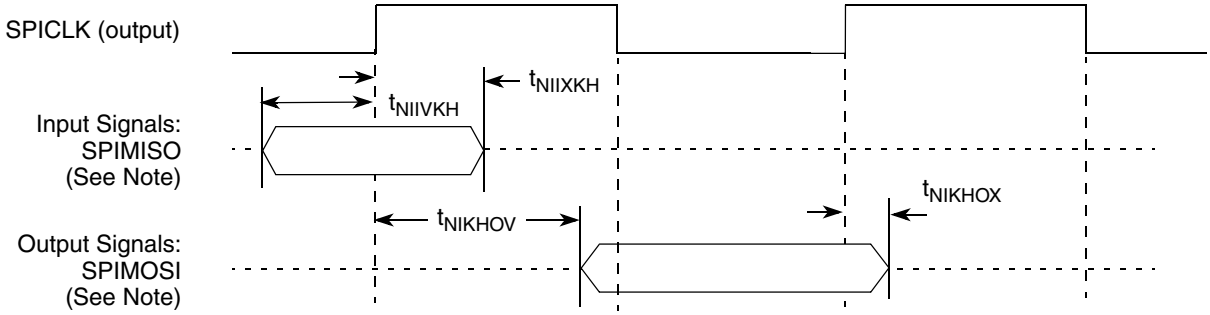
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

The following figure provide the AC test load for the USB.

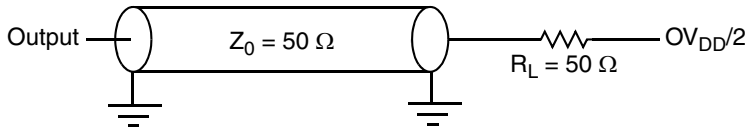


Figure 69. USB AC Test Load

2.22 UTOPIA/POS Interface

This section describes the DC and AC electrical specifications for the UTOPIA interface.

2.22.1 UTOPIA/POS DC Electrical Characteristics

The following table provides the DC electrical characteristics.

Table 80. UTOPIA/POS DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.22.2 UTOPIA/POS AC Timing Specifications

The following table provides the UTOPIA/POS input and output AC timing specifications.

Table 81. UTOPIA/POS AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA/POS outputs—Internal clock delay	t_{UIKHOV}	0	8.0	ns
UTOPIA/POS outputs—External clock delay	t_{UEKHOV}	1.0	10.0	ns
UTOPIA/POS outputs—Internal clock high Impedance	t_{UIKHOX}	0	8.0	ns
UTOPIA/POS outputs—External clock high impedance	t_{UEKHOX}	1.0	10.0	ns
UTOPIA/POS inputs—Internal clock input setup time	t_{UIIVKH}	6.4	—	ns

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