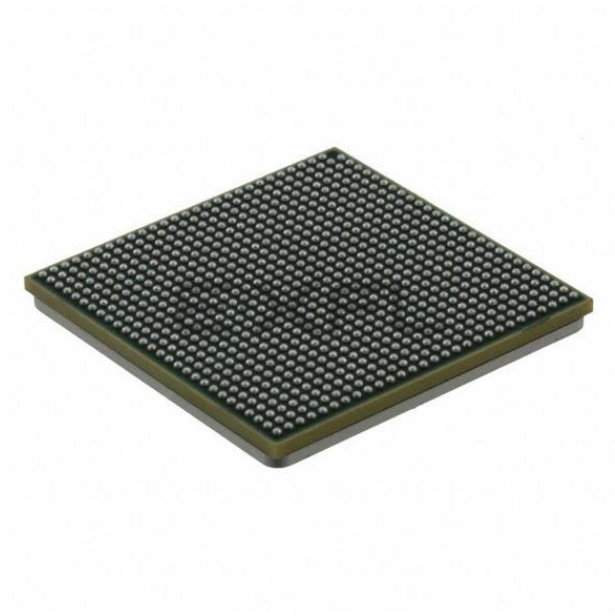

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569vjankgb

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDIC0	J2	I/O	GV_{DD}	27
D2_MDIC1	L2	I/O	GV_{DD}	27
D2_MDM0/D1_MDM4	A13	I/O	GV_{DD}	—
D2_MDM1/D1_MDM5	D13	I/O	GV_{DD}	—
D2_MDM2/D1_MDM6	G14	I/O	GV_{DD}	—
D2_MDM3/D1_MDM7	A9	I/O	GV_{DD}	—
D2_MDM8	E8	I/O	GV_{DD}	—
D2_MDQ0/D1_MDQ32	B14	I/O	GV_{DD}	—
D2_MDQ1/D1_MDQ33	C14	I/O	GV_{DD}	—
D2_MDQ2/D1_MDQ34	C11	I/O	GV_{DD}	—
D2_MDQ3/D1_MDQ35	B11	I/O	GV_{DD}	—
D2_MDQ4/D1_MDQ36	B15	I/O	GV_{DD}	—
D2_MDQ5/D1_MDQ37	A14	I/O	GV_{DD}	—
D2_MDQ6/D1_MDQ38	A12	I/O	GV_{DD}	—
D2_MDQ7/D1_MDQ39	A11	I/O	GV_{DD}	—
D2_MDQ8/D1_MDQ40	F14	I/O	GV_{DD}	—
D2_MDQ9/D1_MDQ41	F13	I/O	GV_{DD}	—
D2_MDQ10/D1_MDQ42	G11	I/O	GV_{DD}	—
D2_MDQ11/D1_MDQ43	F11	I/O	GV_{DD}	—
D2_MDQ12/D1_MDQ44	E14	I/O	GV_{DD}	—
D2_MDQ13/D1_MDQ45	D14	I/O	GV_{DD}	—
D2_MDQ14/D1_MDQ46	D12	I/O	GV_{DD}	—
D2_MDQ15/D1_MDQ47	E11	I/O	GV_{DD}	—
D2_MDQ16/D1_MDQ48	J15	I/O	GV_{DD}	—
D2_MDQ17/D1_MDQ49	J14	I/O	GV_{DD}	—
D2_MDQ18/D1_MDQ50	K13	I/O	GV_{DD}	—
D2_MDQ19/D1_MDQ51	J12	I/O	GV_{DD}	—
D2_MDQ20/D1_MDQ52	H15	I/O	GV_{DD}	—
D2_MDQ21/D1_MDQ53	G15	I/O	GV_{DD}	—
D2_MDQ22/D1_MDQ54	G13	I/O	GV_{DD}	—
D2_MDQ23/D1_MDQ55	H12	I/O	GV_{DD}	—
D2_MDQ24/D1_MDQ56	C10	I/O	GV_{DD}	—
D2_MDQ25/D1_MDQ57	C8	I/O	GV_{DD}	—
D2_MDQ26/D1_MDQ58	C7	I/O	GV_{DD}	—
D2_MDQ27/D1_MDQ59	B7	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ28/D1_MDQ60	B10	I/O	GV_{DD}	—
D2_MDQ29/D1_MDQ61	A10	I/O	GV_{DD}	—
D2_MDQ30/D1_MDQ62	A8	I/O	GV_{DD}	—
D2_MDQ31/D1_MDQ63	A7	I/O	GV_{DD}	—
D2_MDQS0/D1_MDQS4	C12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$	C13	I/O	GV_{DD}	—
D2_MDQS1/D1_MDQS5	G12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$	F12	I/O	GV_{DD}	—
D2_MDQS2/D1_MDQS6	J13	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$	K14	I/O	GV_{DD}	—
D2_MDQS3/D1_MDQS7	D9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$	C9	I/O	GV_{DD}	—
D2_MDQS8	H9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	G9	I/O	GV_{DD}	—
D2_MECC0	G10	I/O	GV_{DD}	—
D2_MECC1	H8	I/O	GV_{DD}	—
D2_MECC2	G8	I/O	GV_{DD}	—
D2_MECC3	F7	I/O	GV_{DD}	—
D2_MECC4	F10	I/O	GV_{DD}	—
D2_MECC5	D8	I/O	GV_{DD}	—
D2_MECC6	E7	I/O	GV_{DD}	—
D2_MECC7	D7	I/O	GV_{DD}	—
D2_MODT0	C1	O	GV_{DD}	—
D2_MODT1	A3	O	GV_{DD}	—
D2_MODT2	H3	O	GV_{DD}	—
D2_MODT3	E1	O	GV_{DD}	—
D2_MAPAR_OUT	F1	O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	G1	I	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	G4	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	E2	O	GV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK0}}$	AF23	O	OV_{DD}	2
$\overline{\text{DMA\_DACK1}}$/MSRCID1	AD27	O	OV_{DD}	11
$\overline{\text{DMA\_DACK2}}$/SD_CMD	AD24	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE0}}$	AD25	O	OV_{DD}	2

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Power Management				
ASLEEP	M23	O	OV_{DD}	11
Thermal Management				
THERM0	U21	—	Internal temperature diode cathode	32
THERM1	U20	—	Internal temperature diode anode	32
Reserved	T22	—	—	9
Analog				
D1_MVREF	N27	Reference voltage for DDR	MV_{REF}	—
D2_MVREF	J1			—
Power and Ground				
V_{DD}	L13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P16	1.0-V/1.1-V core power supply	V_{DD}	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

Table 5. RESET Initialization Timing Specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum rise/fall time of $\overline{\text{HRESET}}$	—	1	SYSCLK	5
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLK	4
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	2	—	SYSCLK	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLK	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	8	—	SYSCLK	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLK	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in *AN4232 MPC8569E PowerQUICC III Design Checklist*.
4. SYSCLK is the primary clock input for the MPC8569E.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following table provides the PLL lock times.

Table 6. PLL Lock Times

Parameter	Min	Max	Unit
Core PLL lock time	—	100	µs
Platform PLL lock time	—	100	µs
QUICC Engine block PLL lock time	—	100	µs
DDR PLL lock times	—	100	µs

Table 8. MPC8569E Power Dissipation (continued)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	1333	533	800	667	1.1	65	5.7 W	1, 2
Thermal						105	7.9 W	1, 3
Maximum							8.6 W	1, 4

Note:

1. These values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running the Dhrystone benchmark, using the *nominal* process and *recommended* core voltage (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the maximum power measured while running the Dhrystone benchmark, using the *worst case* process and *recommended* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions that keeps the execution unit maximally busy and a typical workload on platform interfaces, using the *worst case* process and *nominal* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
5. This table includes power numbers for the V_{DD}, AV_{DD}_n, and ScoreVDD rails.

2.3 Input Clocks

The following table provides the system clock (SYSCLK) DC specifications.

Table 9. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	10.5	11.5	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following figure provides the AC test load for the DDR2 and DDR3 controller bus.

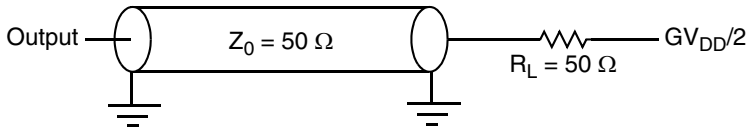


Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.5 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8569E.

2.5.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.5.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	—	3

Notes:

1. f_{CCB} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.6.3.6 TBI Single-Clock Mode AC Specifications

The following table shows the TBI single-clock mode receive AC timing specifications.

Table 34. TBI Single-Clock Mode Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	1
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	2
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	2
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	—	ns	2
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	—	ns	2
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the TBI single-clock mode receive AC timing diagram.

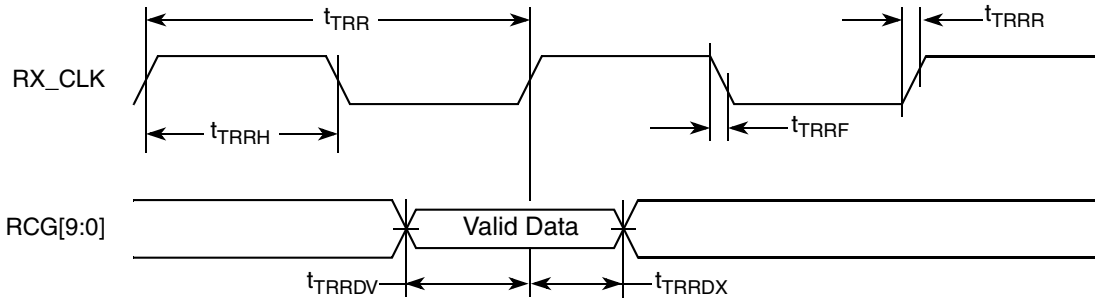


Figure 25. TBI Single-Clock Mode Receive AC Timing Diagram

2.6.3.7 RGMII and RTBI AC Timing Specifications

The following table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.2	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4, 6

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.6.4.1.3 SGMII DC Receiver Electrical Characteristics

The following table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 37. SGMII DC Receiver Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 001	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 100		175	—			
Loss of signal threshold	LSTS = 001	V_{LOS}	30	—	100	mV	3, 4
	LSTS = 100		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See Section 2.10.2, "PCI Express DC Physical Layer Specifications," and Section 2.10.3, "PCI Express AC Physical Layer Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**2** or LSTS**3** bit field of the MPC8569E's SerDes control register SRDSCR4.

2.6.4.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.6.4.2.1 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, "AC Requirements for SerDes Reference Clocks."

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

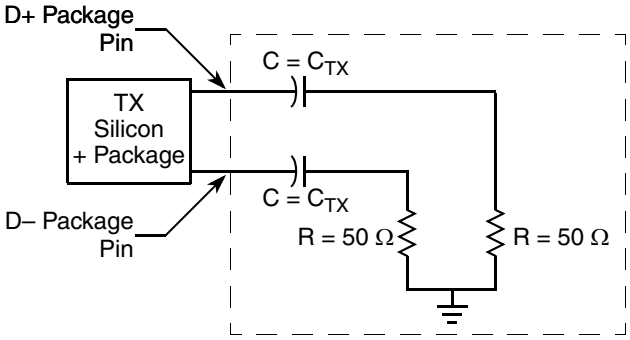
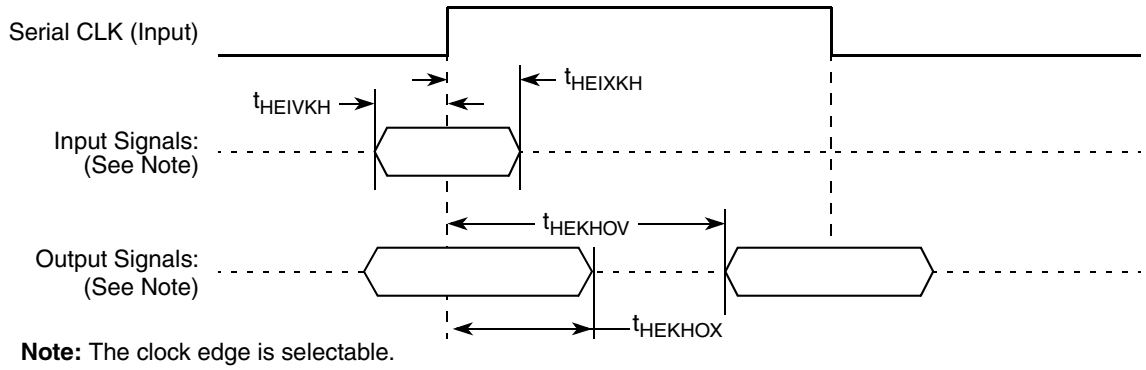


Figure 29. SGMII AC Test/Measurement Load

Figure 36 and Figure 37 represent the AC timing from Table 45 and Table 46. Note that although the specifications generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also note that the clock edge is selectable.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 36. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.

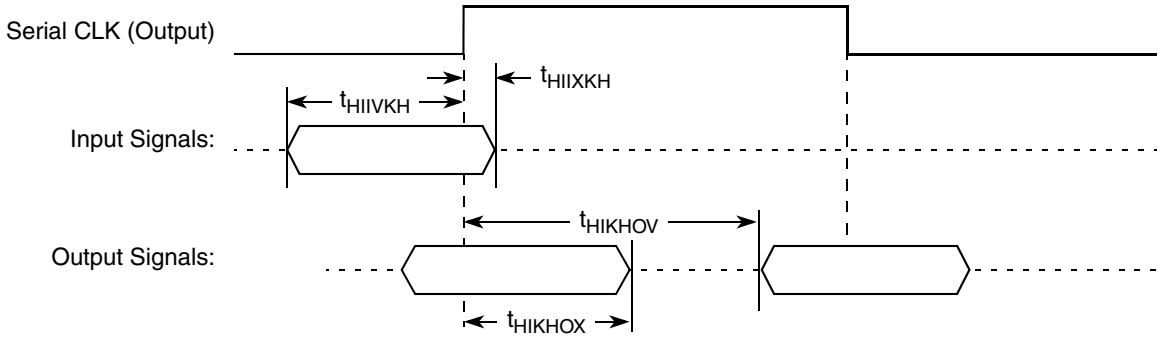


Figure 37. AC Timing (Internal Clock) Diagram

2.9 High-Speed SerDes Interfaces (HSSI)

The MPC859E features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications.The SerDes interface can be used for PCI Express and/or Serial RapidIO and/or SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The below figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

— For external DC-coupled connection, as described in Section 2.9.2.2, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. The following figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

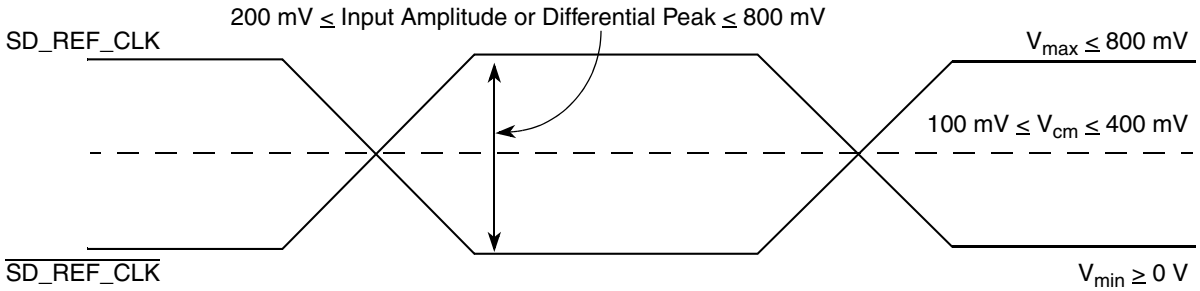


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SCOREGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SCOREGND). The following figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

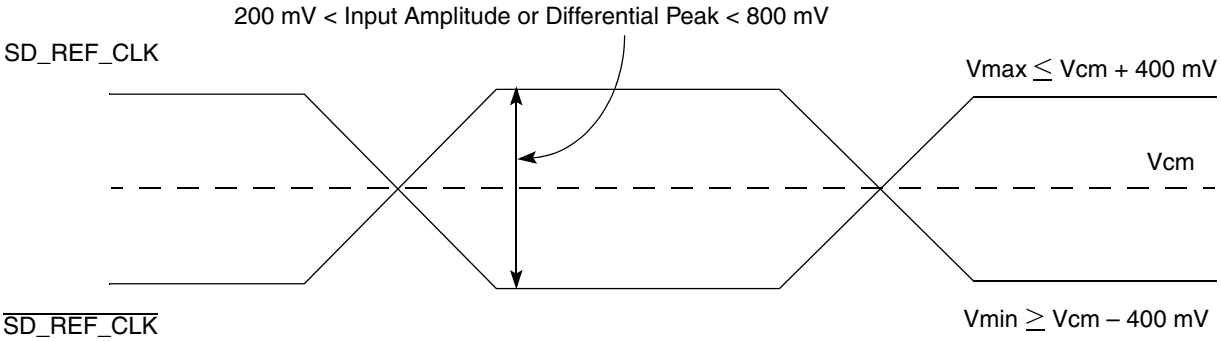


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-ended mode
  - — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. Measured at the package pins of the receiver.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.10.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.10.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum TX eye width	T_{TX-EYE}	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

2.11.3 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.11.3.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clocks of the SRIO interface are described in Section 2.9.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.11.3.2 DC Serial RapidIO Timing Transmitter Specifications

The LP-serial transmitter electrical and timing specifications are given in the following sections.

The differential return loss, S11, of the transmitter in each case are better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

The following table defines the serial RapidIO transmitter DC specifications.

Table 53. SRIO Transmitter DC Timing Specifications—1.25, 2.5, and 3.125 GBauds

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

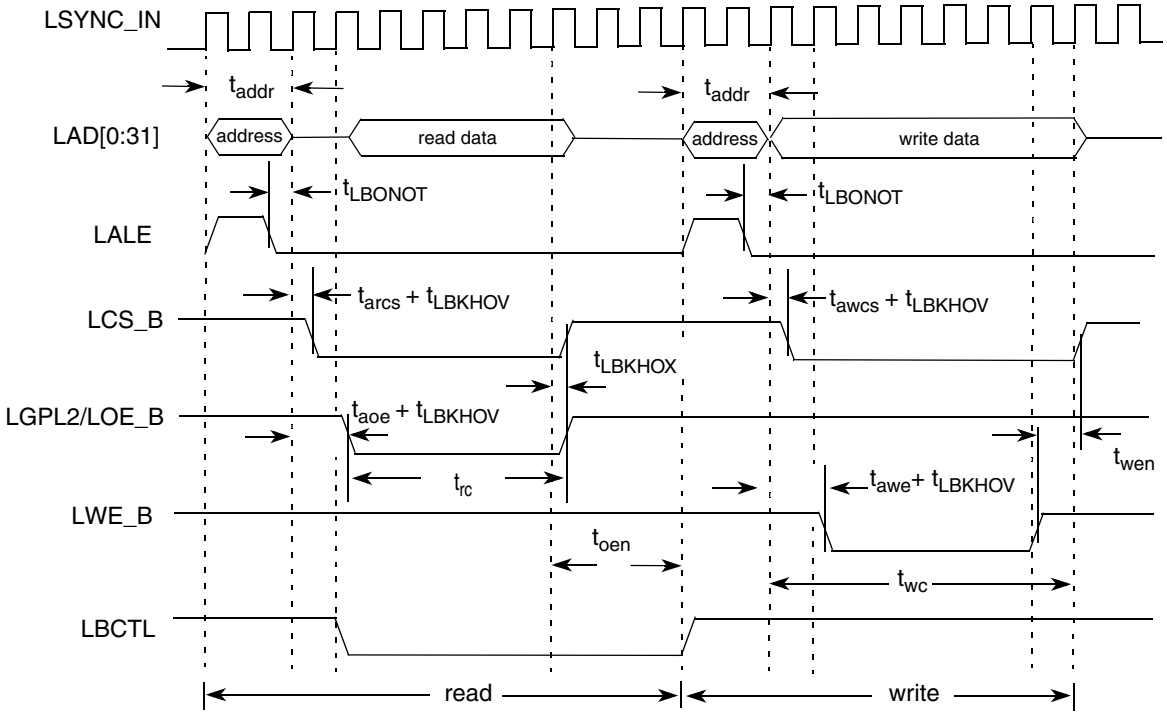
2.11.3.3 DC Serial RapidIO Receiver Specifications

The LP-serial receiver electrical and timing specifications are given in the following sections.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to reference manual.

Figure 58. GPCM Output Timing Diagram (PLL Enabled)

2.15.2.3 Enhanced Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LUPWAIT/LFRB are relative to the rising edge of LCLKs. LUPWAIT/LFRB are relative to the falling edge of LCLKs.

The following figure shows the UTOPIA/POS timing with internal clock.

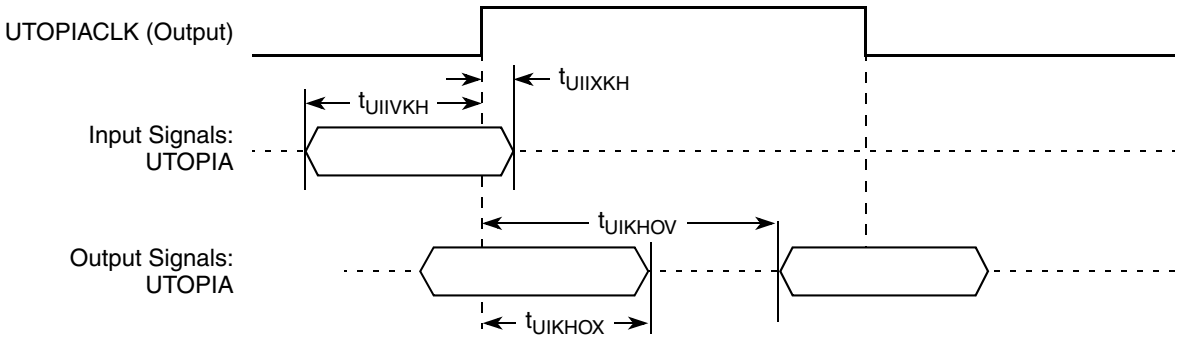


Figure 72. UTOPIA/POS AC Timing (Internal Clock) Diagram

3 Thermal

This section describes the thermal specifications of the MPC8569E.

3.1 Thermal Characteristics

The following table provides the package thermal characteristics of the MPC8569E.

Table 82. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	16	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	5	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	1.0	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.2 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.