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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569vjaunlb

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PE29	AH10	I/O	OV_{DD}	19
QE_PE30	AG11	I/O	OV_{DD}	—
QE_PE31	AE7	I/O	OV_{DD}	—
QE_PF0	AF8	I/O	OV_{DD}	—
QE_PF1	AG8	I/O	OV_{DD}	—
QE_PF2	AE8	I/O	OV_{DD}	—
QE_PF3	AE13	I/O	OV_{DD}	—
QE_PF4	AC13	I/O	OV_{DD}	—
QE_PF5	AD13	I/O	OV_{DD}	—
QE_PF6	AF12	I/O	OV_{DD}	—
QE_PF7	AE12	I/O	OV_{DD}	—
QE_PF8	AG12	I/O	OV_{DD}	—
QE_PF9	AD12	I/O	OV_{DD}	2
QE_PF10	AC10	I/O	OV_{DD}	2
QE_PF11	AC11	I/O	OV_{DD}	2
QE_PF12	AD11	I/O	OV_{DD}	—
QE_PF13	AH12	I/O	OV_{DD}	11
QE_PF14	AH13	I/O	OV_{DD}	2
QE_PF15	AE10	I/O	OV_{DD}	—
QE_PF16	AE9	I/O	OV_{DD}	—
QE_PF17	AF9	I/O	OV_{DD}	—
QE_PF18	AF10	I/O	OV_{DD}	—
QE_PF19	AH8	I/O	OV_{DD}	—
QE_PF20	AH7	I/O	OV_{DD}	—
QE_PF21	AG9	I/O	OV_{DD}	—
QE_PF22	AH9	I/O	OV_{DD}	—
SerDes				
SD_IMP_CAL_RX	W22	I	—	7
SD_IMP_CAL_TX	AA25	I	—	17
SD_PLL_TPA	AA26	O	AV_{DD}_SRDS	8
SD_PLL_TPD	W21	O	XV_{DD}	8
SD_REF_CLK	W26	I	ScoreVDD	—
$\overline{\text{SD\_REF\_CLK}}$	W25	I	ScoreVDD	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	AF11	—	—	—
GND	AF2	—	—	—
GND	AG15	—	—	—
GND	AG17	—	—	—
GND	AG19	—	—	—
GND	AG21	—	—	—
GND	AG24	—	—	—
GND	AG7	—	—	—
GND	AH23	—	—	—
GND	AH25	—	—	—
GND	B13	—	—	—
GND	B17	—	—	—
GND	B20	—	—	—
GND	B23	—	—	—
GND	B27	—	—	—
GND	B3	—	—	—
GND	B6	—	—	—
GND	B9	—	—	—
GND	C4	—	—	—
GND	D11	—	—	—
GND	D16	—	—	—
GND	D19	—	—	—
GND	D2	—	—	—
GND	D25	—	—	—
GND	D28	—	—	—
GND	D5	—	—	—
GND	E13	—	—	—
GND	F17	—	—	—
GND	F20	—	—	—
GND	F23	—	—	—
GND	F27	—	—	—
GND	F3	—	—	—
GND	F6	—	—	—
GND	F9	—	—	—
GND	H1	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	Y13	—	—	—
GND	Y15	—	—	—
GND	Y16	—	—	—
GND	Y17	—	—	—
GND	Y19	—	—	—
GND	V20	—	—	—
GND	T20	—	—	—
GND	W20	—	—	—
GND	Y20	—	—	—
SENSEVSS	P15	Ground sense	—	13
SCOREGND	AA27	SerDes Core Logic GND	—	—
SCOREGND	AB26	SerDes Core Logic GND	—	—
SCOREGND	AC28	SerDes Core Logic GND	—	—
SCOREGND	R28	SerDes Core Logic GND	—	—
SCOREGND	T26	SerDes Core Logic GND	—	—
SCOREGND	U27	SerDes Core Logic GND	—	—
SCOREGND	V25	SerDes Core Logic GND	—	—
SCOREGND	W28	SerDes Core Logic GND	—	—
SCOREGND	Y26	SerDes Core Logic GND	—	—
XGND	AA24	SerDes Transceiver Pad GND	—	—
XGND	AB22	SerDes Transceiver Pad GND	—	—
XGND	AB25	SerDes Transceiver Pad GND	—	—
XGND	AC23	SerDes Transceiver Pad GND	—	—
XGND	R24	SerDes Transceiver Pad GND	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to OV_{DD}.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Range	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD}_CORE AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	ScoreVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR2 and DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	2
QUICC Engine block Ethernet interface I/O voltage	$LV_{DD}1$	–0.3 to 3.63 –0.3 to 2.75	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Range	Unit	Notes
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	–0.3 to 3.63 –0.3 to 2.75	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Ethernet signals	LV_{IN}	–0.3 to ($LV_{DD}n$ + 0.3)	V	3
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
PLL supply voltage	AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	1.0 V ± 30 mV 1.1 V ± 33 mV	V	2

2.1.1.2 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal	18 (full strength mode) 35 (half strength mode)	GV_{DD} = 1.8 V	1
DDR3 signal	20 (full strength mode) 40 (half strength mode)	GV_{DD} = 1.5 V	1
DUART, EPIC, I^2C, JTAG, system control	45	OV_{DD} = 3.3 V	—

Note:

1. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_J = 105°C and at GV_{DD} (min). Refer to the MPC8569 reference manual for the DDR impedance programming procedure through the DDR control driver register 1 (DDRCDR_1).

2.1.2 Power Sequencing

The MPC8569E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $LV_{DD}n$, OV_{DD}, ScoreVDD, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

While V_{DD} is ramping, current may be supplied from V_{DD} through the MPC8569E to GV_{DD}. Nevertheless, GV_{DD} from an external supply should follow the sequencing described above.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

2.1.3 RESET Initialization

This section describes the AC electrical specifications for the RESET timing requirements of the MPC8569E. The following table describes the specifications for the RESET initialization timing.

Table 5. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	10	—	SYSCLK	1, 2
Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion	25	—	ns	3

2.3.2 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the core complex bus clock (CCB_clk). The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB_clk. That is, minimum clock high time is $2 \times t_{CCB\_clk}$, and minimum clock low time is $2 \times t_{CCB\_clk}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.3.3 Gigabit Ethernet Reference Clock Timing

The following table provides the gigabit Ethernet reference clock (TX_CLK) AC timing specifications.

Table 12. TX_CLK[3,4] AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV / 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
TX_CLK frequency	t_{G125}	—	125	—	MHz	—
TX_CLK cycle time	t_{G125}	—	8	—	ns	—
TX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1, 5
TX_CLK duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 5
TX_CLK jitter	—	—	—	± 150	ps	2, 5

Notes:

1. Rise and fall times for TX_CLK are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V, and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. TX_CLK is used to generate the GTX clock for the UEC transmitter with 2% degradation. The TX_CLK duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the UEC GTX_CLK. See Section 2.6.3.7, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Gigabit transmit 125-MHz source. This signal must be generated externally with a crystal or oscillator, or is sometimes provided by the PHY. TX_CLK is a 125-MHz input into the UCC Ethernet Controller and is used to generate all 125-MHz related signals and clocks in the following modes: GMII, TBI, RTBI, RGMII.
4. For GMII and TBI modes, TX_CLK is provided to UCC1 through QE_PC[8:11,14,15] (CLK9-12,15,16) and to UCC2 through QE_PC[2,3,6,7,15:17](CLK3,4,7,8,16:18). For RGMII and RTBI modes, TX_CLK is provided to UCC1 and UCC3 through QE_PC11(CLK12) and to UCC2 and UCC4 through QE_PC16 (CLK17).
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

2.3.4 Other Input Clocks

A description of the overall clocking of this device is available in the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and Enhanced Local Bus see the specific interface section.

2.4 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8569E. Note that the required GV_{DD}(typ) is 1.8 V for DDR2 SDRAM and GV_{DD}(typ) is 1.5 V for DDR3 SDRAM.

2.6 Ethernet Interface

This section provides the AC and DC electrical characteristics for the Ethernet interfaces inside the QUICC Engine block.

2.6.1 GMII/SGMII/MII/SMII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces are defined for 3.3 V. The GMII, MII, and TBI interface timing is compatible with IEEE Std 802.3™. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000)*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2 (3/20/1998)*. The electrical characteristics for the SGMII is specified in Section 2.6.4, "SGMII Interface Electrical Characteristics." The electrical characteristics for MDIO and MDC are specified in Section 2.7, "Ethernet Management Interface."

2.6.2 GMII, MII, RMII, SMII, TBI, RGMII and RTBI DC Electrical Characteristics

The following table shows the GMII, MII, RMII, SMII, and TBI DC electrical characteristics when operating from a 3.3 V supply.

Table 23. GMII, MII, RMII, SMII, and TBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

The following table shows the RGMII, and RTBI DC electrical characteristics when operating from a 2.5 V supply.

Table 24. RGMII and RTBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	10	μA	1

2.6.3.2.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

The following figure shows the MII transmit AC timing diagram.

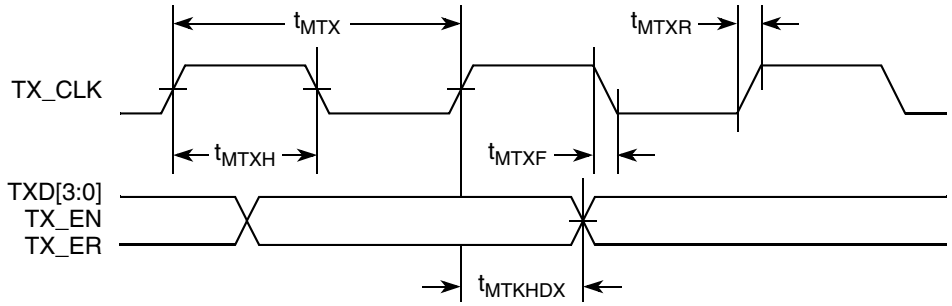


Figure 15. MII Transmit AC Timing Diagram

2.6.3.2.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns	1
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns	1
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	2
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.7.1.1 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 43. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} = 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$2\times(t_{plb\_clk}*8)$	—	—	ns	4
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	3, 4, 5
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDCF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the Mgmt Clock CE_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the QUICC Engine block clock/2.
5. MDC to MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time (t_{MDKHDX}).
(Min setup = cycle time – max delay

The following figure shows the MII management AC timing diagram.

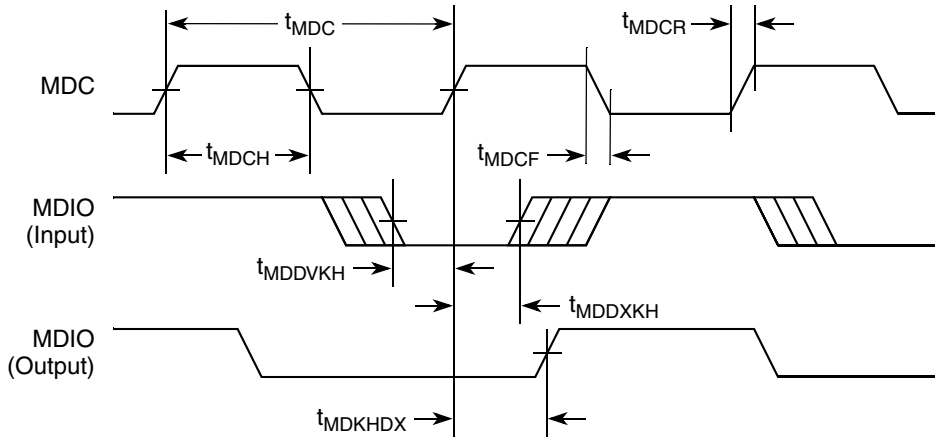


Figure 34. MII Management Interface Timing Diagram

The following table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 52. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.11.3 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.11.3.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clocks of the SRIO interface are described in Section 2.9.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.11.3.2 DC Serial RapidIO Timing Transmitter Specifications

The LP-serial transmitter electrical and timing specifications are given in the following sections.

The differential return loss, S11, of the transmitter in each case are better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

The following table defines the serial RapidIO transmitter DC specifications.

Table 53. SRIO Transmitter DC Timing Specifications—1.25, 2.5, and 3.125 GBauds

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.11.3.3 DC Serial RapidIO Receiver Specifications

The LP-serial receiver electrical and timing specifications are given in the following sections.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 57. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD} (max))	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *MPC8569E PowerQUICC III Integrated Processor Family Reference Manual* for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.12.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface.

Table 58. I²C AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

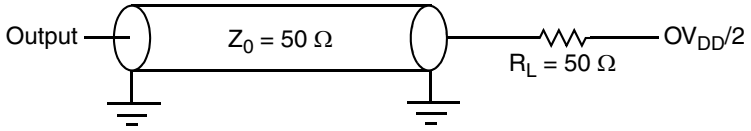


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

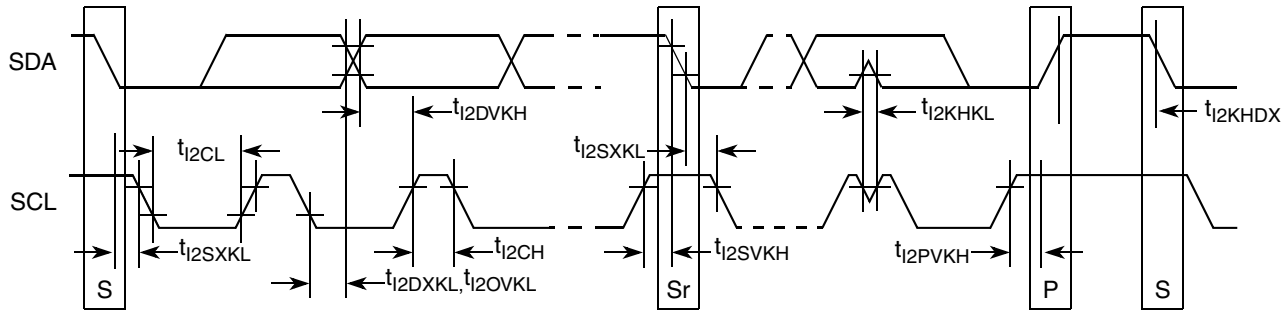


Figure 50. I²C Bus AC Timing Diagram

2.14 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 61. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

Table 62. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	4
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—

The following figure shows the AC timing diagram for PLL-enabled mode.

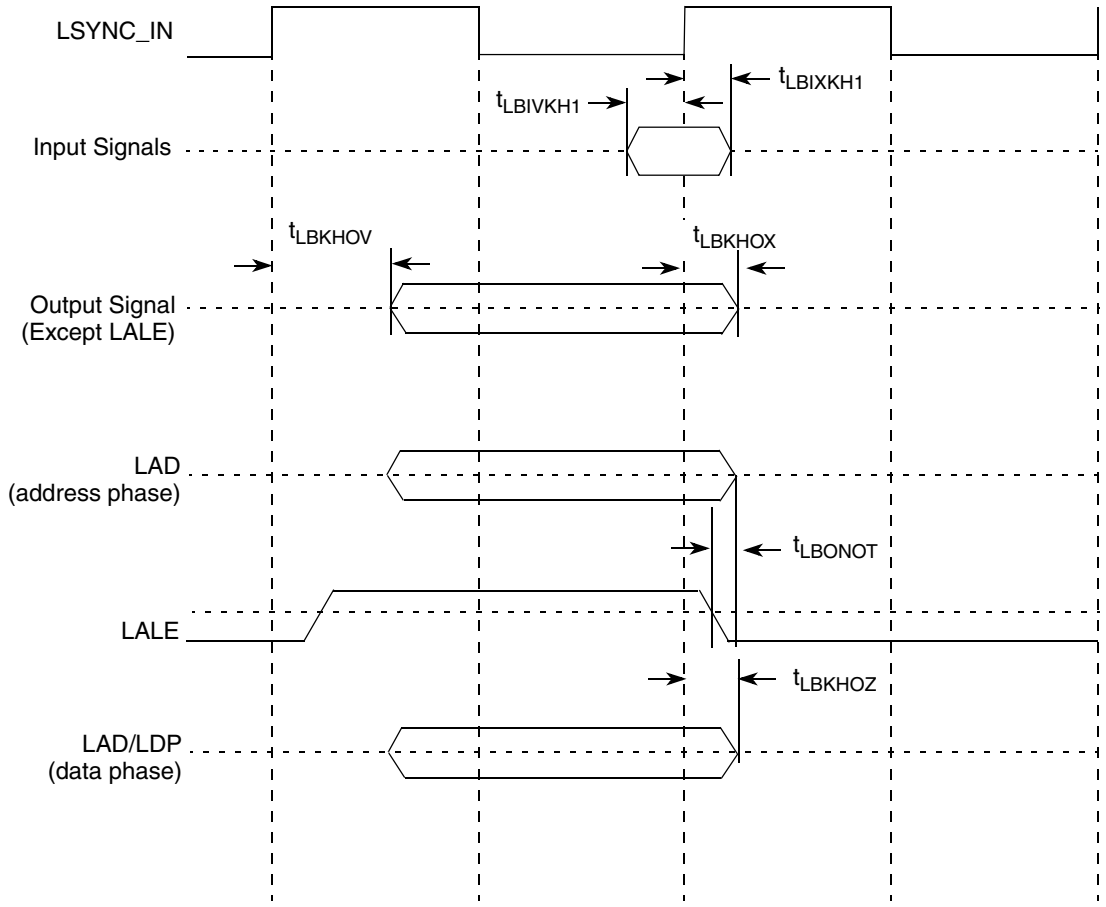


Figure 57. Local Bus AC Timing Diagram (PLL Enabled)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM and FCM.

For input signals, the AC timing data is used directly for all three controllers.

Table 68. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –100 μA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	μA	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.16.2 eSDHC AC Timing Specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 61 and Figure 62.

Table 69. eSDHC AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO full speed/high speed mode MMC full speed/high speed mode	f_{SHSCK}	0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—High speed/Full speed mode	t_{SHSCKL}	7/10	—	ns	4
SD_CLK clock high time—High speed/Full speed mode	t_{SHSCKH}	7/10	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4, 5
Input setup times: SD_CMD, SD_DATx, $\overline{SD\_CD}$ to SD_CLK	$t_{SHSIVKH}$	3.7	—	ns	3, 4, 6
Input hold times: SD_CMD, SD_DATx, $\overline{SD\_CD}$ to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 6
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4, 6

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 0.65ns.
4. Ccard ≤10 pF, (1 card) and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
6. The parameter values apply to both full speed and high speed modes.

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

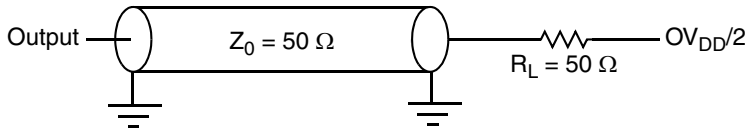


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

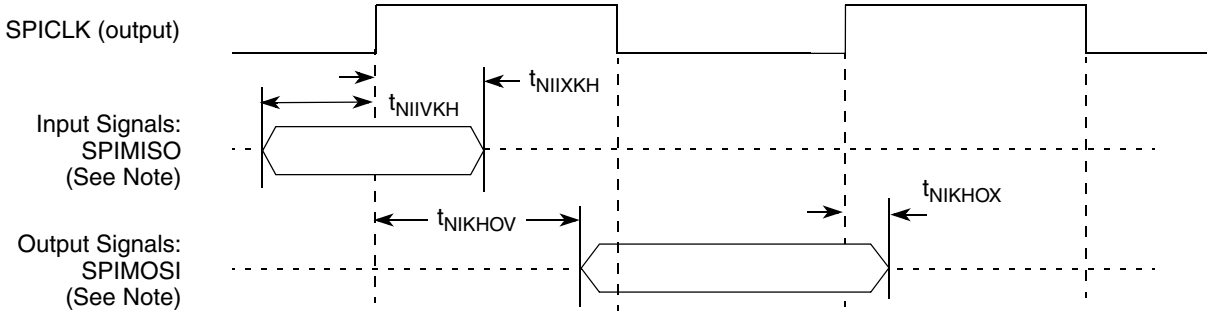
Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.