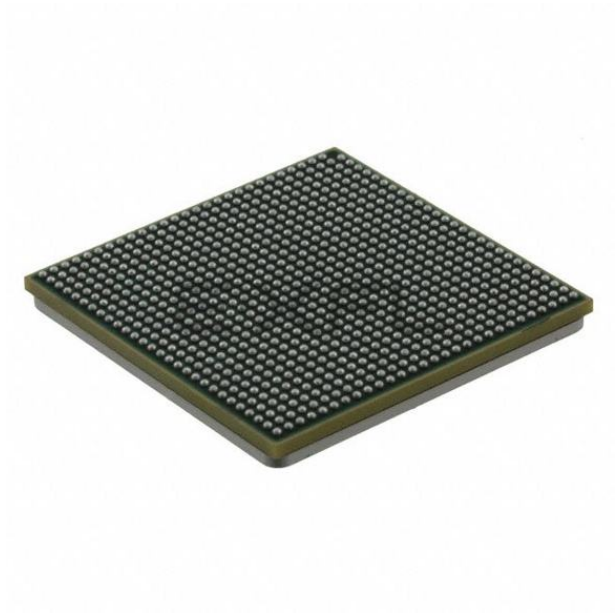

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569vtaqljb

The following figure provides detailed view D of the MPC8569E 783-pin BGA ball map diagram.

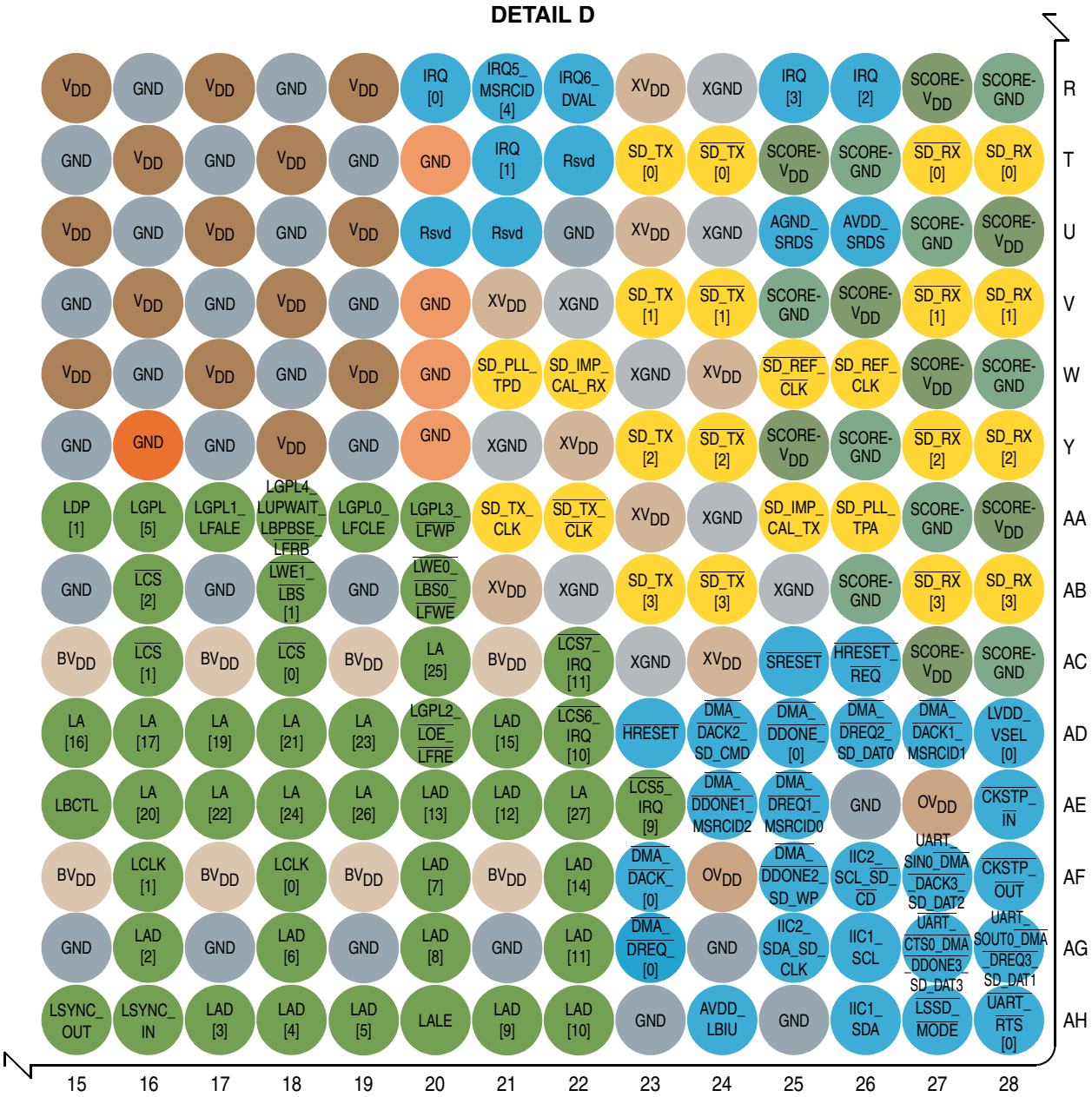


Figure 6. MPC8569E Detail D Ball Map

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDIC0	J2	I/O	GV_{DD}	27
D2_MDIC1	L2	I/O	GV_{DD}	27
D2_MDM0/D1_MDM4	A13	I/O	GV_{DD}	—
D2_MDM1/D1_MDM5	D13	I/O	GV_{DD}	—
D2_MDM2/D1_MDM6	G14	I/O	GV_{DD}	—
D2_MDM3/D1_MDM7	A9	I/O	GV_{DD}	—
D2_MDM8	E8	I/O	GV_{DD}	—
D2_MDQ0/D1_MDQ32	B14	I/O	GV_{DD}	—
D2_MDQ1/D1_MDQ33	C14	I/O	GV_{DD}	—
D2_MDQ2/D1_MDQ34	C11	I/O	GV_{DD}	—
D2_MDQ3/D1_MDQ35	B11	I/O	GV_{DD}	—
D2_MDQ4/D1_MDQ36	B15	I/O	GV_{DD}	—
D2_MDQ5/D1_MDQ37	A14	I/O	GV_{DD}	—
D2_MDQ6/D1_MDQ38	A12	I/O	GV_{DD}	—
D2_MDQ7/D1_MDQ39	A11	I/O	GV_{DD}	—
D2_MDQ8/D1_MDQ40	F14	I/O	GV_{DD}	—
D2_MDQ9/D1_MDQ41	F13	I/O	GV_{DD}	—
D2_MDQ10/D1_MDQ42	G11	I/O	GV_{DD}	—
D2_MDQ11/D1_MDQ43	F11	I/O	GV_{DD}	—
D2_MDQ12/D1_MDQ44	E14	I/O	GV_{DD}	—
D2_MDQ13/D1_MDQ45	D14	I/O	GV_{DD}	—
D2_MDQ14/D1_MDQ46	D12	I/O	GV_{DD}	—
D2_MDQ15/D1_MDQ47	E11	I/O	GV_{DD}	—
D2_MDQ16/D1_MDQ48	J15	I/O	GV_{DD}	—
D2_MDQ17/D1_MDQ49	J14	I/O	GV_{DD}	—
D2_MDQ18/D1_MDQ50	K13	I/O	GV_{DD}	—
D2_MDQ19/D1_MDQ51	J12	I/O	GV_{DD}	—
D2_MDQ20/D1_MDQ52	H15	I/O	GV_{DD}	—
D2_MDQ21/D1_MDQ53	G15	I/O	GV_{DD}	—
D2_MDQ22/D1_MDQ54	G13	I/O	GV_{DD}	—
D2_MDQ23/D1_MDQ55	H12	I/O	GV_{DD}	—
D2_MDQ24/D1_MDQ56	C10	I/O	GV_{DD}	—
D2_MDQ25/D1_MDQ57	C8	I/O	GV_{DD}	—
D2_MDQ26/D1_MDQ58	C7	I/O	GV_{DD}	—
D2_MDQ27/D1_MDQ59	B7	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
TDI	P21	I	OV_{DD}	26
TDO	P23	O	OV_{DD}	25
TMS	N22	I	OV_{DD}	26
$\overline{\text{TRST}}$	P22	I	OV_{DD}	26
Programmable Interrupt Controller				
IRQ0	R20	I	OV_{DD}	—
IRQ1	T21	I	OV_{DD}	—
IRQ2	R26	I	OV_{DD}	—
IRQ3	R25	I	OV_{DD}	—
IRQ4/MSRCID3	N20	I	OV_{DD}	—
IRQ5/MSRCID4	R21	I	OV_{DD}	—
IRQ6/MDVAL	R22	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	M20	O	OV_{DD}	5, 6, 11
$\overline{\text{MCP}}$	M22	I	OV_{DD}	6
$\overline{\text{UDE}}$	M21	I	OV_{DD}	6
QUICC Engine Block				
QE_PA0	T11	I/O	$LV_{DD}1$	—
QE_PA1	U11	I/O	$LV_{DD}1$	—
QE_PA2	R11	I/O	$LV_{DD}1$	—
QE_PA3	U10	I/O	$LV_{DD}1$	—
QE_PA4	R10	I/O	$LV_{DD}1$	—
QE_PA5	V11	I/O	OV_{DD}	—
QE_PA6	R9	I/O	$LV_{DD}1$	—
QE_PA7	U9	I/O	$LV_{DD}1$	—
QE_PA8	T8	I/O	$LV_{DD}1$	—
QE_PA9	U8	I/O	$LV_{DD}1$	—
QE_PA10	V10	I/O	OV_{DD}	—
QE_PA11	V9	I/O	OV_{DD}	—
QE_PA12	R8	I/O	$LV_{DD}1$	—
QE_PA13	V8	I/O	OV_{DD}	—
QE_PA14	P7	I/O	$LV_{DD}2$	—
QE_PA15	L6	I/O	$LV_{DD}2$	—
QE_PA16	M6	I/O	$LV_{DD}2$	—
QE_PA17	N6	I/O	$LV_{DD}2$	—
QE_PA18	L5	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	P18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W19	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	B22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	C3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D1	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	E12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H10	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	H13	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H20	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K11	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K6	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K9	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L21	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L23	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	AF11	—	—	—
GND	AF2	—	—	—
GND	AG15	—	—	—
GND	AG17	—	—	—
GND	AG19	—	—	—
GND	AG21	—	—	—
GND	AG24	—	—	—
GND	AG7	—	—	—
GND	AH23	—	—	—
GND	AH25	—	—	—
GND	B13	—	—	—
GND	B17	—	—	—
GND	B20	—	—	—
GND	B23	—	—	—
GND	B27	—	—	—
GND	B3	—	—	—
GND	B6	—	—	—
GND	B9	—	—	—
GND	C4	—	—	—
GND	D11	—	—	—
GND	D16	—	—	—
GND	D19	—	—	—
GND	D2	—	—	—
GND	D25	—	—	—
GND	D28	—	—	—
GND	D5	—	—	—
GND	E13	—	—	—
GND	F17	—	—	—
GND	F20	—	—	—
GND	F23	—	—	—
GND	F27	—	—	—
GND	F3	—	—	—
GND	F6	—	—	—
GND	F9	—	—	—
GND	H1	—	—	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

2.1.1.2 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal	18 (full strength mode) 35 (half strength mode)	GV_{DD} = 1.8 V	1
DDR3 signal	20 (full strength mode) 40 (half strength mode)	GV_{DD} = 1.5 V	1
DUART, EPIC, I^2C, JTAG, system control	45	OV_{DD} = 3.3 V	—

Note:

1. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_J = 105°C and at GV_{DD} (min). Refer to the MPC8569 reference manual for the DDR impedance programming procedure through the DDR control driver register 1 (DDRCDR_1).

2.1.2 Power Sequencing

The MPC8569E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $LV_{DD}n$, OV_{DD}, ScoreVDD, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

While V_{DD} is ramping, current may be supplied from V_{DD} through the MPC8569E to GV_{DD}. Nevertheless, GV_{DD} from an external supply should follow the sequencing described above.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

2.1.3 RESET Initialization

This section describes the AC electrical specifications for the RESET timing requirements of the MPC8569E. The following table describes the specifications for the RESET initialization timing.

Table 5. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	10	—	SYSCLK	1, 2
Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion	25	—	ns	3

2.6 Ethernet Interface

This section provides the AC and DC electrical characteristics for the Ethernet interfaces inside the QUICC Engine block.

2.6.1 GMII/SGMII/MII/SMII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces are defined for 3.3 V. The GMII, MII, and TBI interface timing is compatible with IEEE Std 802.3™. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000)*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2 (3/20/1998)*. The electrical characteristics for the SGMII is specified in Section 2.6.4, "SGMII Interface Electrical Characteristics." The electrical characteristics for MDIO and MDC are specified in Section 2.7, "Ethernet Management Interface."

2.6.2 GMII, MII, RMII, SMII, TBI, RGMII and RTBI DC Electrical Characteristics

The following table shows the GMII, MII, RMII, SMII, and TBI DC electrical characteristics when operating from a 3.3 V supply.

Table 23. GMII, MII, RMII, SMII, and TBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

The following table shows the RGMII, and RTBI DC electrical characteristics when operating from a 2.5 V supply.

Table 24. RGMII and RTBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	10	μA	1

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

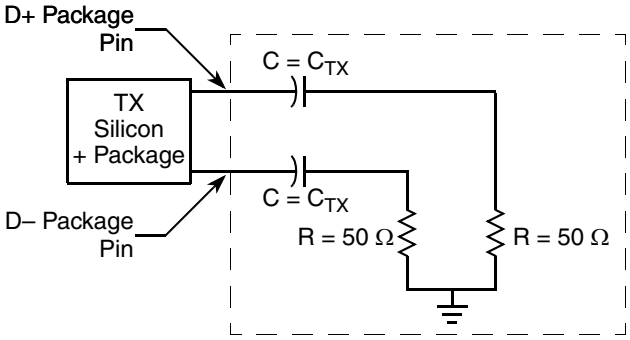


Figure 29. SGMII AC Test/Measurement Load

The following figure shows the data and command input AC timing diagram.

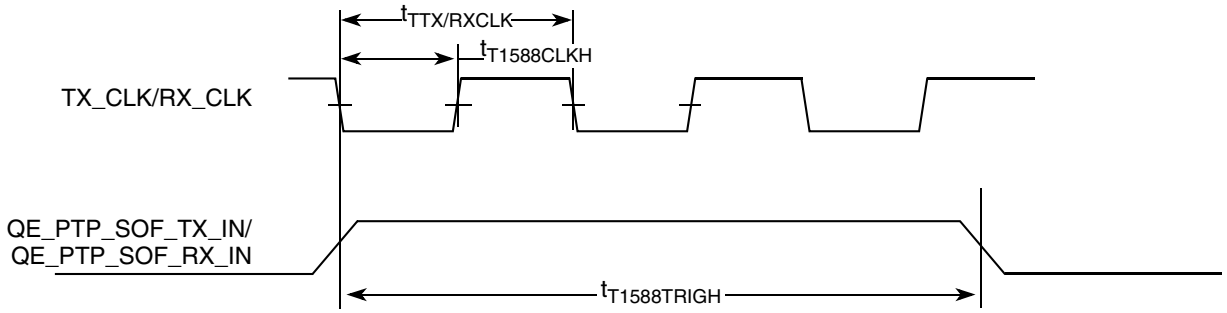


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

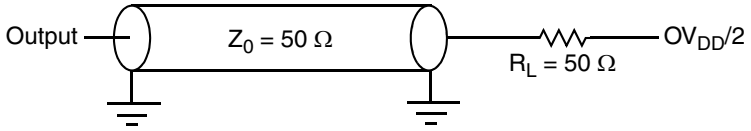


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

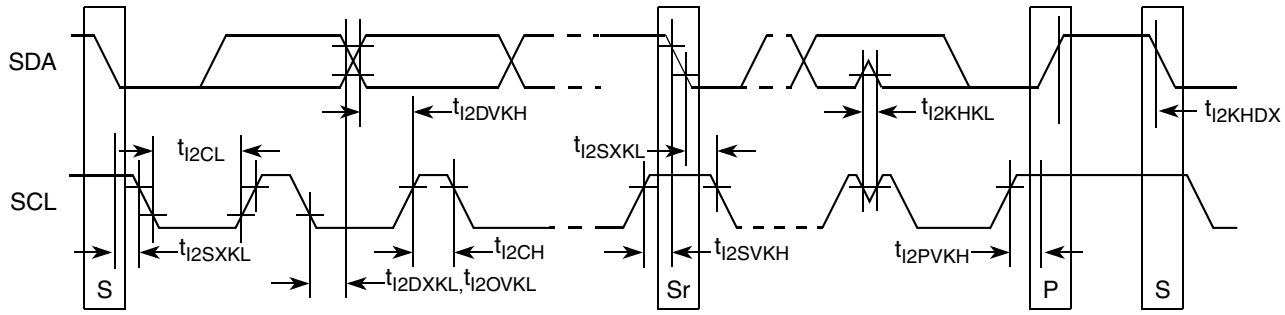


Figure 50. I²C Bus AC Timing Diagram

The following figure shows the AC timing diagram for PLL-enabled mode.

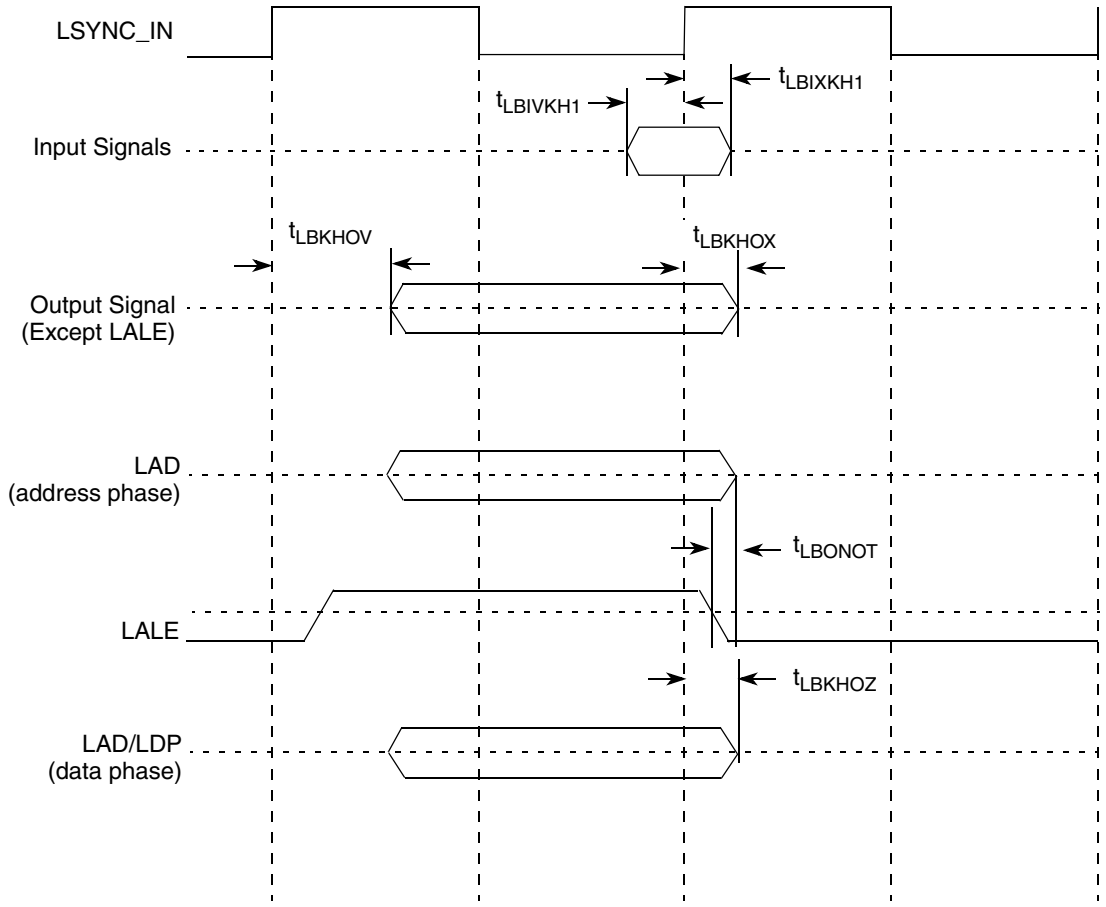
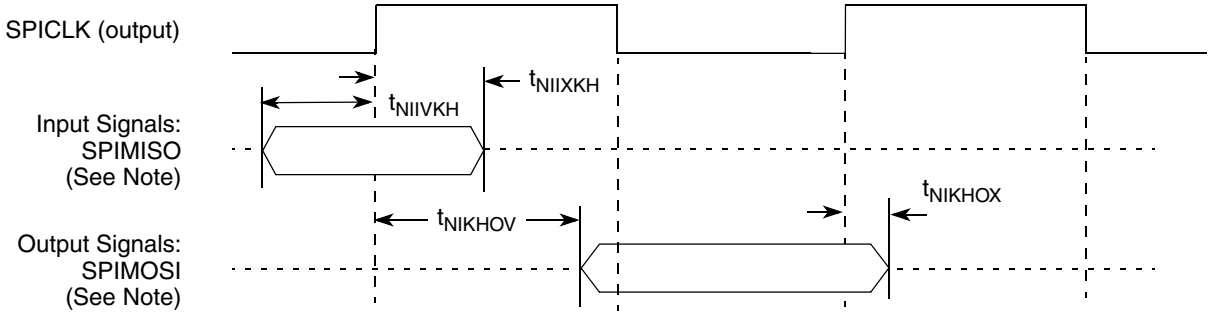


Figure 57. Local Bus AC Timing Diagram (PLL Enabled)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM and FCM.

For input signals, the AC timing data is used directly for all three controllers.

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

The following figure shows the UTOPIA/POS timing with internal clock.

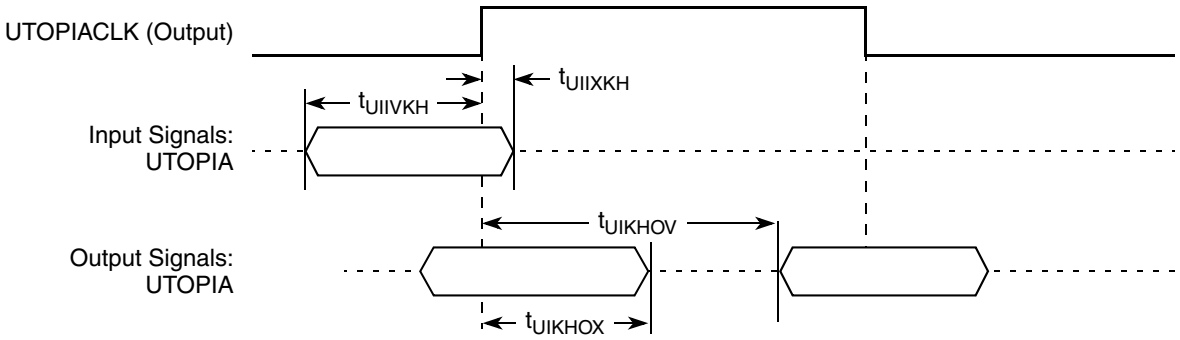


Figure 72. UTOPIA/POS AC Timing (Internal Clock) Diagram

3 Thermal

This section describes the thermal specifications of the MPC8569E.

3.1 Thermal Characteristics

The following table provides the package thermal characteristics of the MPC8569E.

Table 82. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	16	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	5	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	1.0	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.2 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the package. This spring force should not exceed 10 pounds force (45 Newtons).

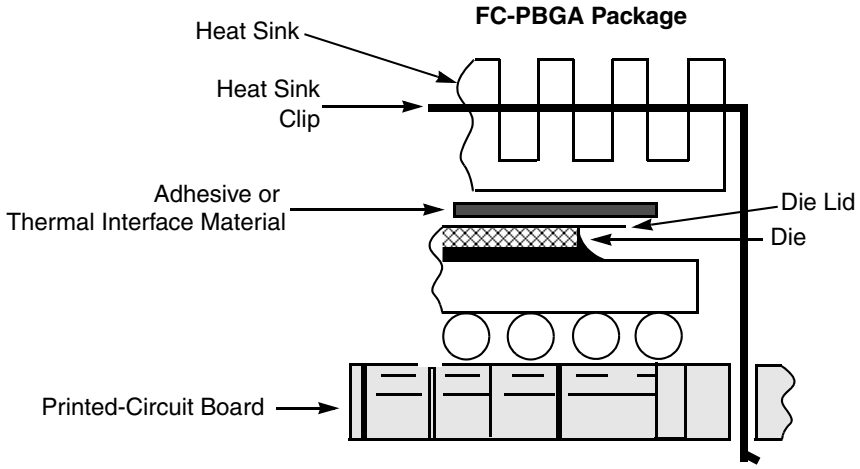


Figure 73. Package Exploded Cross-Sectional View

The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.3.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

5 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

Ordering information for the parts fully covered by this specification document is provided in Section 5.1, "Part Numbers Fully Addressed by This Document."

5.1 Part Numbers Fully Addressed by This Document

The following table shows the device nomenclature.

Table 84. Device Nomenclature

MPC	nnnn	E	C	Vx	AA	X	G	R
Product Code[1]	**Part Identifier**	**Security Engine**	**Temperature Range**	**Package** [2]	**Processor Frequency** [3]	**DDR Frequency**[4]	**QE Frequency**	**Revision Level**
MPC PPC	8569	E = included	Blank = 0° to 105°C C = –40° to 105°C	VT = FC-PBGA, Pb free, C5 spheres VJ = FC-PBGA, Pb free C4 bumps and pb free C5 spheres	AN = 800 MHz AQ = 1067 MHz AU = 1333 MHz	K = 600 MHz L = 667 MHz N = 800 MHz	G = 400 MHz J = 533 MHz L = 667 MHz	Blank = Rev. 1.0 (SVR = 0x8088_0010 A = Rev. 2.0 (SVR = 0x8088_0020 B = Rev. 2.1 (SVR = 0x8088_0021
		Blank = not included						A = Rev. 2.0 (SVR = 0x8080_0020 B = Rev. 2.1 (SVR = 0x8080_0021

Notes:

1. MPC stands for "qualified." PPC stands for pre-production samples.
2. See Section 4, "Package Description," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
4. See Table 85 for the corresponding maximum platform frequency.
5. C5 spheres are used by customer to attach to pcb. C4 bumps are bumps used on die of the device to connect between die and package substrate.

5.2 Part Marking

Parts are marked as the example shown in the following figure.

FC-PBGA

Notes:
MPC8569xxxxxx is the orderable part number.
MMMMM is the mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
ATWLYYWW is the traceability code.

Figure 76. Part Marking for FC-PBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8569E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8569ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)
- *QUICC Engine Block Reference Manual with Protocol Interworking* (document number: QEIWRM)

7 Document Revision History

The following table provides a revision history for this document.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
2	10/2013	• Added footnote 5 and added new VJ package description in Table 84, “Device Nomenclature.
1	02/2012	• In Table 1, “MPC8569E Pinout Listing,” updated pin U20 from Reserved to THERM1 (internal thermal diode anode) and pin U21 from Reserved to THERM0 (internal thermal diode cathode). Removed note 9 and added note 32 to pins U20 and U21. • In Table 38, “SGMII Transmit AC Timing Specifications,” updated min and typical values for the AC coupling capacitor parameter. • In Table 48, “SD_REF_CLK and SD_REF_CLK Input Clock Requirements,” removed the condition that the reference clock duty cycle should be measured at 1.6 V. • Added Section 2.6.5.1, “QUICC Engine Block IEEE 1588 DC Specifications.” • Added Section 3.3.3, “Temperature Diode.”
0	06/2011	Initial public release