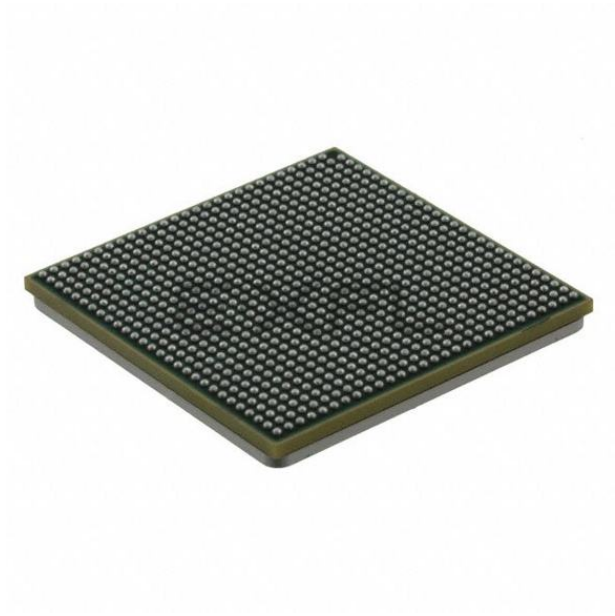

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569vtaunlb

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
DMA_DDONE1/MSRCID2	AE24	O	OV_{DD}	2
DMA_DDONE2/SD_WP	AF25	O	OV_{DD}	—
DMA_DREQ0	AG23	I	OV_{DD}	—
DMA_DREQ1/MSRCID0	AE25	I	OV_{DD}	—
DMA_DREQ2/SD_DAT0	AD26	I	OV_{DD}	—
DUART				
UART_SOUT0/DMA_DREQ3/SD_DAT1	AG28	O	OV_{DD}	2
UART_SIN0/DMA_DACK3/SD_DAT2	AF27	I	OV_{DD}	—
UART_CTS0/DMA_DDONE3/SD_DAT3	AG27	I	OV_{DD}	—
UART_RTS0	AH28	O	OV_{DD}	—
Enhanced Local Bus Controller Interface				
LA16	AD15	O	BV_{DD}	2
LA17	AD16	O	BV_{DD}	2
LA18	AE14	O	BV_{DD}	2
LA19	AD17	O	BV_{DD}	2
LA20	AE16	O	BV_{DD}	2
LA21	AD18	O	BV_{DD}	2
LA22	AE17	O	BV_{DD}	11
LA23	AD19	O	BV_{DD}	2
LA24	AE18	O	BV_{DD}	18
LA25	AC20	O	BV_{DD}	18
LA26	AE19	O	BV_{DD}	18
LA27	AE22	O	BV_{DD}	18
LAD0	AG14	I/O	BV_{DD}	23
LAD1	AF14	I/O	BV_{DD}	23
LAD2	AG16	I/O	BV_{DD}	23
LAD3	AH17	I/O	BV_{DD}	23
LAD4	AH18	I/O	BV_{DD}	23
LAD5	AH19	I/O	BV_{DD}	23
LAD6	AG18	I/O	BV_{DD}	23
LAD7	AF20	I/O	BV_{DD}	23
LAD8	AG20	I/O	BV_{DD}	23
LAD9	AH21	I/O	BV_{DD}	23
LAD10	AH22	I/O	BV_{DD}	23
LAD11	AG22	I/O	BV_{DD}	23

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
LAD12	AE21	I/O	BV_{DD}	23
LAD13	AE20	I/O	BV_{DD}	23
LAD14	AF22	I/O	BV_{DD}	23
LAD15	AD21	I/O	BV_{DD}	23
LALE	AH20	O	BV_{DD}	20
LBCTL	AE15	O	BV_{DD}	20
LCLK0	AF18	O	BV_{DD}	11
LCLK1	AF16	O	BV_{DD}	11
$\overline{\text{LCS0}}$	AC18	O	BV_{DD}	2
$\overline{\text{LCS1}}$	AC16	O	BV_{DD}	2
$\overline{\text{LCS2}}$	AB16	O	BV_{DD}	2
$\overline{\text{LCS3}}$	AC14	O	BV_{DD}	21
$\overline{\text{LCS4}}$/IRQ8	AD14	I/O	BV_{DD}	21
$\overline{\text{LCS5}}$/IRQ9	AE23	I/O	BV_{DD}	21
$\overline{\text{LCS6}}$/IRQ10	AD22	I/O	BV_{DD}	21
$\overline{\text{LCS7}}$/IRQ11	AC22	I/O	BV_{DD}	21
LDP0	AB14	I/O	BV_{DD}	—
LDP1	AA15	I/O	BV_{DD}	—
LGPL0/LFCLE	AA19	O	BV_{DD}	2
LGPL1/LFALE	AA17	O	BV_{DD}	2
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AD20	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	AA20	O	BV_{DD}	2
LGPL4/LUPWAIT/LBPBSE/$\overline{\text{LFRB}}$	AA18	I/O	BV_{DD}	29
LGPL5	AA16	O	BV_{DD}	2
LSYNC_IN	AH16	I	BV_{DD}	—
LSYNC_OUT	AH15	O	BV_{DD}	—
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$LFWE	AB20	O	BV_{DD}	11
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	AB18	O	BV_{DD}	24
I^2C				
IIC1_SDA	AH26	I/O	OV_{DD}	5, 28
IIC1_SCL	AG26	I/O	OV_{DD}	5, 28
IIC2_SDA/SD_CLK	AG25	I/O	OV_{DD}	3
IIC2_SCL/$\overline{\text{SD\_CD}}$	AF26	I/O	OV_{DD}	3
JTAG				
TCK	N21	I	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y18	1.0-V/1.1-V core power supply	V_{DD}	—
BV_{DD}	AC15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
GV_{DD}	B12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B2	1.8-/1.5-V DDR power supply	GV_{DD}	—

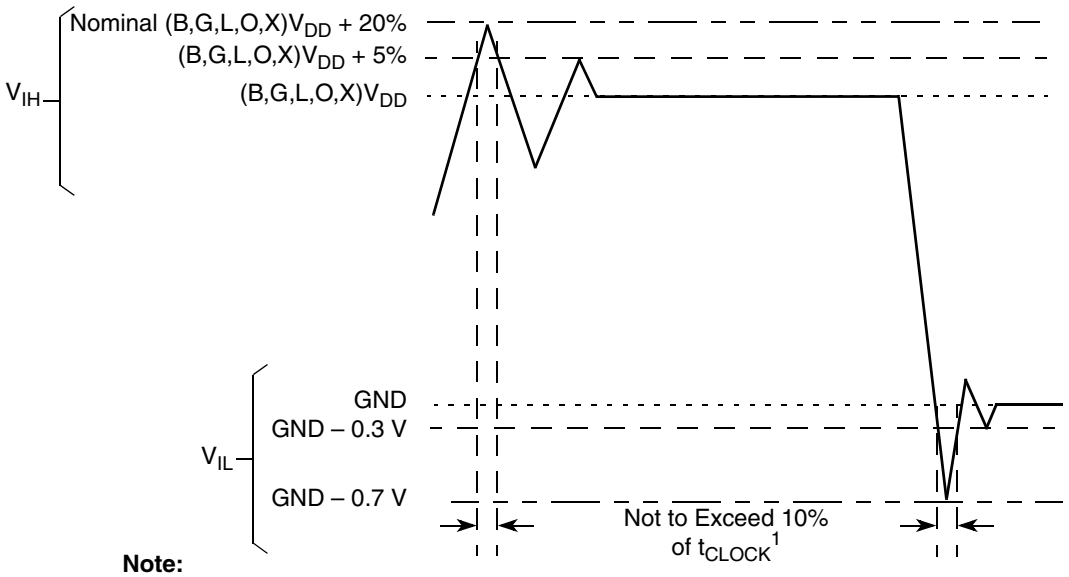
Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD	P14	Core supply sense	V_{DD}	13
XV_{DD}	AA23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AB21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AC24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	R23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	U23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	V21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	W24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	Y22	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
AV_{DD}_CORE	L1	1.0-V/1.1-V AV_{DD} supply for the core PLL	—	12
AV_{DD}_DDR	M28	1.0-V/1.1-V AV_{DD} supply for the DDR PLL	—	12
AV_{DD}_LBIU	AH24	1.0-V/1.1-V AV_{DD} supply for the eLBC PLL	—	12
AV_{DD}_PLAT	N28	1.0-V/1.1-V AV_{DD} supply for the platform PLL	—	12
AV_{DD}_QE	K1	1.0-V/1.1-V AV_{DD} supply for the QUICC Engine block PLL	—	12
AV_{DD}_SRDS	U26	1.0-V/1.1-V AV_{DD} supply for the SerDes PLL	—	12
GND	AA2	—	—	—
GND	AB15	—	—	—
GND	AB17	—	—	—
GND	AB19	—	—	—
GND	AC9	—	—	—
GND	AD5	—	—	—
GND	AE26	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	H11	—	—	—
GND	H14	—	—	—
GND	H17	—	—	—
GND	H21	—	—	—
GND	H25	—	—	—
GND	H28	—	—	—
GND	H6	—	—	—
GND	K12	—	—	—
GND	K15	—	—	—
GND	K19	—	—	—
GND	K2	—	—	—
GND	K21	—	—	—
GND	K27	—	—	—
GND	K5	—	—	—
GND	K7	—	—	—
GND	L12	—	—	—
GND	L14	—	—	—
GND	L16	—	—	—
GND	L18	—	—	—
GND	L20	—	—	—
GND	L22	—	—	—
GND	L24	—	—	—
GND	L28	—	—	—
GND	L8	—	—	—
GND	L9	—	—	—
GND	M1	—	—	—
GND	M13	—	—	—
GND	M15	—	—	—
GND	M17	—	—	—
GND	M19	—	—	—
GND	M2	—	—	—
GND	M27	—	—	—
GND	N10	—	—	—
GND	N12	—	—	—
GND	N14	—	—	—

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	—
RX_CLK clock rise time (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

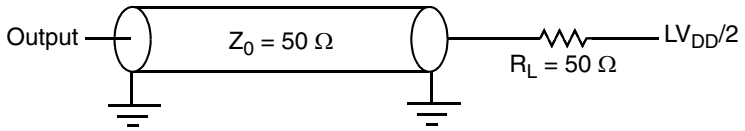


Figure 13. GMII AC Test Load

The following figure shows the GMII receive AC timing diagram.

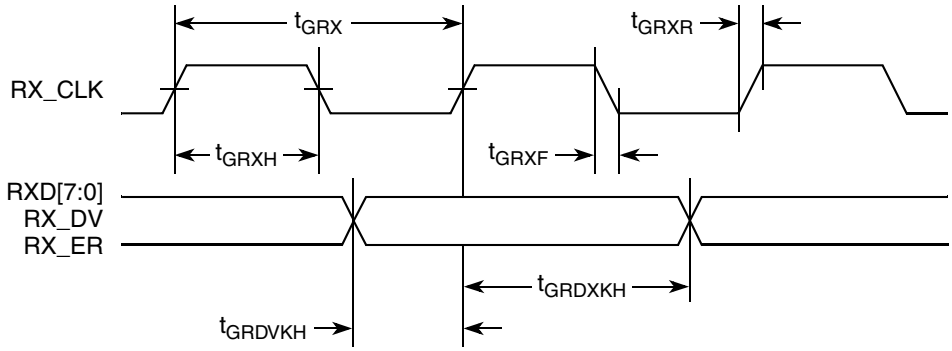


Figure 14. GMII Receive AC Timing Diagram

2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.6.3.4 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.6.3.4.1 RMII Transmit AC Timing Specifications

The following table shows the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMT}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMTH}	35	—	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	4.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	4.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

The following figure shows the RMII transmit AC timing diagram.

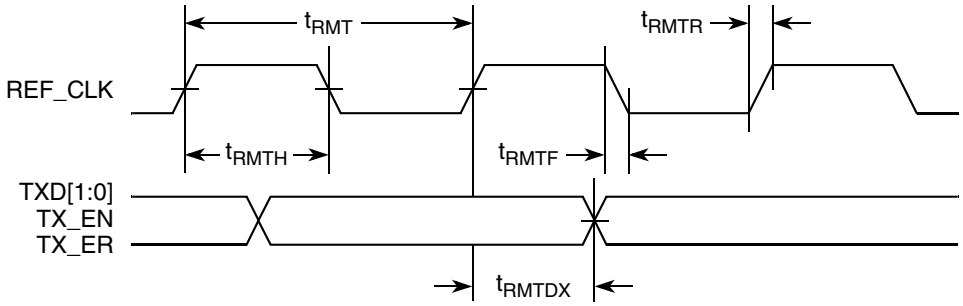


Figure 19. RMII Transmit AC Timing Diagram

2.6.3.4.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMR}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMRH}	35	—	65	%	1
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	1
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1

2.8 HDLC, BISYNC, Transparent, and Synchronous UART Interfaces

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART interfaces of the MPC8569E.

2.8.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the HDLC, BISYNC, Transparent, and synchronous UART interfaces.

Table 44. HDLC, BISYNC, and Transparent DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.8.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

The following table provides the input and output AC timing specifications for the HDLC, BISYNC, and Transparent protocols.

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	8.4	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	5.5	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	8	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns	—

— For external DC-coupled connection, as described in Section 2.9.2.2, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. The following figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

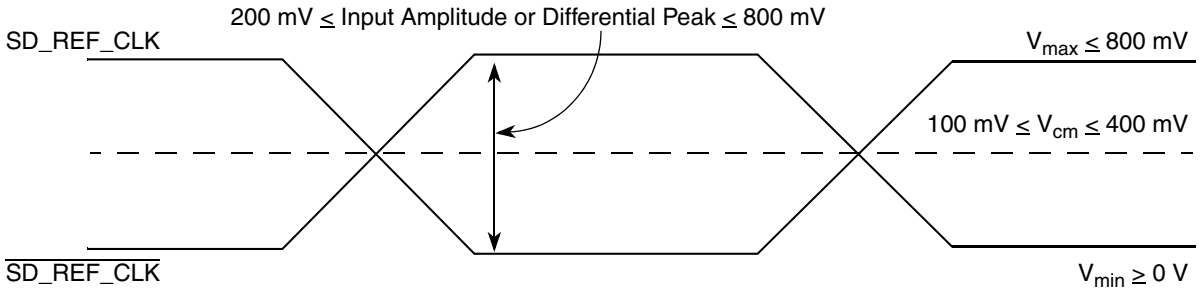


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SCOREGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SCOREGND). The following figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

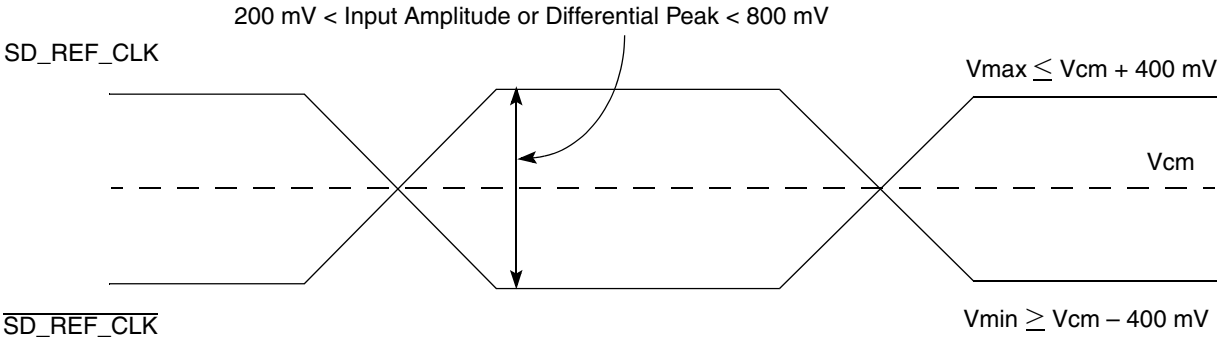


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-ended mode
  - — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. Measured at the package pins of the receiver.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.10.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.10.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum TX eye width	T_{TX-EYE}	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

2.10.4 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

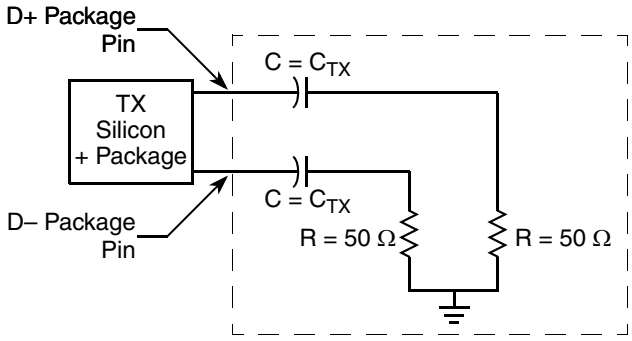


Figure 46. Compliance Test/Measurement Load

2.11 Serial RapidIO (SRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the MPC8569E, for the LP-serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC-coupling at the receiver input must be used.Signal Definitions

2.11.1 Signal Definitions

This section defines terms used in the description and specification of differential signals used by the LP-Serial links. Figure 47 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input

The following table defines the serial RapidIO receiver DC specifications.

Table 54. SRIO Receiver DC Timing Specifications—1.25 GBaud, 2.5 GBaud, 3.125 GBaud

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:
1. Measured at receiver

2.11.4 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.11.4.1 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the Serial RapidIO clock requirements for SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, “AC Requirements for SerDes Reference Clocks.”

2.11.4.2 AC Requirements for Serial RapidIO Transmitter

The following table defines the transmitter AC specifications for the Serial RapidIO. The AC timing specifications do not include RefClk jitter

Table 55. SRIO Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

The following table defines the receiver AC specifications for Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 56. SRIO Receiver AC Timing Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1, 3
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1, 3
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1, 3
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 48. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.
3. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

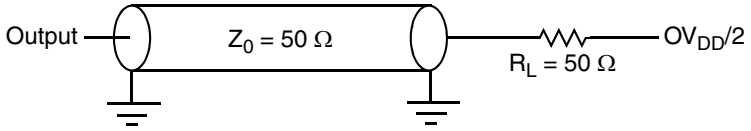


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

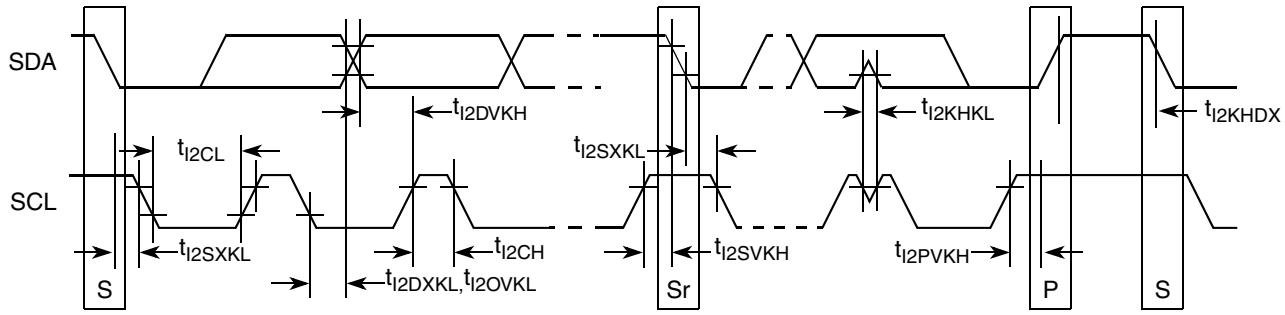


Figure 50. I²C Bus AC Timing Diagram

The following figure shows the AC timing diagram for PLL bypass mode.

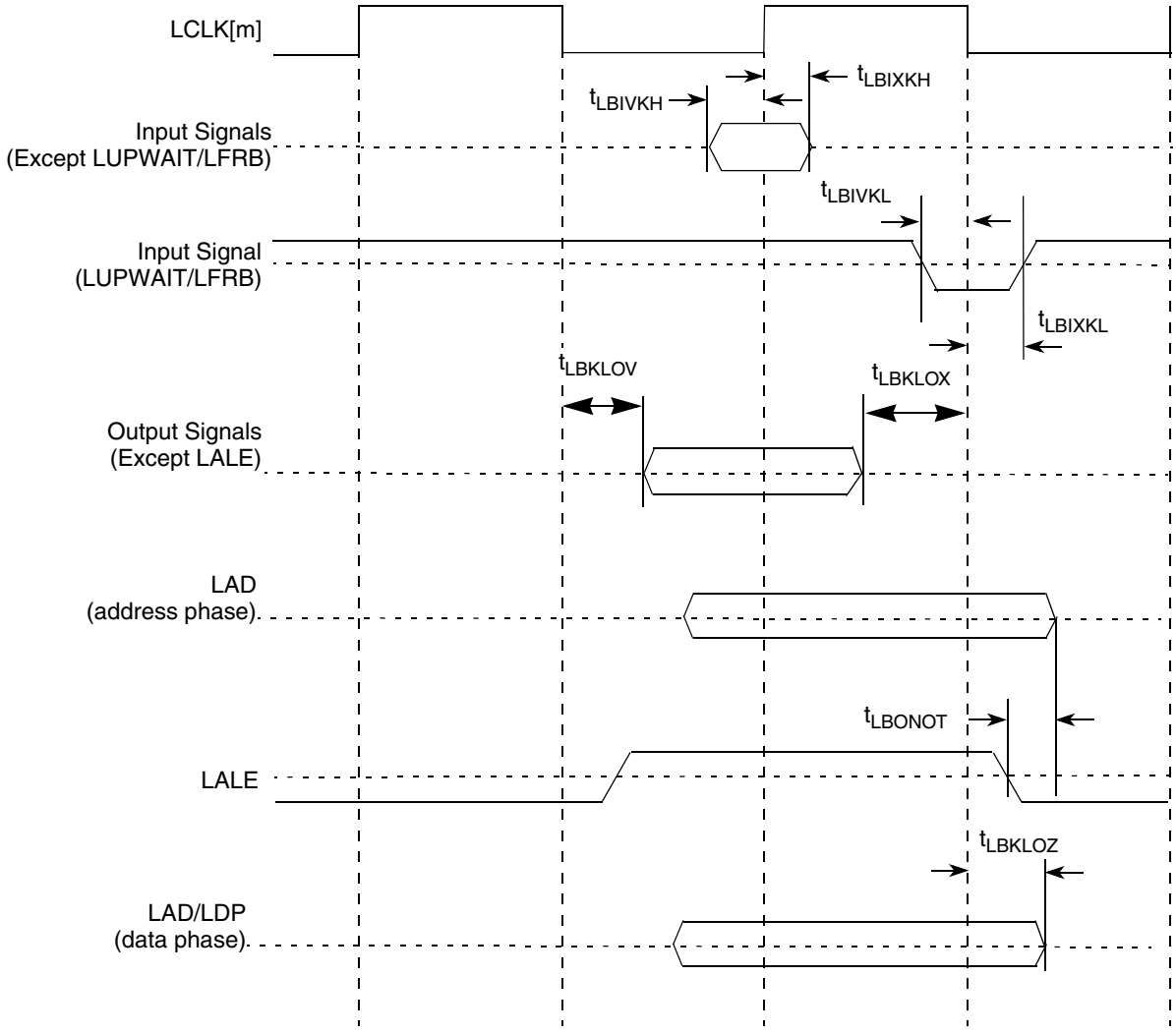


Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure provides the eSDHC clock input timing diagram.

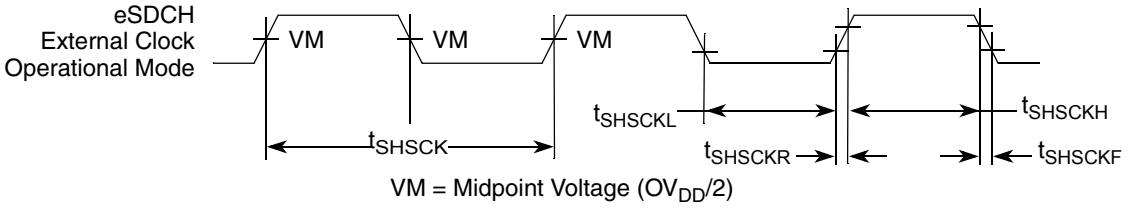


Figure 61. eSDHC Clock Input Timing Diagram

The following figure provides the data and command input/output timing diagram.

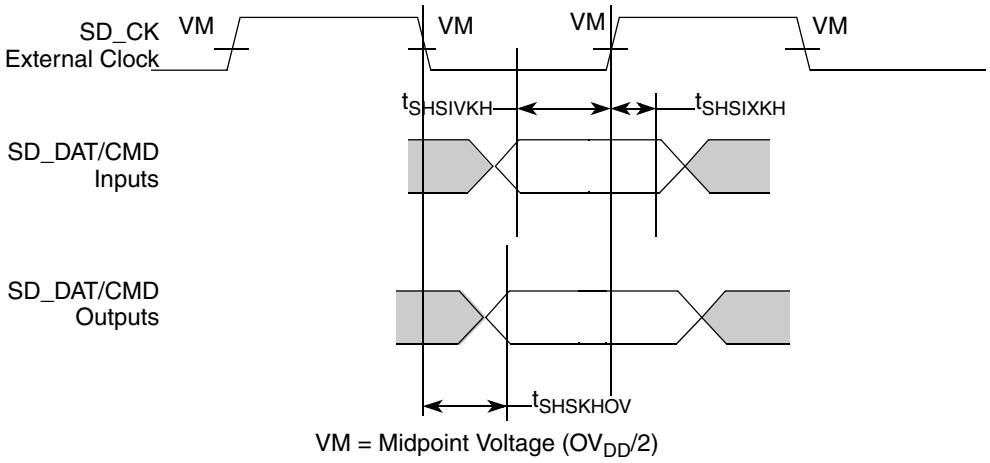


Figure 62. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8569E.

2.17.1 Timers DC Electrical Characteristics

The following table provides the timers DC electrical characteristics.

Table 70. Timers DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OVIN = 0 V or OVIN = OVDD)	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 77. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

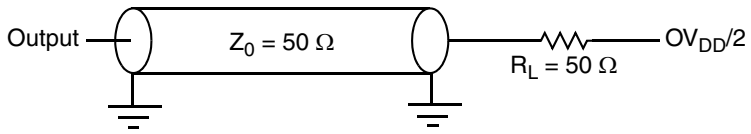
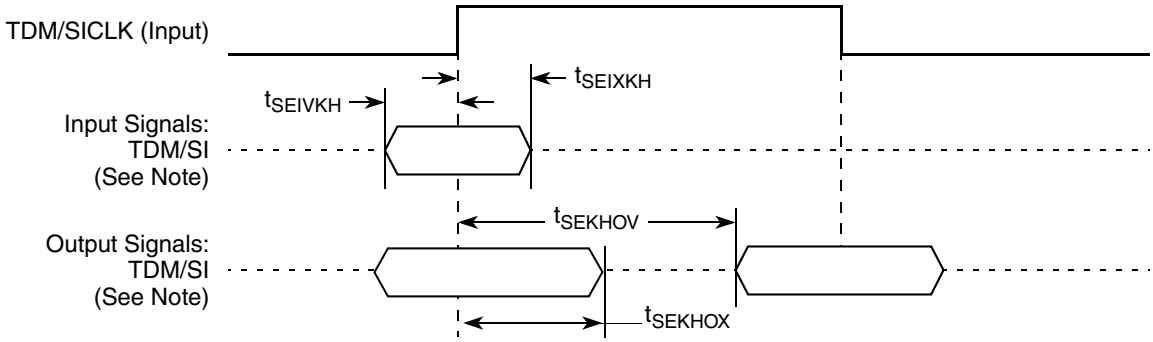


Figure 67. TDM/SI AC Test Load

The below figure represents the AC timing from Table 77. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. The following figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 68. TDM/SI AC Timing (External Clock) Diagram

The following figure provide the AC test load for the USB.

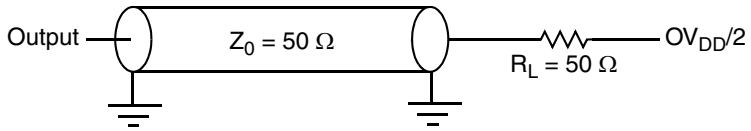


Figure 69. USB AC Test Load

2.22 UTOPIA/POS Interface

This section describes the DC and AC electrical specifications for the UTOPIA interface.

2.22.1 UTOPIA/POS DC Electrical Characteristics

The following table provides the DC electrical characteristics.

Table 80. UTOPIA/POS DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.22.2 UTOPIA/POS AC Timing Specifications

The following table provides the UTOPIA/POS input and output AC timing specifications.

Table 81. UTOPIA/POS AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA/POS outputs—Internal clock delay	t_{UIKHOV}	0	8.0	ns
UTOPIA/POS outputs—External clock delay	t_{UEKHOV}	1.0	10.0	ns
UTOPIA/POS outputs—Internal clock high Impedance	t_{UIKHOX}	0	8.0	ns
UTOPIA/POS outputs—External clock high impedance	t_{UEKHOX}	1.0	10.0	ns
UTOPIA/POS inputs—Internal clock input setup time	t_{UIIVKH}	6.4	—	ns