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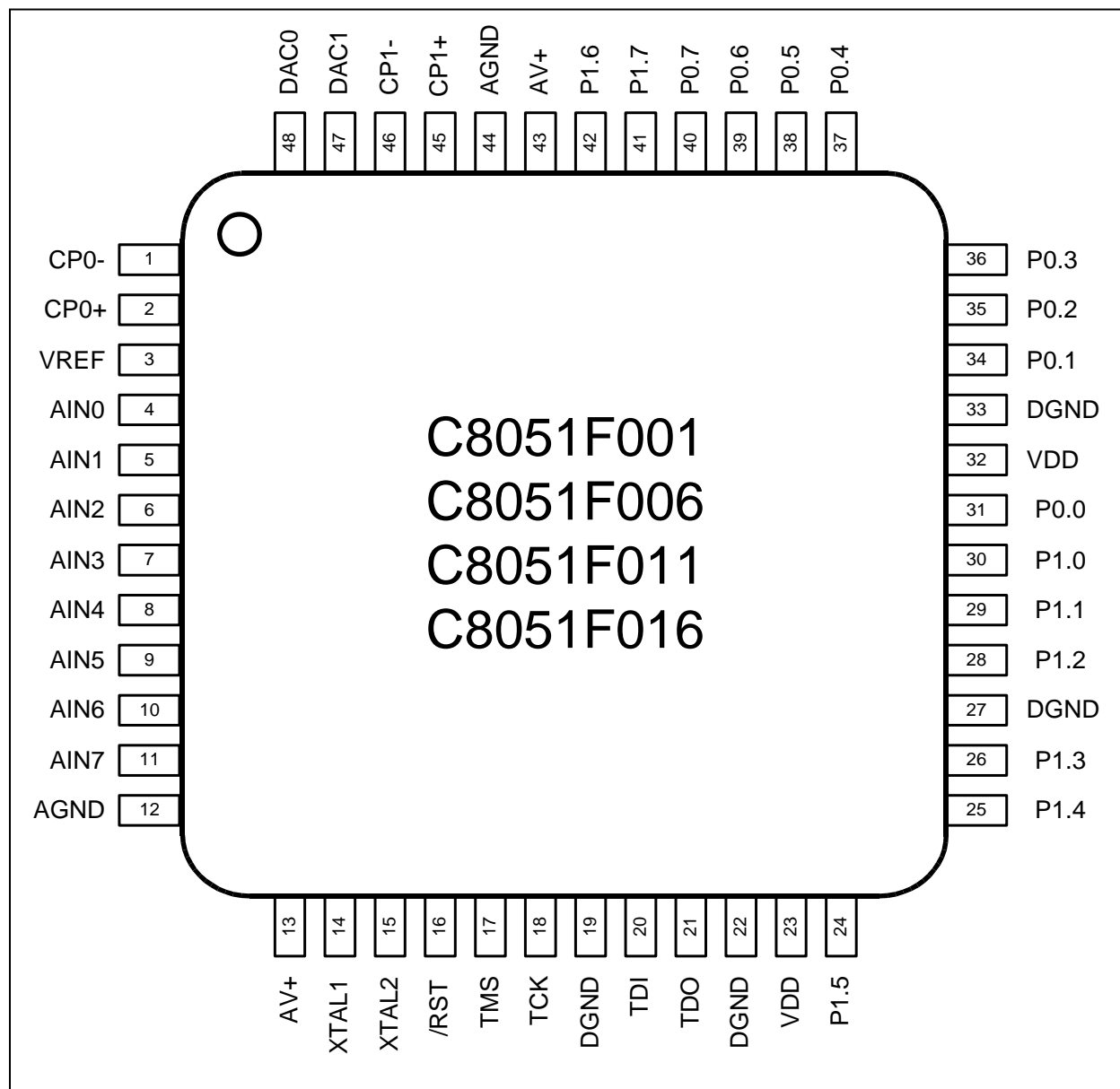
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/c8051f001-gq">https://www.e-xfl.com/product-detail/silicon-labs/c8051f001-gq</a>

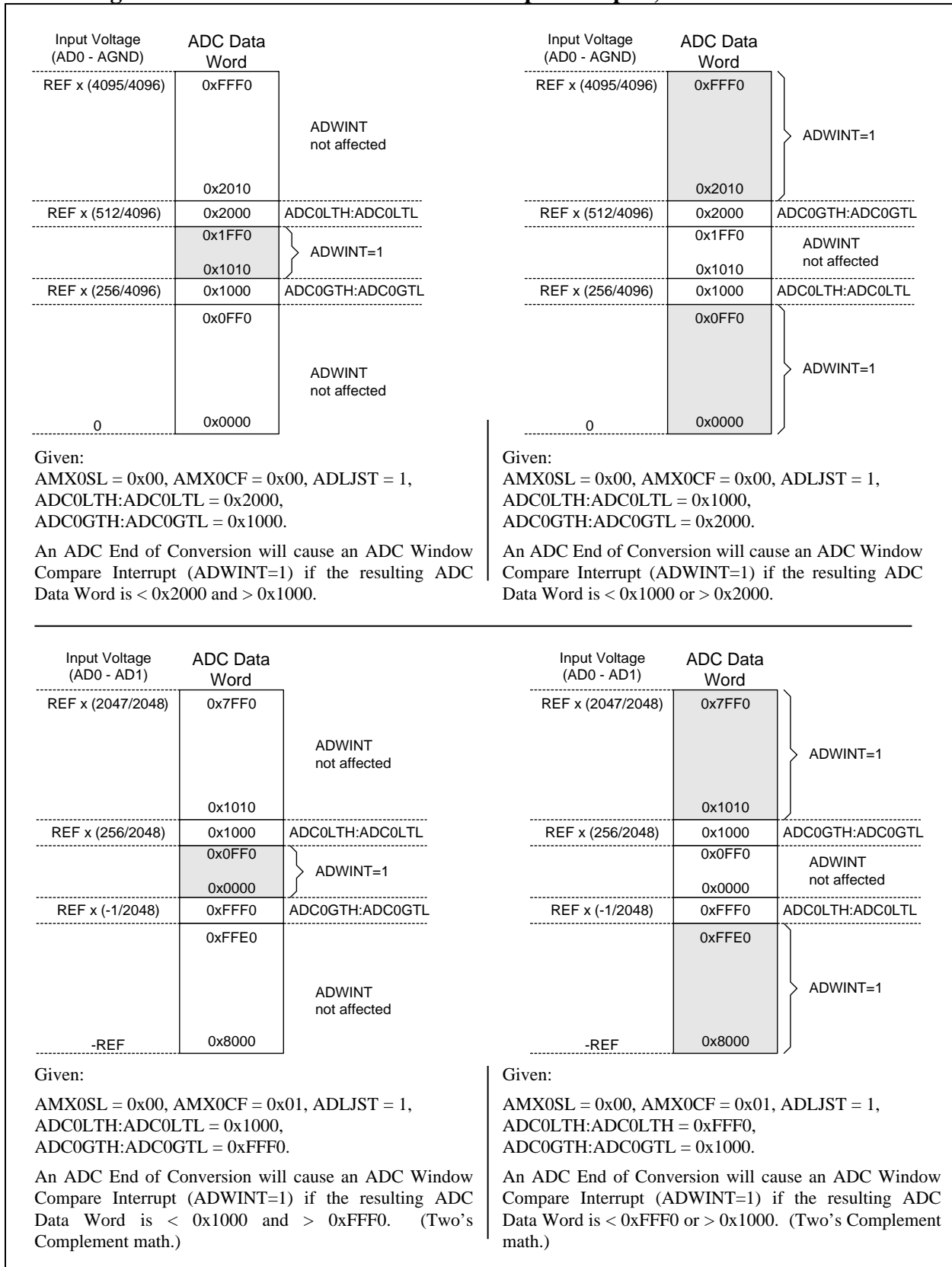
**Figure 4.3. TQFP-48 Pinout Diagram**



**Figure 5.7. ADC0CN: ADC Control Register (C8051F00x)**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCEN	ADCTM	ADCINT	ADBUSH	ADSTM1	ADSTM0	ADWINT	ADLJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
						(bit addressable)		0xE8
<p>Bit7: ADCEN: ADC Enable Bit  0: ADC Disabled. ADC is in low power shutdown.  1: ADC Enabled. ADC is active and ready for data conversions.</p> <p>Bit6: ADCTM: ADC Track Mode Bit  0: When the ADC is enabled, tracking is always done unless a conversion is in process  1: Tracking Defined by ADSTM1-0 bits  ADSTM1-0:  00: Tracking starts with the write of 1 to ADBUSH and lasts for 3 SAR clocks  01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks  10: ADC tracks only when CNVSTR input is logic low  11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks</p> <p>Bit5: ADCINT: ADC Conversion Complete Interrupt Flag  (Must be cleared by software)  0: ADC has not completed a data conversion since the last time this flag was cleared  1: ADC has completed a data conversion</p> <p>Bit4: ADBUSH: ADC Busy Bit  Read  0: ADC Conversion complete or no valid data has been converted since a reset. The falling edge of ADBUSH generates an interrupt when enabled.  1: ADC Busy converting data  Write  0: No effect  1: Starts ADC Conversion if ADSTM1-0 = 00b</p> <p>Bits3-2: ADSTM1-0: ADC Start of Conversion Mode Bits  00: ADC conversion started upon every write of 1 to ADBUSH  01: ADC conversions taken on every overflow of Timer 3  10: ADC conversion started upon every rising edge of CNVSTR  11: ADC conversions taken on every overflow of Timer 2</p> <p>Bit1: ADWINT: ADC Window Compare Interrupt Flag  (Must be cleared by software)  0: ADC Window Comparison Data match has not occurred  1: ADC Window Comparison Data match occurred</p> <p>Bit0: ADLJST: ADC Left Justify Data Bit  0: Data in ADC0H:ADC0L Registers is right justified  1: Data in ADC0H:ADC0L Registers is left justified</p>								

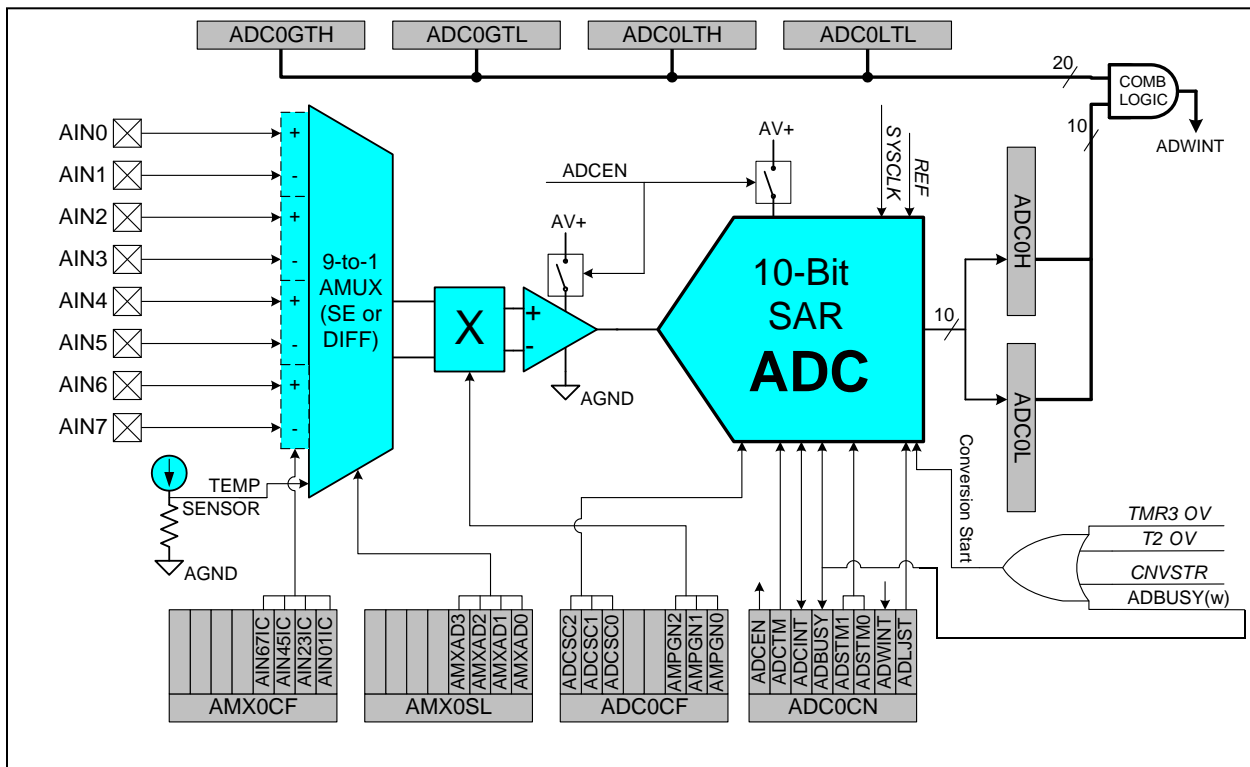
**Figure 5.15. 12-Bit ADC Window Interrupt Examples, Left Justified Data**



## 6. ADC (10-Bit, C8051F010/1/2/5/6/7 Only)

The ADC subsystem for the C8051F010/1/2/5/6/7 consists of a 9-channel, configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 10-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector (see block diagram in Figure 6.1). The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Register's shown in Figure 6.1. The ADC subsystem (ADC, track-and-hold and PGA) is enabled only when the ADCEN bit in the ADC Control register (ADC0CN, Figure 6.7) is set to 1. The ADC subsystem is in low power shutdown when this bit is 0. The Bias Enable bit (BIASE) in the REF0CN register (see Figure 9.2) must be set to 1 in order to supply bias to the ADC.

Figure 6.1. 10-Bit ADC Functional Block Diagram



### 6.1. Analog Multiplexer and PGA

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-board temperature sensor (temperature transfer function is shown in Figure 6.3). Note that the PGA gain is applied to the temperature sensor reading. AMUX input pairs can be programmed to operate in either the differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes “on-the-fly”. The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (Figure 6.5), and the Configuration register AMX0CF (Figure 6.4). The table in Figure 6.5 shows AMUX functionality by channel for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the AMPGN2-0 bits in the ADC Configuration register, ADC0CF (Figure 6.6). The PGA can be software-programmed for gains of 0.5, 1, 2, 4, 8 or 16. It defaults to unity gain on reset.

Figure 6.5. AMX0SL: AMUX Channel Select Register (C8051F01x)

								Reset Value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00000000
-	-	-	-	AMXAD3	AMXAD2	AMXAD1	AMXAD0	SFR Address: 0xBB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7-4: UNUSED. Read = 0000b; Write = don't care  
 Bits3-0: AMXAD3-0: AMUX Address Bits  
 0000-1111: ADC Inputs selected per chart below

		AMXAD3-0								
		0000	0001	0010	0011	0100	0101	0110	0111	1xxx
A M X 0 S L  B I T S  3 - 0	0000	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	1000	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR

## 8. COMPARATORS

The MCU family has two on-chip analog voltage comparators as shown in Figure 8.1. The inputs of each Comparator are available at the package pins. The output of each comparator is optionally available at the package pins via the I/O crossbar (see Section 15.1). When assigned to package pins, each comparator output can be programmed to operate in open drain or push-pull modes (see section 15.3).

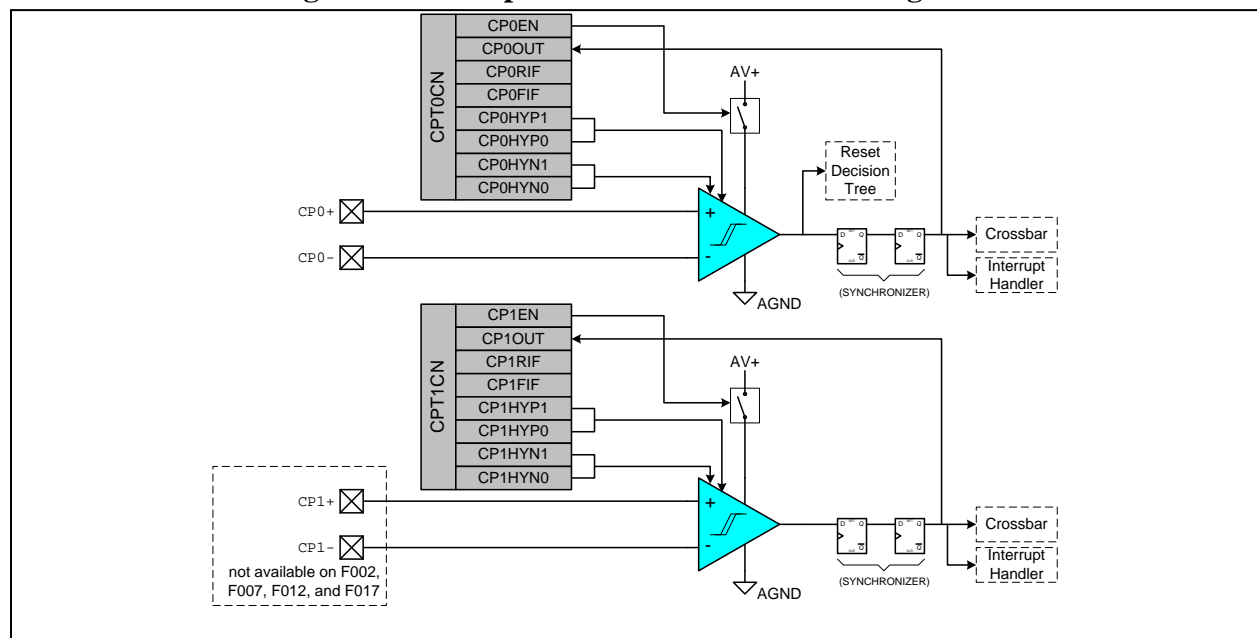
The hysteresis of each comparator is software-programmable via its respective Comparator control register (CPT0CN, CPT1CN). The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage. The output of the comparator can be polled in software, or can be used as an interrupt source. Each comparator can be individually enabled or disabled (shutdown). When disabled, the comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, its interrupt capability is suspended and its supply current falls to less than 1 $\mu$ A. Comparator 0 inputs can be externally driven from -0.25V to (AV+) + 0.25V without damage or upset.

The Comparator 0 hysteresis is programmed using bits 3-0 in the Comparator 0 Control Register CPT0CN (shown in Figure 8.3). The amount of *negative* hysteresis voltage is determined by the settings of the CP0HYN bits. As shown in Figure 8.2, settings of 10, 4 or 2mV of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of *positive* hysteresis is determined by the setting the CP0HYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section 10.4). The CP0FIF flag is set upon a Comparator 0 falling-edge interrupt, and the CP0RIF flag is set upon the Comparator 0 rising-edge interrupt. Once set, these bits remain set until cleared by the CPU. The Output State of Comparator 0 can be obtained at any time by reading the CP0OUT bit. Note the comparator output and interrupt should be ignored until the comparator settles after power-up. Comparator 0 is enabled by setting the CP0EN bit, and is disabled by clearing this bit. Note there is a 20 $\mu$ s settling time for the comparator output to stabilize after setting the CP0EN bit or a power-up. Comparator 0 can also be programmed as a reset source. For details, see Section 13.

The operation of Comparator 1 is identical to that of Comparator 0, except the Comparator 1 is controlled by the CPT1CN Register (Figure 8.4). Comparator 1 can not be programmed as a reset source. Also, the input pins for Comparator 1 are not pinned out on the F002, F007, F012, or F017 devices. The complete electrical specifications for the Comparators are given in Table 8.1.

**Figure 8.1. Comparator Functional Block Diagram**



**Figure 9.2. REF0CN: Reference Control Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xD1

Bits7-3: UNUSED. Read = 00000b; Write = don't care  
 Bit2: TEMPE: Temperature Sensor Enable Bit  
       0: Internal Temperature Sensor Off.  
       1: Internal Temperature Sensor On.  
 Bit1: BIASE: Bias Enable Bit for ADC and DAC's  
       0: Internal Bias Off.  
       1: Internal Bias On (required for use of ADC or DAC's).  
 Bit0: REFBE: Internal Voltage Reference Buffer Enable Bit  
       0: Internal Reference Buffer Off. System reference can be driven from external source on VREF pin.  
       1: Internal Reference Buffer On. System reference provided by internal voltage reference.

**Table 9.1. Reference Electrical Characteristics**

VDD = 3.0V, AV+ = 3.0V, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INTERNAL REFERENCE (REFBE = 1)</b>					
Output Voltage	25°C ambient	2.34	2.43	2.50	V
VREF Short Circuit Current				30	mA
VREF Power Supply Current (supplied by AV+)			50		μA
VREF Temperature Coefficient			15		ppm/°C
Load Regulation	Load = (0-to-200μA) to AGND (Note 1)		0.5		ppm/μA
VREF Turn-on Time1	4.7μF tantalum, 0.1μF ceramic bypass		2		ms
VREF Turn-on Time2	0.1μF ceramic bypass		20		μs
VREF Turn-on Time3	no bypass cap		10		μs
<b>EXTERNAL REFERENCE (REFBE = 0)</b>					
Input Voltage Range		1.00		(AV+) - 0.3V	V
Input Current			0	1	μA

Note 1: The reference can only source current. When driving an external load, it is recommended to add a load resistor to AGND.



Address	Register	Description	Page No.
0x89	TMOD	Counter/Timer Mode	143
0x91	TMR3CN	Timer 3 Control	152
0x95	TMR3H	Timer 3 High	153
0x94	TMR3L	Timer 3 Low	153
0x93	TMR3RLH	Timer 3 Reload High	153
0x92	TMR3RLL	Timer 3 Reload Low	153
0xFF	WDTCN	Watchdog Timer Control	96
0xE1	XBR0	Port I/O Crossbar Configuration 1	105
0xE2	XBR1	Port I/O Crossbar Configuration 2	107
0xE3	XBR2	Port I/O Crossbar Configuration 3	108
0x84-86, 0x96-97, 0x9C, 0xA1-A3, 0xA9-AC, 0xAE, 0xB3-B5, 0xB9, 0xBD, 0xC9, 0xCE, 0xDF, 0xE4-E5, 0xF1-F5		Reserved	

\* Refers to a register in the C8051F000/1/2/5/6/7 only.

\*\* Refers to a register in the C8051F010/1/2/5/6/7 only.

\*\*\* Refers to a register in the C8051F005/06/07/15/16/17 only.

**Table 10.4. Interrupt Summary**

Interrupt Source	Interrupt Vector	Priority Order	Interrupt-Pending Flag	Enable
Reset	0x0000	Top	None	Always enabled
External Interrupt 0 (/INT0)	0x0003	0	IE0 (TCON.1)	EX0 (IE.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	ET0 (IE.1)
External Interrupt 1 (/INT1)	0x0013	2	IE1 (TCON.3)	EX1 (IE.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	ET1 (IE.3)
Serial Port (UART)	0x0023	4	RI (SCON.0) TI (SCON.1)	ES (IE.4)
Timer 2 Overflow (or EXF2)	0x002B	5	TF2 (T2CON.7)	ET2 (IE.5)
Serial Peripheral Interface	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	ESPI0 (EIE1.0)
SMBus Interface	0x003B	7	SI (SMB0CN.3)	ESMB0 (EIE1.1)
ADC0 Window Comparison	0x0043	8	ADWINT (ADC0CN.2)	EWADC0 (EIE1.2)
Programmable Counter Array 0	0x004B	9	CF (PCA0CN.7) CCFn (PCA0CN.n)	EPCA0 (EIE1.3)
Comparator 0 Falling Edge	0x0053	10	CP0FIF (CPT0CN.4)	ECP0F (EIE1.4)
Comparator 0 Rising Edge	0x005B	11	CP0RIF (CPT0CN.5)	ECP0R (EIE1.5)
Comparator 1 Falling Edge	0x0063	12	CP1FIF (CPT1CN.4)	ECP1F (EIE1.6)
Comparator 1 Rising Edge	0x006B	13	CP1RIF (CPT1CN.5)	ECP1R (EIE1.7)
Timer 3 Overflow	0x0073	14	TF3 (TMR3CN.7)	ET3 (EIE2.0)
ADC0 End of Conversion	0x007B	15	ADCINT (ADC0CN.5)	EADC0 (EIE2.1)
External Interrupt 4	0x0083	16	IE4 (PRT1IF.4)	EX4 (EIE2.2)
External Interrupt 5	0x008B	17	IE5 (PRT1IF.5)	EX5 (EIE2.3)
External Interrupt 6	0x0093	18	IE6 (PRT1IF.6)	EX6 (EIE2.4)
External Interrupt 7	0x009B	19	IE7 (PRT1IF.7)	EX7 (EIE2.5)
Unused Interrupt Location	0x00A3	20	None	Reserved (EIE2.6)
External Crystal OSC Ready	0x00AB	21	XTLVLD (OSCXCN.7)	EXVLD (EIE2.7)

#### 10.4.3. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP-EIP2) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate.

#### 10.4.4. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

### 13.8.1. Watchdog Usage

The WDT consists of a 21-bit timer running from the programmed system clock. The timer measures the period between specific writes to its control register. If this period exceeds the programmed limit, a WDT reset is generated. The WDT can be enabled and disabled as needed in software, or can be permanently enabled if desired. Watchdog features are controlled via the Watchdog Timer Control Register (WDTCN) shown in Figure 13.3.

#### Enable/Reset WDT

The watchdog timer is both enabled and the countdown restarted by writing 0xA5 to the WDTCN register. The user's application software should include periodic writes of 0xA5 to WDTCN as needed to prevent a watchdog timer overflow. The WDT is enabled and restarted as a result of any system reset.

#### Disable WDT

Writing 0xDE followed by 0xAD to the WDTCN register disables the WDT. The following code segment illustrates disabling the WDT.

```
CLR    EA                ; disable all interrupts
MOV    WDTCN,#0DEh      ; disable software
MOV    WDTCN,#0ADh      ; watchdog timer
SETB   EA                ; re-enable interrupts
```

The writes of 0xDE and 0xAD must occur within 4 clock cycles of each other, or the disable operation is ignored. Interrupts should be disabled during this procedure to avoid delay between the two writes.

#### Disable WDT Lockout

Writing 0xFF to WDTCN locks out the disable feature. Once locked out, the disable operation is ignored until the next system reset. Writing 0xFF does not enable or reset the watchdog timer. Applications always intending to use the watchdog should write 0xFF to WDTCN in their initialization code.

#### Setting WDT Interval

WDTCN.[2:0] control the watchdog timeout interval. The interval is given by the following equation:

$$4^{3+WDTCN[2:0]} \times T_{SYSCLK}, \text{ (where } T_{SYSCLK} \text{ is the system clock period).}$$

For a 2MHz system clock, this provides an interval range of 0.032msec to 524msec. WDTCN.7 must be a 0 when setting this interval. Reading WDTCN returns the programmed interval. WDTCN.[2:0] is 111b after a system reset.

**Figure 13.3. WDTCN: Watchdog Timer Control Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	xxxxx111
								SFR Address: 0xFF
<p>Bits7-0: WDT Control</p> <p>Writing 0xA5 both enables and reloads the WDT.</p> <p>Writing 0xDE followed within 4 clocks by 0xAD disables the WDT.</p> <p>Writing 0xFF locks out the disable feature.</p> <p>Bit4: Watchdog Status Bit (when Read)</p> <p>Reading the WDTCN.[4] bit indicates the Watchdog Timer Status.</p> <p>0: WDT is inactive</p> <p>1: WDT is active</p> <p>Bits2-0: Watchdog Timeout Interval Bits</p> <p>The WDTCN.[2:0] bits set the Watchdog Timeout Interval. When writing these bits, WDTCN.7 must be set to 0.</p>								

## 15. PORT INPUT/OUTPUT

The MCUs have a wide array of digital resources, which are available through four digital I/O ports, P0, P1, P2 and P3. Each of the pins on Ports 0, 1, and 2 can be defined as either its corresponding port I/O or one of the internal digital resources assigned as shown in Figure 15.1. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins available on the selected package (the C8051F000/05/10/15 have all four ports pinned out, the F001/06/11/16 have P0 and P1, and the F002/07/12/17 have P0). This resource assignment flexibility is achieved through the use of a Priority CrossBar Decoder. (Note that the state of a Port I/O pin can always be read in the corresponding Port latch regardless of the Crossbar settings).

The CrossBar assigns the selected internal digital resources to the I/O pins based on the Priority Decode Table 15.1. The registers XBR0, XBR1, and XBR2, defined in Figure 15.3, Figure 15.4, and Figure 15.5 are used to select an internal digital function or let an I/O pin default to being a Port I/O. The crossbar functions identically for each MCU, with the caveat that P2 is not pinned out on the F001/06/11/16, and both P1 and P2 are not pinned out on the F002/07/12/17. Digital resources assigned to port pins that are not pinned out cannot be accessed.

All Port I/Os are 5V tolerant (Refer to Figure 15.2 for the port cell circuit.) The Port I/O cells are configured as either push-pull or open-drain in the Port Configuration Registers (PRT0CF, PRT1CF, PRT2CF, PRT3CF). Complete Electrical Specifications for Port I/O are given in Table 15.2.

### 15.1. Priority Cross Bar Decoder

One of the design goals of this MCU family was to make the entire palette of digital resources available to the designer even on reduced pin count packages. The Priority CrossBar Decoder provides an elegant solution to the problem of connecting the internal digital resources to the physical I/O pins.

The Priority CrossBar Decode (Table 15.1) assigns a priority to each I/O function, starting at the top with the SMBus. As the table illustrates, when selected, its two signals will be assigned to Pin 0 and 1 of I/O Port 0. The decoder always fills I/O bits from LSB to MSB starting with Port 0, then Port 1, finishing if necessary with Port 2. If you choose not to use a resource, the next function down on the table will fill the priority slot. In this way it is possible to choose only the functions required by the design, making full use of the available I/O pins. Also, any extra Port I/O are grouped together for more convenient use in application code.

Registers XBR0, XBR1 and XBR2 are used to assign the digital I/O resources to the physical I/O Port pins. It is important to understand that when the SMBus, SPI Bus, or UART is selected, the crossbar assigns all pins associated with the selected bus. It would be impossible for instance to assign the RX pin from the UART function without also assigning the TX function. Standard Port I/Os appear contiguously after the prioritized functions have been assigned. For example, if you choose functions that take the first 14 Port I/O (P0.[7:0], P1.[5:0]), you would have 18 Port I/O left unused by the crossbar (P1.[7:6], P2 and P3).

### 15.2. Port I/O Initialization

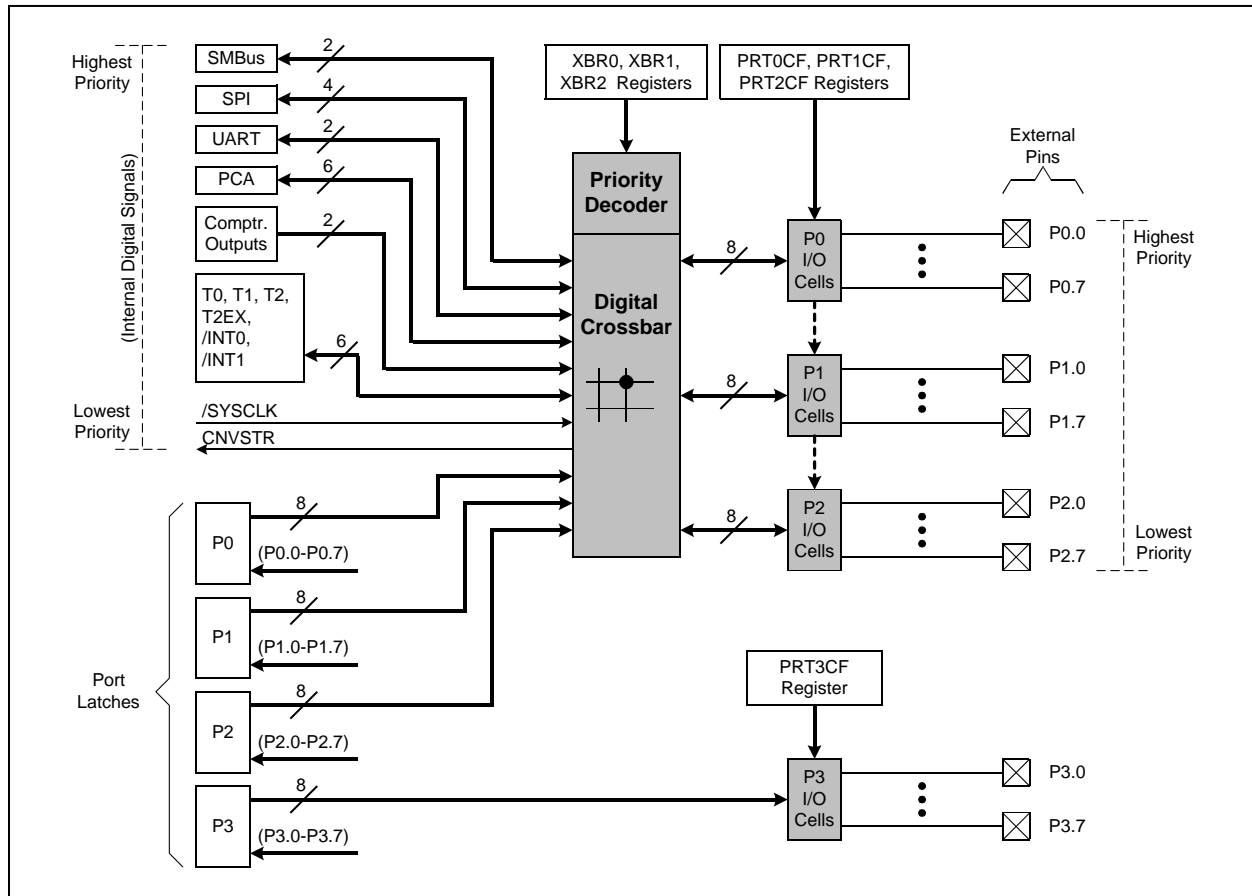
Port I/O initialization is straightforward. Registers XBR0, XBR1 and XBR2 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR2 to 1 enables the CrossBar. **Until the Crossbar is enabled, the external pins remain as standard Ports in input mode regardless of the XBRn Register settings.** For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table; as an alternative, the Code Configuration Wizard function of the IDE software will determine the Port I/O pin-assignments based on the XBRn Register settings.

The output driver characteristics of the I/O pins are defined using the Port Configuration Registers PRT0CF, PRT1CF, PRT2CF and PRT3CF (see Figure 15.7, Figure 15.9, Figure 15.12, and Figure 15.14). Each Port Output driver can be configured as either Open Drain or Push-Pull. This is required even for the digital resources selected in the XBRn registers and is not automatic. The only exception to this is the SMBus (SDA, SCL) and UART Receive (RX, when in mode 0) pins which are Open-drain regardless of the PRTnCF settings. When the WEAKPUD bit in XBR2 is 0, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does

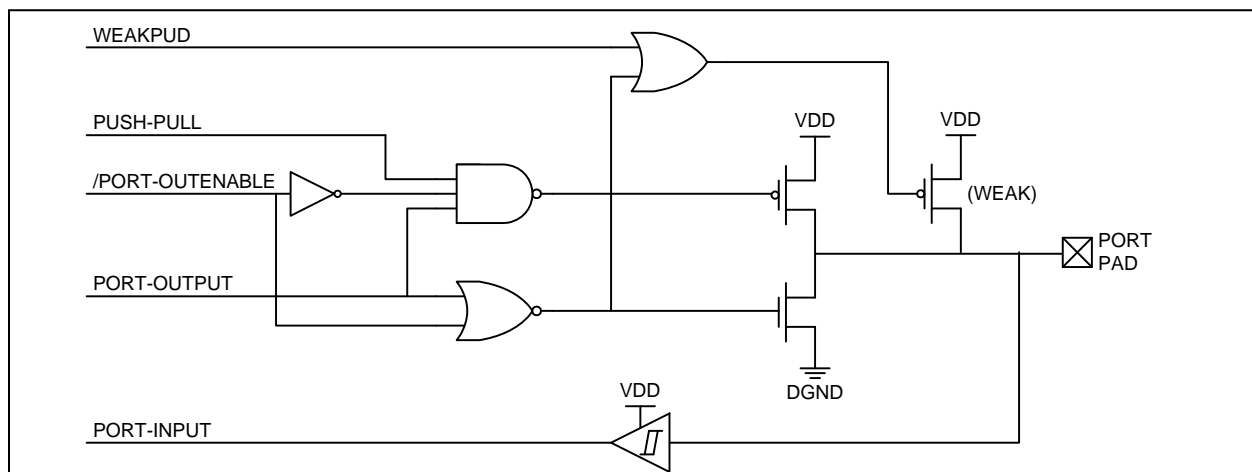
not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an open-drain output that is driving a 0 to avoid unnecessary power dissipation.

The third and final step is to initialize the individual resources selected using the appropriate setup registers. Initialization procedures for the various digital resources may be found in the detailed explanation of each available function. The reset state of each register is shown in the figures that describe each individual register.

**Figure 15.1. Port I/O Functional Block Diagram**



**Figure 15.2. Port I/O Cell Block Diagram**



**Figure 15.11. P2: Port2 Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xA0

Bits7-0: P2.[7:0]  
 (Write – Output appears on I/O pins per XBR0, XBR1, and XBR2 registers)  
 0: Logic Low Output.  
 1: Logic High Output (high-impedance if corresponding PRT2CF.n bit = 0)  
 (Read – Regardless of XBR0, XBR1, and XBR2 Register settings).  
 0: P2.n is logic low.  
 1: P2.n is logic high.

**Figure 15.12. PRT2CF: Port2 Configuration Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA6

Bits7-0: PRT2CF.[7:0]: Output Configuration Bits for P2.7-P2.0 (respectively)  
 0: Corresponding P2.n Output mode is Open-Drain.  
 1: Corresponding P2.n Output mode is Push-Pull.

### 16.6.5. Status Register

The SMB0STA Status register holds an 8-bit status code indicating the current state of the SMBus. There are 28 possible SMBus states, each with a corresponding unique status code. The five most significant bits of the status code vary while the three least-significant bits of a valid status code are fixed at zero when SI = 1. Therefore, all possible status codes are multiples of eight. This facilitates the use of status codes in software as an index used to branch to appropriate service routines (allowing 8 bytes of code to service the state or jump to a more extensive service routine).

For the purposes of user software, the contents of the SMB0STA register is only defined when the SI flag is logic 1. Software should never write to the SMB0STA register. Doing so will yield indeterminate results. The 28 SMBus states, along with their corresponding status codes, are given in Table 16.1.

**Figure 16.8. SMB0STA: SMBus Status Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC1

Bits7-3: STA7-STA3: SMBus Status Code.  
These bits contain the SMBus Status Code. There are 28 possible status codes. Each status code corresponds to a single SMBus state. A valid status code is present in SMB0STA when the SI flag (SMB0CN.3) is set. The content of SMB0STA is not defined when the SI flag is logic 0. Writing to the SMB0STA register at any time will yield indeterminate results.

Bits2-0: STA2-STA0: The three least significant bits of SMB0STA are always read as logic 0 when the SI flag is logic 1.

## 17. SERIAL PERIPHERAL INTERFACE BUS

The Serial Peripheral Interface (SPI) provides access to a four-wire, full-duplex, serial bus. SPI supports the connection of multiple slave devices to a master device on the same bus. A separate slave-select signal (NSS) is used to select a slave device and enable a data transfer between the master and the selected slave. Multiple masters on the same bus are also supported. Collision detection is provided when two or more masters attempt a data transfer at the same time. The SPI can operate as either a master or a slave. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency.

When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

**Figure 17.1. SPI Block Diagram**

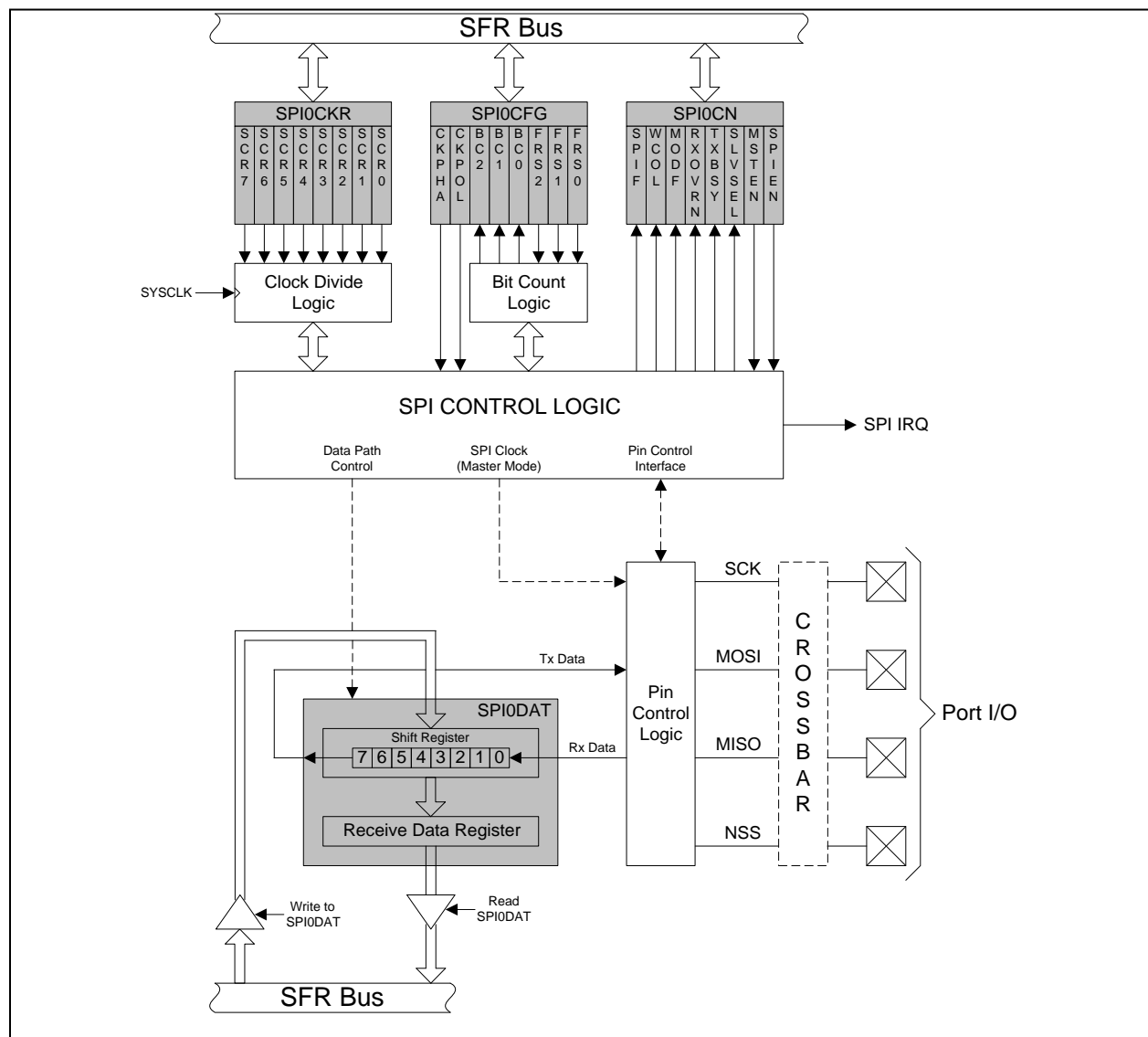
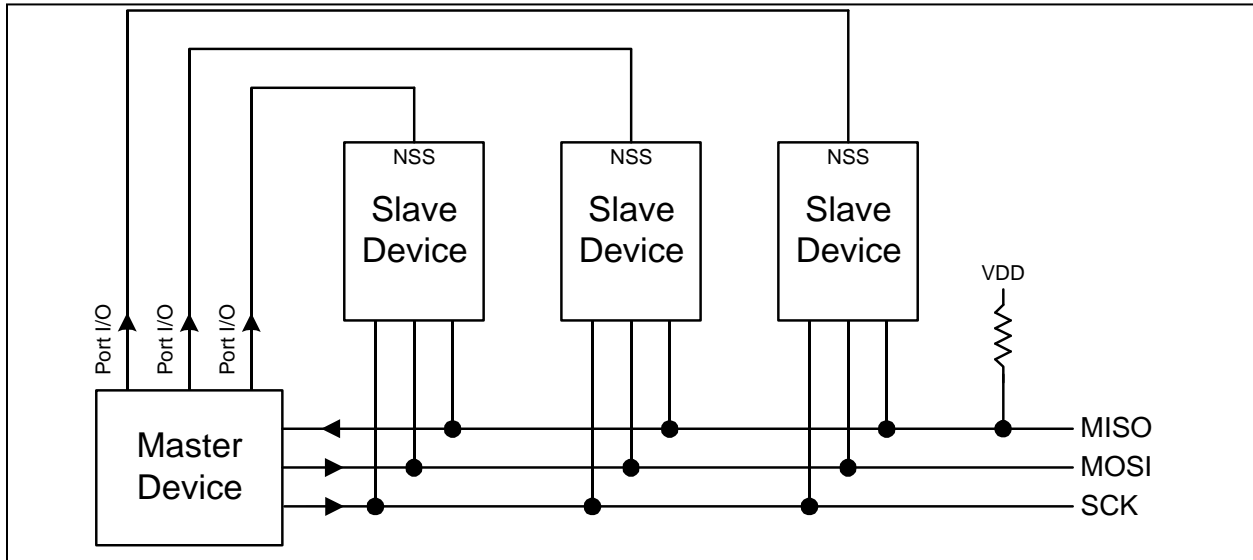




Figure 17.2. Typical SPI Interconnection



### 17.1. Signal Descriptions

The four signals used by the SPI (MOSI, MISO, SCK, NSS) are described below.

#### 17.1.1. Master Out, Slave In

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. Data is transferred most-significant bit first.

#### 17.1.2. Master In, Slave Out

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most-significant bit first. A SPI slave places the MISO pin in a high-impedance state when the slave is not selected.

#### 17.1.3. Serial Clock

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines.

#### 17.1.4. Slave Select

The slave select (NSS) signal is an input used to select the SPI module when in slave mode by a master, or to disable the SPI module when in master mode. When in slave mode, it is pulled low to initiate a data transfer and remains low for the duration of the transfer.

**Figure 19.6. CKCON: Clock Control Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	T2M	T1M	T0M	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8E

Bits7-6: UNUSED. Read = 00b, Write = don't care.

Bit5: T2M: Timer 2 Clock Select.  
This bit controls the division of the system clock supplied to Timer 2. This bit is ignored when the timer is in baud rate generator mode or counter mode (i.e. C/T2 = 1).  
0: Timer 2 uses the system clock divided by 12.  
1: Timer 2 uses the system clock.

Bit4: T1M: Timer 1 Clock Select.  
This bit controls the division of the system clock supplied to Timer 1.  
0: Timer 1 uses the system clock divided by 12.  
1: Timer 1 uses the system clock.

Bit3: T0M: Timer 0 Clock Select.  
This bit controls the division of the system clock supplied to Counter/Timer 0.  
0: Counter/Timer uses the system clock divided by 12.  
1: Counter/Timer uses the system clock.

Bits2-0: Reserved. Read = 000b, Must Write = 000.

## 19.2. Timer 2

Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFRs: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. (Refer to Section 14 for information on selecting and configuring external I/O pins.) Timer 2 can also be used to start an ADC Data Conversion.

Timer 2 offers capabilities not found in Timer 0 and Timer 1. It operates in one of three modes: 16-bit Counter/Timer with Capture, 16-bit Counter/Timer with Auto-Reload or Baud Rate Generator Mode. Timer 2's operating mode is selected by setting configuration bits in the Timer 2 Control (T2CON) register. Below is a summary of the Timer 2 operating modes and the T2CON bits used to configure the counter/timer. Detailed descriptions of each mode follow.

RCLK	TCLK	CP/RL2	TR2	Mode
0	0	1	1	16-bit Counter/Timer with Capture
0	0	0	1	16-bit Counter/Timer with Auto-Reload
0	1	X	1	Baud Rate Generator for TX
1	0	X	1	Baud Rate Generator for RX
1	1	X	1	Baud Rate Generator for TX and RX
X	X	X	0	Off

**Figure 20.10. PCA0CPMn: PCA Capture/Compare Registers**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xDA-0xDE

PCA0CPMn Address: PCA0CPM0 = 0xDA (n = 0)  
PCA0CPM1 = 0xDB (n = 1)  
PCA0CPM2 = 0xDC (n = 2)  
PCA0CPM3 = 0xDD (n = 3)  
PCA0CPM4 = 0xDE (n = 4)

Bit7: UNUSED. Read = 0, Write = don't care.

Bit6: ECOMn: Comparator Function Enable.  
This bit enables/disables the comparator function for PCA module *n*.  
0: Disabled.  
1: Enabled.

Bit5: CAPPn: Capture Positive Function Enable.  
This bit enables/disables the positive edge capture for PCA module *n*.  
0: Disabled.  
1: Enabled.

Bit4: CAPNn: Capture Negative Function Enable.  
This bit enables/disables the negative edge capture for PCA module *n*.  
0: Disabled.  
1: Enabled.

Bit3: MATn: Match Function Enable.  
This bit enables/disables the match function for PCA module *n*. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set.  
0: Disabled.  
1: Enabled.

Bit2: TOGn: Toggle Function Enable.  
This bit enables/disables the toggle function for PCA module *n*. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle.  
0: Disabled.  
1: Enabled.

Bit1: PWMn: Pulse Width Modulation Mode Enable.  
This bit enables/disables the comparator function for PCA module *n*. When enabled, a pulse width modulated signal is output on the CEXn pin.  
0: Disabled.  
1: Enabled.

Bit0: ECCFn: Capture/Compare Flag Interrupt Enable.  
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.  
0: Disable CCFn interrupts.  
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

### **21.3. Debug Support**

Each MCU has on-chip JTAG and debug circuitry that provide *non-intrusive, full speed, in-circuit debug using the production part installed in the end application* using the four pin JTAG I/F. Silicon Labs' debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, and run and halt commands. No additional target RAM, program memory, or communications channels are required. All the digital and analog peripherals are functional and work correctly (remain in sync) while debugging. The WDT is disabled when the MCU is halted during single stepping or at a breakpoint.

The C8051F000DK, C8051F005DK, C8051F010DK, and C8051F015DK are development kits with all the hardware and software necessary to develop application code and perform in-circuit debugging with each MCU in the C8051F000 family. Each kit includes an Integrated Development Environment (IDE) which has a debugger and integrated 8051 assembler. It has an RS-232 to JTAG protocol translator module referred to as the EC. There is also a target application board with a C8051F000, F005, F010, or F015 installed and with a large prototyping area. The kit also includes RS-232 and JTAG cables, and wall-mount power supply.