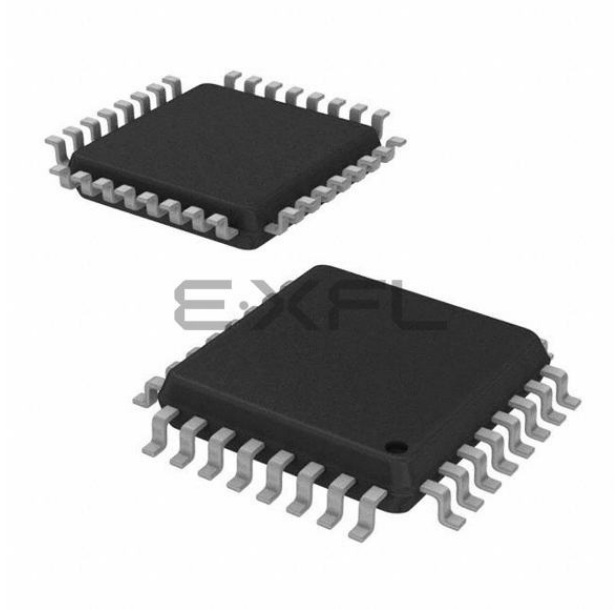

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f002r

Figure 5.3. Temperature Sensor Transfer Function

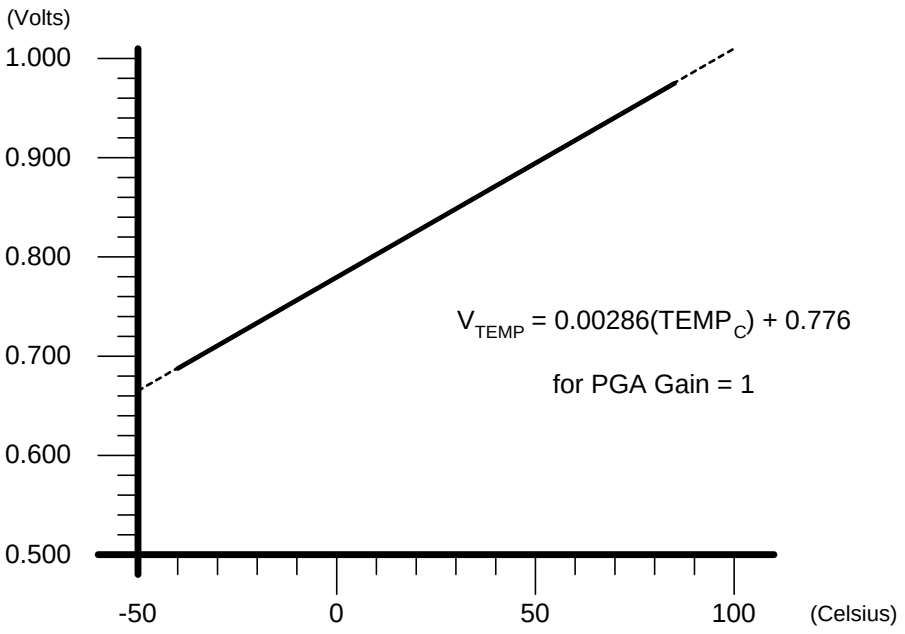


Figure 5.4. AMX0CF: AMUX Configuration Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AIN67IC	AIN45IC	AIN23IC	AIN01IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBA

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bit3: AIN67IC: AIN6, AIN7 Input Pair Configuration Bit
0: AIN6 and AIN7 are independent singled-ended inputs
1: AIN6, AIN7 are (respectively) +, - differential input pair
Bit2: AIN45IC: AIN4, AIN5 Input Pair Configuration Bit
0: AIN4 and AIN5 are independent singled-ended inputs
1: AIN4, AIN5 are (respectively) +, - differential input pair
Bit1: AIN23IC: AIN2, AIN3 Input Pair Configuration Bit
0: AIN2 and AIN3 are independent singled-ended inputs
1: AIN2, AIN3 are (respectively) +, - differential input pair
Bit0: AIN01IC: AIN0, AIN1 Input Pair Configuration Bit
0: AIN0 and AIN1 are independent singled-ended inputs
1: AIN0, AIN1 are (respectively) +, - differential input pair

NOTE: The ADC Data Word is in 2's complement format for channels configured as differential.

Figure 5.5. AMX0SL: AMUX Channel Select Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMXAD3	AMXAD2	AMXAD1	AMXAD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bits3-0: AMXAD3-0: AMUX Address Bits
0000-1111: ADC Inputs selected per chart below

		AMXAD3-0								
		0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1xxx**
AMX0CF BITS 3-0	**0000**	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	AIN6	AIN7	TEMP SENSOR
	0100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	0111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		AIN6	AIN7	TEMP SENSOR
	1000	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1001	+(AIN0) -(AIN1)		AIN2	AIN3	AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1010	AIN0	AIN1	+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1011	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		AIN4	AIN5	+(AIN6) -(AIN7)		TEMP SENSOR
	1100	AIN0	AIN1	AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1101	+(AIN0) -(AIN1)		AIN2	AIN3	+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1110	AIN0	AIN1	+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR
	1111	+(AIN0) -(AIN1)		+(AIN2) -(AIN3)		+(AIN4) -(AIN5)		+(AIN6) -(AIN7)		TEMP SENSOR

Figure 5.6. ADC0CF: ADC Configuration Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCSC2	ADCSC1	ADCSC0	-	-	AMPGN2	AMPGN1	AMPGN0	01100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBC

Bits7-5: ADCSC2-0: ADC SAR Conversion Clock Period Bits
000: SAR Conversion Clock = 1 System Clock
001: SAR Conversion Clock = 2 System Clocks
010: SAR Conversion Clock = 4 System Clocks
011: SAR Conversion Clock = 8 System Clocks
1xx: SAR Conversion Clock = 16 Systems Clocks
(Note: the SAR Conversion Clock should be ≤ 2MHz)
Bits4-3: UNUSED. Read = 00b; Write = don't care
Bits2-0: AMPGN2-0: ADC Internal Amplifier Gain
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
11x: Gain = 0.5

Figure 5.8. ADC0H: ADC Data Word MSB Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBF

Bits7-0: ADC Data Word Bits
For ADLJST = 1: Upper 8-bits of the 12-bit ADC Data Word.
For ADLJST = 0: Bits7-4 are the sign extension of Bit3. Bits 3-0 are the upper 4-bits of the 12-bit ADC Data Word.

Figure 5.9. ADC0L: ADC Data Word LSB Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBE

Bits7-0: ADC Data Word Bits
For ADLJST = 1: Bits7-4 are the lower 4-bits of the 12-bit ADC Data Word. Bits3-0 will always read 0.
For ADLJST = 0: Bits7-0 are the lower 8-bits of the 12-bit ADC Data Word.

NOTE: Resulting 12-bit ADC Data Word appears in the ADC Data Word Registers as follows:
ADC0H[3:0]:ADC0L[7:0], if ADLJST = 0
(ADC0H[7:4] will be sign extension of ADC0H.3 if a differential reading, otherwise = 0000b)

ADC0H[7:0]:ADC0L[7:4], if ADLJST = 1
(ADC0L[3:0] = 0000b)

EXAMPLE: ADC Data Word Conversion Map, AIN0 Input in Single-Ended Mode
(AMX0CF=0x00, AMX0SL=0x00)

AIN0 – AGND (Volts)	**ADC0H:ADC0L** (ADLJST = 0)	**ADC0H:ADC0L** (ADLJST = 1)
REF x (4095/4096)	0x0FFF	0xFFF0
REF x ½	0x0800	0x8000
REF x (2047/4096)	0x07FF	0x7FF0
0	0x0000	0x0000

EXAMPLE: ADC Data Word Conversion Map, AIN0-AIN1 Differential Input Pair
(AMX0CF=0x01, AMX0SL=0x00)

AIN0 – AIN1 (Volts)	**ADC0H:ADC0L** (ADLJST = 0)	**ADC0H:ADC0L** (ADLJST = 1)
REF x (2047/2048)	0x07FF	0x7FF0
0	0x0000	0x0000
-REF x (1/2048)	0xFFFF	0xFFF0
-REF	0xF800	0x8000

5.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Figure 5.14 and Figure 5.15 show example comparisons for reference. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 5.10. ADC0GTH: ADC Greater-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC5

Bits7-0:
The high byte of the ADC Greater-Than Data Word.

Figure 5.11. ADC0GTL: ADC Greater-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC4

Bits7-0:
The low byte of the ADC Greater-Than Data Word.
Definition:
ADC Greater-Than Data Word = ADC0GTH:ADC0GTL

Figure 5.12. ADC0LTH: ADC Less-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC7

Bits7-0:
The high byte of the ADC Less-Than Data Word.

Figure 5.13. ADC0LTL: ADC Less-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC6

Bits7-0:
These bits are the low byte of the ADC Less-Than Data Word.
Definition:
ADC Less-Than Data Word = ADC0LTH:ADC0LTL

Figure 8.2. Comparator Hysteresis Plot

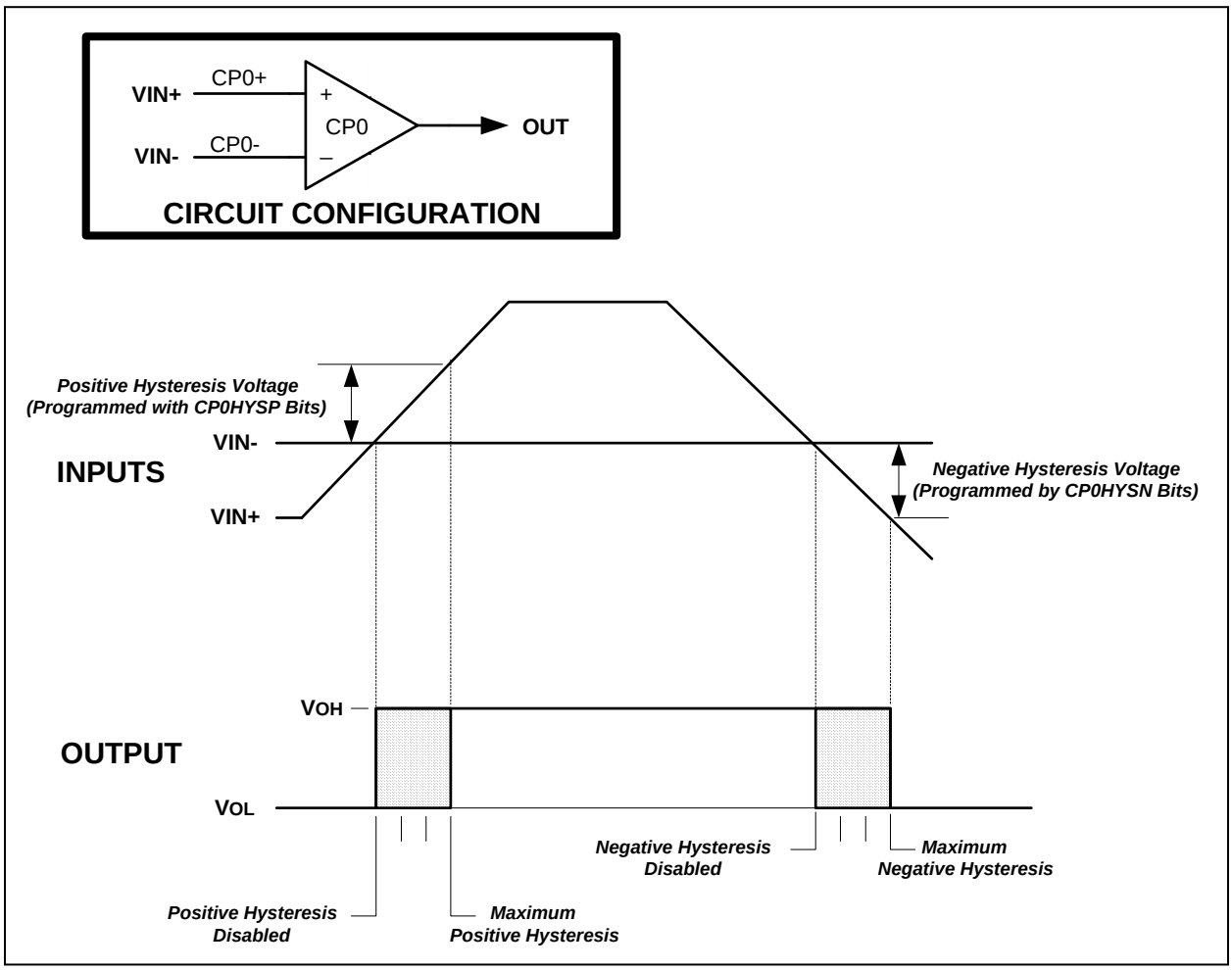


Figure 8.3. CPT0CN: Comparator 0 Control Register

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP1	CP0HYP0	CP0HYN1	CP0HYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9E

Bit7: CP0EN: Comparator 0 Enable Bit
0: Comparator 0 Disabled.
1: Comparator 0 Enabled.

Bit6: CP0OUT: Comparator 0 Output State Flag
0: Voltage on CP0+ < CP0-
1: Voltage on CP0+ > CP0-

Bit5: CP0RIF: Comparator 0 Rising-Edge Interrupt Flag
0: No Comparator 0 Rising-Edge Interrupt has occurred since this flag was cleared
1: Comparator 0 Rising-Edge Interrupt has occurred since this flag was cleared

Bit4: CP0FIF: Comparator 0 Falling-Edge Interrupt Flag
0: No Comparator 0 Falling-Edge Interrupt has occurred since this flag was cleared
1: Comparator 0 Falling-Edge Interrupt has occurred since this flag was cleared

Bit3-2: CP0HYP1-0: Comparator 0 Positive Hysteresis Control Bits
00: Positive Hysteresis Disabled
01: Positive Hysteresis = 2mV
10: Positive Hysteresis = 4mV
11: Positive Hysteresis = 10mV

Bit1-0: CP0HYN1-0: Comparator 0 Negative Hysteresis Control Bits
00: Negative Hysteresis Disabled
01: Negative Hysteresis = 2mV
10: Negative Hysteresis = 4mV
11: Negative Hysteresis = 10mV

Figure 10.10. IP: Interrupt Priority

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PT2	PS	PT1	PX1	PT0	PX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xB8

Bits7-6: UNUSED. Read = 11b, Write = don't care.

Bit5: PT2 Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupts.
0: Timer 2 interrupts set to low priority level.
1: Timer 2 interrupts set to high priority level.

Bit4: PS: Serial Port (UART) Interrupt Priority Control.
This bit sets the priority of the Serial Port (UART) interrupts.
0: UART interrupts set to low priority level.
1: UART interrupts set to high priority level.

Bit3: PT1: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupts.
0: Timer 1 interrupts set to low priority level.
1: Timer 1 interrupts set to high priority level.

Bit2: PX1: External Interrupt 1 Priority Control.
This bit sets the priority of the External Interrupt 1 interrupts.
0: External Interrupt 1 set to low priority level.
1: External Interrupt 1 set to high priority level.

Bit1: PT0: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupts.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.

Bit0: PX0: External Interrupt 0 Priority Control.
This bit sets the priority of the External Interrupt 0 interrupts.
0: External Interrupt 0 set to low priority level.
1: External Interrupt 0 set to high priority level.

Figure 15.13. P3: Port3 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xB0

Bits7-0: P3.[7:0]
(Write)
0: Logic Low Output.
1: Logic High Output (high-impedance if corresponding PRT3CF.n bit = 0)
(Read)
0: P3.n is logic low.
1: P3.n is logic high.

Figure 15.14. PRT3CF: Port3 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA7

Bits7-0: PRT3CF.[7:0]: Output Configuration Bits for P3.7-P3.0 (respectively)
0: Corresponding P3.n Output mode is Open-Drain.
1: Corresponding P3.n Output mode is Push-Pull.

Table 15.2. Port I/O DC Electrical Characteristics

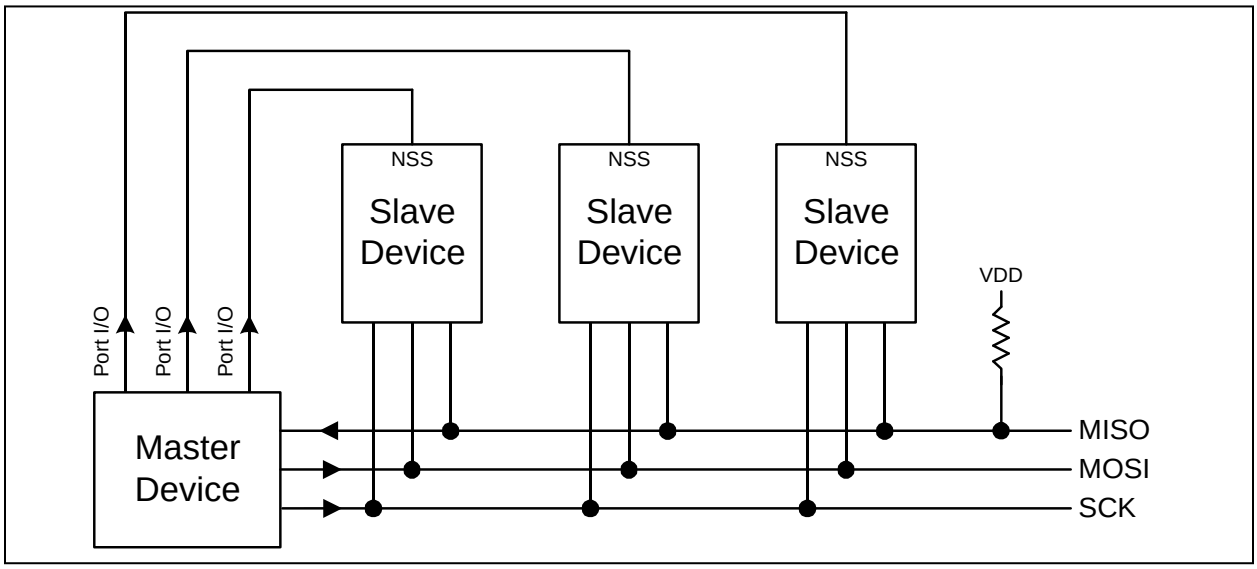
VDD = 2.7 to 3.6V, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	I_{OH} = -10uA, Port I/O push-pull I_{OH} = -3mA, Port I/O push-pull I_{OH} = -10mA, Port I/O push-pull	VDD – 0.1 VDD – 0.7	 VDD – 0.8		V
Output Low Voltage	I_{OL} = 10uA I_{OL} = 8.5mA I_{OL} = 25mA		 1.0	0.1 0.6	V
Input High Voltage		0.7 x VDD			V
Input Low Voltage				0.3 x VDD	V
Input Leakage Current	DGND < Port Pin < VDD, Pin Tri-state Weak Pull-up Off Weak Pull-up On		 30	 ±1	µA
Capacitive Loading			5		pF

Table 16.1. SMBus Status Codes

Status Code (SMB0STA)	Mode	**SMBus State**
0x00	All	Bus Error (i.e. illegal START, illegal STOP, …)
0x08	Master Transmitter/Receiver	START condition transmitted.
0x10	Master Transmitter/Receiver	Repeated START condition transmitted.
0x18	Master Transmitter	Slave address + W transmitted. ACK received.
0x20	Master Transmitter	Slave address + W transmitted. NACK received.
0x28	Master Transmitter	Data byte transmitted. ACK received.
0x30	Master Transmitter	Data byte transmitted. NACK received.
0x38	Master Transmitter	Arbitration lost
0x40	Master Receiver	Slave address + R transmitted. ACK received.
0x48	Master Receiver	Slave address + R transmitted. NACK received
0x50	Master Receiver	Data byte received. ACK transmitted.
0x58	Master Receiver	Data byte received. NACK transmitted.
0x60	Slave Receiver	SMB0's own slave address + W received. ACK transmitted.
0x68	Slave Receiver	Arbitration lost in transmitting slave address + R/W as master. Own slave address + W received. ACK transmitted.
0x70	Slave Receiver	General call address (0x00) received. ACK returned.
0x78	Slave Receiver	Arbitration lost in transmitting slave address + R/W as master. General call address received. ACK transmitted.
0x80	Slave Receiver	SMB0's own slave address + W received. Data byte received. ACK transmitted.
0x88	Slave Receiver	SMB0's own slave address + W received. Data byte received. NACK transmitted.
0x90	Slave Receiver	General call address (0x00) received. Data byte received. ACK transmitted.
0x98	Slave Receiver	General call address (0x00) received. Data byte received. NACK transmitted.
0xA0	Slave Receiver	A STOP or repeated START received while addressed as a slave.
0xA8	Slave Transmitter	SMB0's own slave address + R received. ACK transmitted.
0xB0	Slave Transmitter	Arbitration lost in transmitting slave address + R/W as master. Own slave address + R received. ACK transmitted.
0xB8	Slave Transmitter	Data byte transmitted. ACK received.
0xC0	Slave Transmitter	Data byte transmitted. NACK received.
0xC8	Slave Transmitter	Last data byte transmitted (AA=0). ACK received.
0xD0	Slave Transmitter/Receiver	SCL Clock High Timer per SMB0CR timed out (FTE=1)
0xF8	All	Idle

Figure 17.2. Typical SPI Interconnection



17.1. Signal Descriptions

The four signals used by the SPI (MOSI, MISO, SCK, NSS) are described below.

17.1.1. Master Out, Slave In

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. Data is transferred most-significant bit first.

17.1.2. Master In, Slave Out

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most-significant bit first. A SPI slave places the MISO pin in a high-impedance state when the slave is not selected.

17.1.3. Serial Clock

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines.

17.1.4. Slave Select

The slave select (NSS) signal is an input used to select the SPI module when in slave mode by a master, or to disable the SPI module when in master mode. When in slave mode, it is pulled low to initiate a data transfer and remains low for the duration of the transfer.

Figure 18.9. SCON: Serial Port Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0x98

Bits7-6: SM0-SM1: Serial Port Operation Mode.
These bits select the Serial Port Operation Mode.

SM0	SM1	Mode
0	0	Mode 0: Synchronous Mode
0	1	Mode 1: 8-Bit UART, Variable Baud Rate
1	0	Mode 2: 9-Bit UART, Fixed Baud Rate
1	1	Mode 3: 9-Bit UART, Variable Baud Rate

Bit5: SM2: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port Operation Mode.
Mode 0: No effect
Mode 1: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI will only be activated if stop bit is logic level 1.
Mode 2 and 3: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI is set and an interrupt is generated only when the ninth bit is logic 1.

Bit4: REN: Receive Enable.
This bit enables/disables the UART receiver.
0: UART reception disabled.
1: UART reception enabled.

Bit3: TB8: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in Modes 2 and 3. It is not used in Modes 0 and 1. Set or cleared by software as required.

Bit2: RB8: Ninth Receive Bit.
The bit is assigned the logic level of the ninth bit received in Modes 2 and 3. In Mode 1, if SM2 is logic 0, RB8 is assigned the logic level of the received stop bit. RB8 is not used in Mode 0.

Bit1: TI: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by the UART (after the 8th bit in Mode 0, or at the beginning of the stop bit in other modes). When the UART interrupt is enabled, setting this bit causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software

Bit0: RI: Receive Interrupt Flag.
Set by hardware when a byte of data has been received by the UART (after the 8th bit in Mode 0, or after the stop bit in other modes – see SM2 bit for exception). When the UART interrupt is enabled, setting this bit causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software.

19.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

Timer 0 and Timer 1 behave differently in Mode 3. Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. It can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3, so with Timer 0 in Mode 3, Timer 1 can be turned off and on by switching it into and out of its Mode 3. When Timer 0 is in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used for baud rate generation. Refer to Section 18 (UART) for information on configuring Timer 1 for baud rate generation.

Figure 19.3. T0 Mode 3 Block Diagram

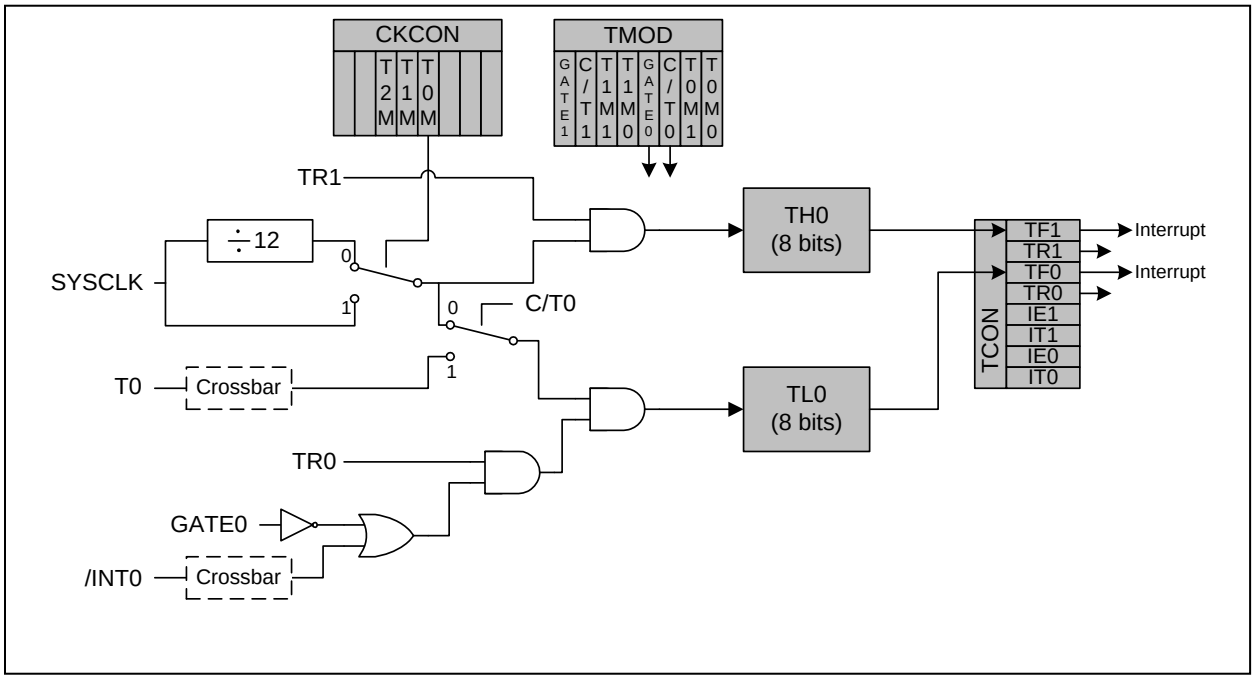


Figure 19.15. RCAP2L: Timer 2 Capture Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xCA

Bits 7-0: RCAP2L: Timer 2 Capture Register Low Byte.
The RCAP2L register captures the low byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is configured in auto-reload mode, it holds the low byte of the reload value.

Figure 19.16. RCAP2H: Timer 2 Capture Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xCB

Bits 7-0: RCAP2H: Timer 2 Capture Register High Byte.
The RCAP2H register captures the high byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is configured in auto-reload mode, it holds the high byte of the reload value.

Figure 19.17. TL2: Timer 2 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xCC

Bits 7-0: TL2: Timer 2 Low Byte.
The TL2 register contains the low byte of the 16-bit Timer 2.

Figure 19.18. TH2: Timer 2 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xCD

Bits 7-0: TH2: Timer 2 High Byte.
The TH2 register contains the high byte of the 16-bit Timer 2.

Figure 20.9. PCA0MD: PCA Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CIDL	-	-	-	-	CPS1	CPS0	ECF	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xD9

Bit7: CIDL: PCA Counter/Timer Idle Control.
Specifies PCA behavior when CPU is in Idle Mode.
0: PCA continues to function normally while the system controller is in Idle Mode.
1: PCA operation is suspended while the system controller is in Idle Mode.

Bits6-3: UNUSED. Read = 0000b, Write = don't care.

Bits2-1: CPS1-CPS0: PCA Counter/Timer Pulse Select.
These bits select the timebase source for the PCA counter.

CPS1	CPS0	Timebase
0	0	System clock divided by 12
0	1	System clock divided by 4
1	0	Timer 0 overflow
1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)

Bit0: ECF: PCA Counter/Timer Overflow Interrupt Enable.
This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.
0: Disable the CF interrupt.
1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.

21.1.1. EXTEST Instruction

The EXTEST instruction is accessed via the IR. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature. All inputs to on-chip logic are set to one.

21.1.2. SAMPLE Instruction

The SAMPLE instruction is accessed via the IR. The Boundary DR provides observability and presetting of the scan-path latches.

21.1.3. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard 1-bit JTAG Bypass data register.

21.1.4. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

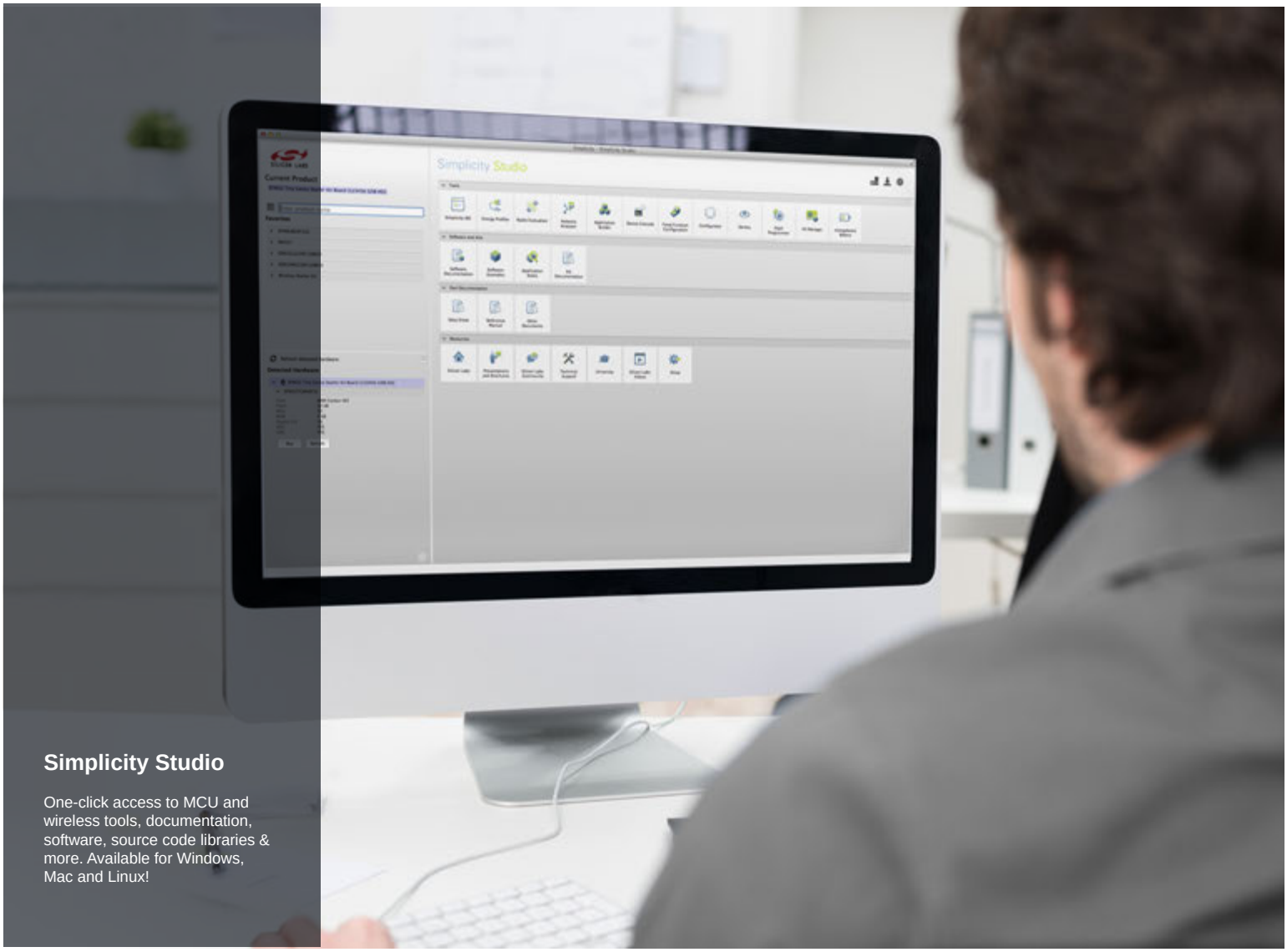
Figure 21.2. DEVICEID: JTAG Device ID Register

Version	Part Number	Manufacturer ID	1	Reset Value (Varies)
Bit31 Bit28	Bit27 Bit12	Bit11 Bit1	Bit0	

Version = 0000b (Revision A) or
= 0001b (Revision B)

Part Number = 0000 0000 0000 0000b or
= 0000 0000 0000 0010b

Manufacturer ID = 0010 0100 001b (Silicon Laboratories)



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