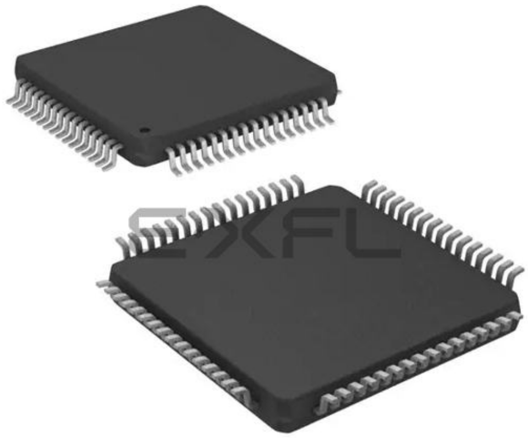
Silicon Labs - C8051F010R Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f010r

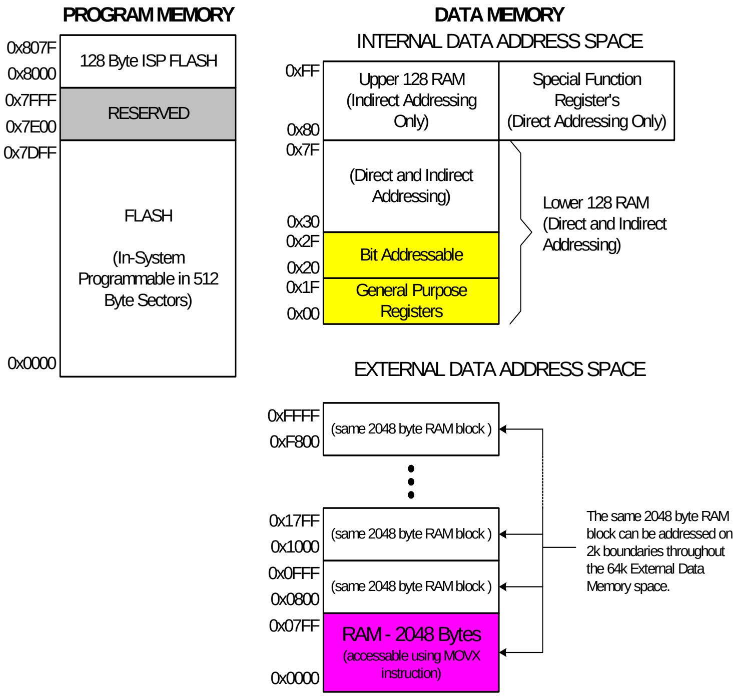
1.2. On-Board Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general-purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F005/06/07/15/16/17 MCUs additionally has a 2048 byte RAM block in the external data memory address space. This 2048 byte block can be addressed over the entire 64k external data memory address range (see Figure 1.6).

The MCU's program memory consists of 32k + 128 bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See Figure 1.6 for the MCU system memory map.

Figure 1.6. On-Board Memory Map


PROGRAM MEMORY
0x807F
0x8000
128 Byte ISP FLASH
0x7FFF
0x7E00
RESERVED
0x7DFF
FLASH
(In-System Programmable in 512 Byte Sectors)
0x0000
DATA MEMORY
INTERNAL DATA ADDRESS SPACE
0xFF
0x80
Upper 128 RAM (Indirect Addressing Only)
Special Function Register's (Direct Addressing Only)
0x7F
(Direct and Indirect Addressing)
0x30
0x2F
Bit Addressable
0x20
0x1F
General Purpose Registers
0x00
Lower 128 RAM (Direct and Indirect Addressing)
EXTERNAL DATA ADDRESS SPACE
0xFFFF
0xF800
(same 2048 byte RAM block)
0x17FF
0x1000
(same 2048 byte RAM block)
0x0FFF
0x0800
(same 2048 byte RAM block)
0x07FF
0x0000
RAM - 2048 Bytes
(accessable using MOVX instruction)
The same 2048 byte RAM block can be addressed on 2k boundaries throughout the 64k External Data Memory space.

5.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Figure 5.14 and Figure 5.15 show example comparisons for reference. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 5.10. ADC0GTH: ADC Greater-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC5

Bits7-0:
The high byte of the ADC Greater-Than Data Word.

Figure 5.11. ADC0GTL: ADC Greater-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC4

Bits7-0:
The low byte of the ADC Greater-Than Data Word.
Definition:
ADC Greater-Than Data Word = ADC0GTH:ADC0GTL

Figure 5.12. ADC0LTH: ADC Less-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC7

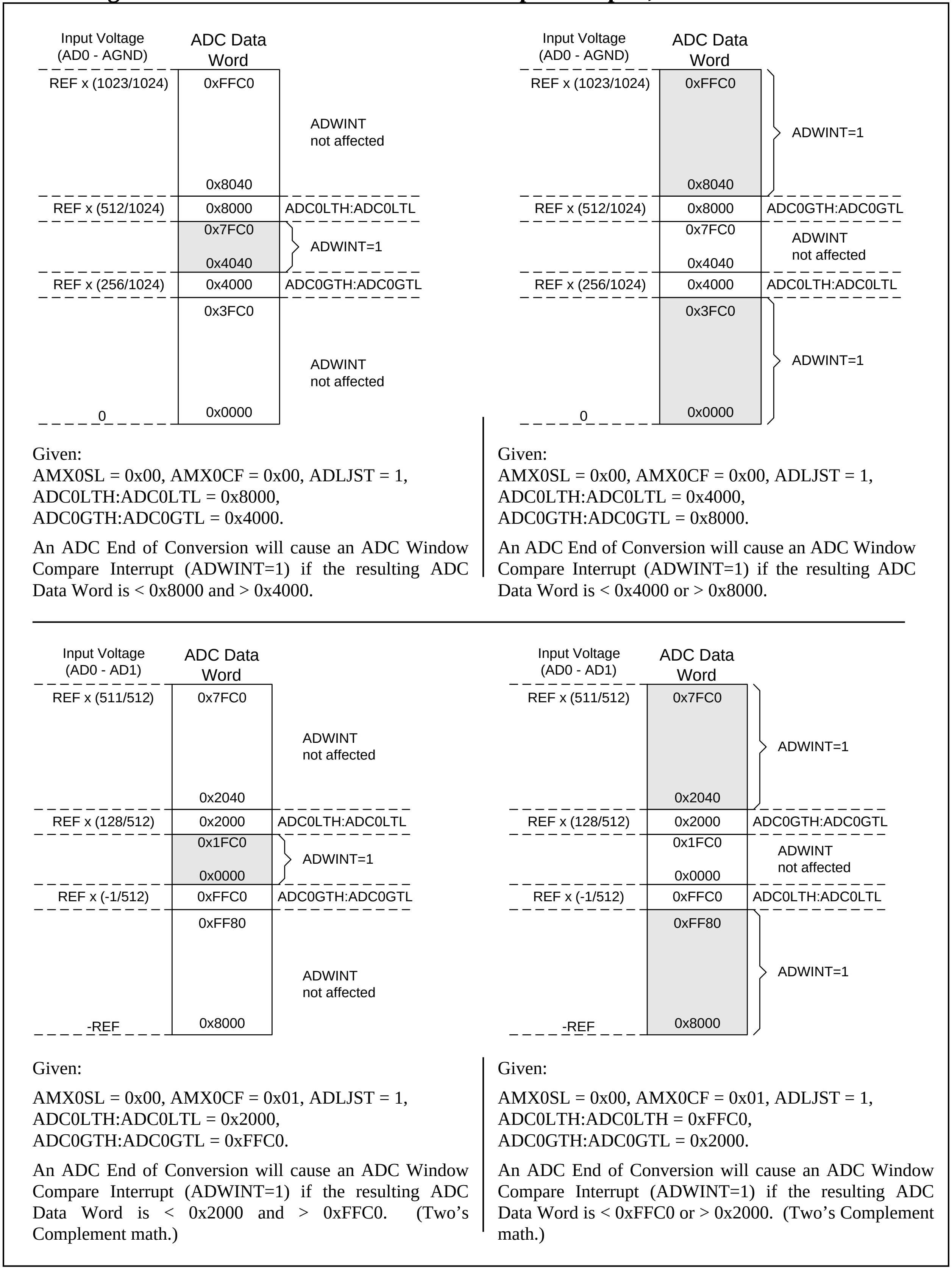
Bits7-0:
The high byte of the ADC Less-Than Data Word.

Figure 5.13. ADC0LTL: ADC Less-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC6

Bits7-0:
These bits are the low byte of the ADC Less-Than Data Word.
Definition:
ADC Less-Than Data Word = ADC0LTH:ADC0LTL

Figure 6.15. 10-Bit ADC Window Interrupt Examples, Left Justified Data



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x8000,
ADC0GTH:ADC0GTL = 0x4000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x8000 and > 0x4000.

Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x4000,
ADC0GTH:ADC0GTL = 0x8000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x4000 or > 0x8000.

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x2000,
ADC0GTH:ADC0GTL = 0xFFC0.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0xFFC0. (Two's Complement math.)

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,
ADC0LTH:ADC0LTH = 0xFFC0,
ADC0GTH:ADC0GTL = 0x2000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFC0 or > 0x2000. (Two's Complement math.)

Figure 7.5. DAC1H: DAC1 High Byte Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xD6

Bits7-0: DAC1 Data Word Most Significant Byte.

Figure 7.6. DAC1L: DAC1 Low Byte Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xD5

Bits7-0: DAC1 Data Word Least Significant Byte.

Figure 7.7. DAC1CN: DAC1 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DAC1EN	-	-	-	-	DAC1DF2	DAC1DF1	DAC1DF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xD7

Bit7: DAC1EN: DAC1 Enable Bit
0: DAC1 Disabled. DAC1 Output pin is disabled; DAC1 is in low power shutdown mode.
1: DAC1 Enabled. DAC1 Output is pin active; DAC1 is operational.
Bits6-3: UNUSED. Read = 0000b; Write = don’t care
Bits2-0: DAC1DF2-0: DAC1 Data Format Bits
000: The most significant nybble of the DAC1 Data Word is in DAC1H[3:0], while the least significant byte is in DAC1L.

DAC1H								DAC1L							
▨	▨	▨	▨	MSB											LSB

001: The most significant 5-bits of the DAC1 Data Word is in DAC1H[4:0], while the least significant 7-bits is in DAC1L[7:1].

DAC1H								DAC1L							
▨	▨	▨	MSB											LSB	▨

010: The most significant 6-bits of the DAC1 Data Word is in DAC1H[5:0], while the least significant 6-bits is in DAC1L[7:2].

DAC1H								DAC1L							
▨	▨	MSB											LSB	▨	▨

011: The most significant 7-bits of the DAC1 Data Word is in DAC1H[6:0], while the least significant 5-bits is in DAC1L[7:3].

DAC1H								DAC1L							
▨	MSB											LSB	▨	▨	▨

1xx: The most significant byte of the DAC1 Data Word is in DAC1H, while the least significant nybble is in DAC1L[7:4].

DAC1H								DAC1L							
MSB											LSB	▨	▨	▨	▨

register configured for accessing the external data memory space. Refer to Section 11 (Flash Memory) for further details.

Figure 10.6. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xD0

Bit7: CY: Carry Flag.
This bit is set when the last arithmetic operation results in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: AC: Auxiliary Carry Flag.
This bit is set when the last arithmetic operation results in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: F0: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits4-3: RS1-RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00-0x07
0	1	1	0x08-0x0F
1	0	2	0x10-0x17
1	1	3	0x18-0x1F

Note: Any instruction which changes the RS1-RS0 bits must not be immediately followed by the “MOV Rn, A” instruction.

Bit2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:

- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255) .
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: PARITY: Parity Flag.
(Read only)
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

10.5. Power Management Modes

The CIP-51 core has two software programmable power management modes: Idle and Stop. Idle mode halts the CPU while leaving the external peripherals and internal clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the system clock is stopped. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power. Figure 10.15 describes the Power Control Register (PCON) used to control the CIP-51's power management modes.

Although the CIP-51 has Idle and Stop modes built in (as with any standard 8051 architecture), power management of the entire MCU is better accomplished by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and put into low power mode. Digital peripherals, such as timers or serial buses, draw little power whenever they are not in use. Turning off the oscillator saves even more power, but requires a reset to restart the MCU.

10.5.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt or /RST is asserted. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU will resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Any instructions that set the IDLE bit should be followed by an instruction that has 2 or more op-code bytes, for example:

```
// in 'C':
PCON |= 0x01;           // set IDLE bit
PCON  = PCON;           // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL   PCON,  #01h       ; set IDLE bit
MOV  PCON,  PCON        ; ... followed by a 3-cycle dummy instruction
```

If enabled, the WDT will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section 13.8 Watchdog Timer for more information on the use and configuration of the WDT.

10.5.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes. In Stop mode, the CPU and oscillators are stopped, effectively shutting down all digital peripherals. Each analog peripheral must be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to sleep for longer than the MCD timeout of 100µsec.

Figure 10.15. PCON: Power Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x87

Bit7: SMOD: Serial Port Baud Rate Doubler Enable.
0: Serial Port baud rate is that defined by Serial Port Mode in SCON.
1: Serial Port baud rate is double that defined by Serial Port Mode in SCON.

Bits6-2: GF4-GF0: General Purpose Flags 4-0.
These are general purpose flags for use under software control.

Bit1: STOP: Stop Mode Select.
Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
1: Goes into power down mode. (Turns off internal oscillator).

Bit0: IDLE: Idle Mode Select.
Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.
1: Goes into idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

Figure 11.4. FLSCL: Flash Memory Timing Prescaler

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FOSE	FRAE	-	-	FLASCL				10001111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB6

Bit7: FOSE: Flash One-Shot Timer Enable
0: Flash One-shot timer disabled.
1: Flash One-shot timer enabled

Bit6: FRAE: Flash Read Always Enable
0: Flash reads per one-shot timer
1: Flash always in read mode

Bits5-4: UNUSED. Read = 00b, Write = don’t care.

Bits3-0: FLASCL: Flash Memory Timing Prescaler.
This register specifies the prescaler value for a given system clock required to generate the correct timing for Flash write/erase operations. If the prescaler is set to 1111b, Flash write/erase operations are disabled.
0000: System Clock < 50kHz
0001: 50kHz ≤ System Clock < 100kHz
0010: 100kHz ≤ System Clock < 200kHz
0011: 200kHz ≤ System Clock < 400kHz
0100: 400kHz ≤ System Clock < 800kHz
0101: 800kHz ≤ System Clock < 1.6MHz
0110: 1.6MHz ≤ System Clock < 3.2MHz
0111: 3.2MHz ≤ System Clock < 6.4MHz
1000: 6.4MHz ≤ System Clock < 12.8MHz
1001: 12.8MHz ≤ System Clock < 25.6MHz
1010: 25.6MHz ≤ System Clock < 51.2MHz *
1011, 1100, 1101, 1110: Reserved Values
1111: Flash Memory Write/Erase Disabled

The prescaler value is the smallest value satisfying the following equation:
FLASCL > $\log_2$(System Clock / 50kHz)

* For test purposes. The C8051F000 family is not guaranteed for operation over 25MHz.

13. RESET SOURCES

The reset circuitry of the MCUs allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the CIP-51 halts program execution, forces the external port pins to a known state and initializes the SFRs to their defined reset values. Interrupts and timers are disabled. On exit, the program counter (PC) is reset, and program execution starts at location 0x0000.

All of the SFRs are reset to predefined values. The reset values of the SFR bits are defined in the SFR detailed descriptions. The contents of internal data memory are not changed during a reset and any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic ones), activating internal weak pull-ups which take the external I/O pins to a high state. The weak pull-ups are enabled during and after the reset. If the source of reset is from the VDD Monitor or writing a 1 to PORSF, the /RST pin is driven low until the end of the VDD reset timeout.

On exit from the reset state, the MCU uses the internal oscillator running at 2MHz as the system clock by default. Refer to Section 14 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval. (Section 13.8 details the use of the Watchdog Timer.)

There are seven sources for putting the MCU into the reset state: power-on/power-fail, external /RST pin, external CNVSTR signal, software commanded, Comparator 0, Missing Clock Detector, and Watchdog Timer. Each reset source is described below:

Figure 13.1. Reset Sources Diagram

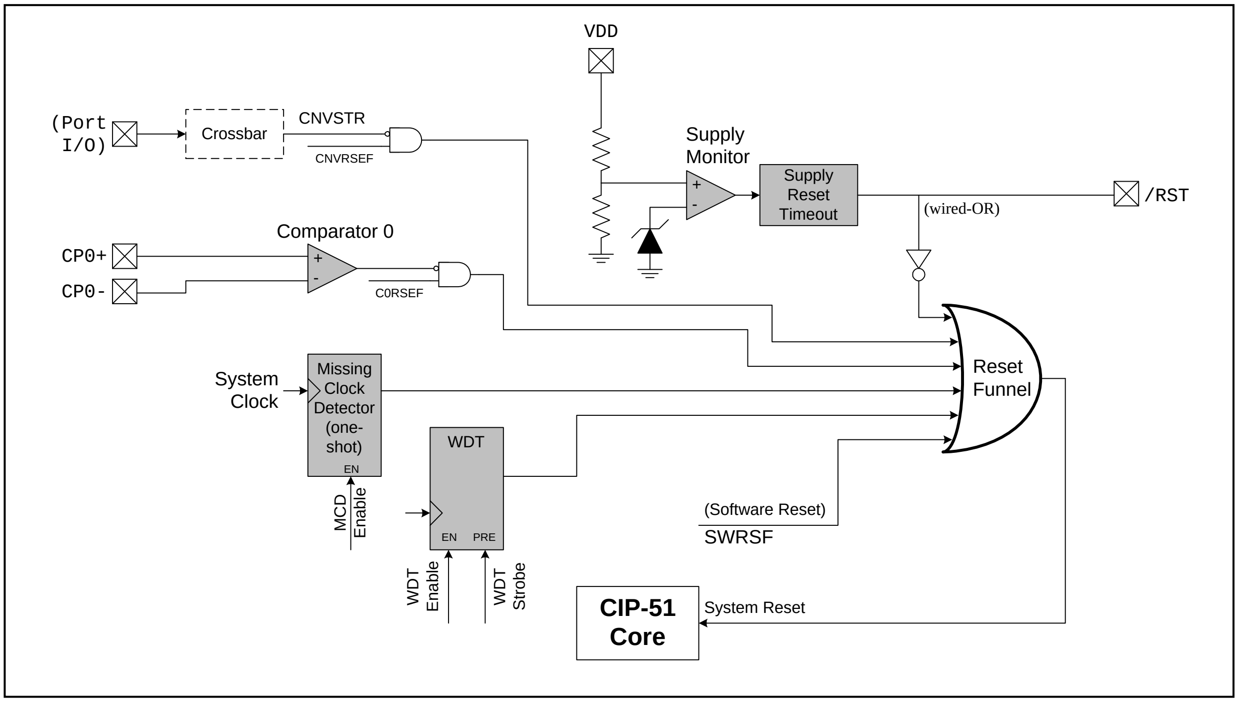


Figure 13.4. RSTSRC: Reset Source Register

R	R/W	R/W	R/W	R	R	R/W	R	Reset Value
JTAGRST	CNVRSEF	C0RSEF	SWRSEF	WDTRSF	MCDRSF	PORSF	PINRSF	xxxxxxxx
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xEF

(Note: Do not use read-modify-write operations on this register.)

Bit7: JTAGRST. JTAG Reset Flag.
0: JTAG is not currently in reset state.
1: JTAG is in reset state.

Bit6: CNVRSEF: Convert Start Reset Source Enable and Flag
Write
0: CNVSTR is not a reset source
1: CNVSTR is a reset source (active low)
Read
0: Source of prior reset was not from CNVSTR
1: Source of prior reset was from CNVSTR

Bit5: C0RSEF: Comparator 0 Reset Enable and Flag
Write
0: Comparator 0 is not a reset source
1: Comparator 0 is a reset source (active low)
Read
Note: The value read from C0RSEF is not defined if Comparator 0 has not been enabled as a reset source.
0: Source of prior reset was not from Comparator 0
1: Source of prior reset was from Comparator 0

Bit4: SWRSF: Software Reset Force and Flag
Write
0: No Effect
1: Forces an internal reset. /RST pin is not effected.
Read
0: Prior reset source was not from write to the SWRSF bit.
1: Prior reset source was from write to the SWRSF bit.

Bit3: WDTRSF: Watchdog Timer Reset Flag
0: Source of prior reset was not from WDT timeout.
1: Source of prior reset was from WDT timeout.

Bit2: MCDRSF: Missing Clock Detector Flag
0: Source of prior reset was not from Missing Clock Detector timeout.
1: Source of prior reset was from Missing Clock Detector timeout.

Bit1: PORSF: Power-On Reset Force and Flag
Write
0: No effect
1: Forces a Power-On Reset. /RST is driven low.
Read
0: Source of prior reset was not from POR.
1: Source of prior reset was from POR.

Bit0: PINRSF: HW Pin Reset Flag
0: Source of prior reset was not from /RST pin.
1: Source of prior reset was from /RST pin.

Figure 15.4. XBR1: Port I/O CrossBar Register 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SYSCKE	T2EXE	T2E	INT1E	T1E	INT0E	T0E	CP1OEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE2

Bit7: SYSCKE: SYSCLK Output Enable Bit
0: SYSCLK unavailable at Port pin.
1: SYSCLK output routed to Port Pin.

Bit6: T2EXE: T2EX Enable Bit
0: T2EX unavailable at Port pin.
1: T2EX routed to Port Pin.

Bit5: T2E: T2 Enable Bit
0: T2 unavailable at Port pin.
1: T2 routed to Port Pin.

Bit4: INT1E: /INT1 Enable Bit
0: /INT1 unavailable at Port pin.
1: /INT1 routed to Port Pin.

Bit3: T1E: T1 Enable Bit
0: T1 unavailable at Port pin.
1: T1 routed to Port Pin.

Bit2: INT0E: /INT0 Enable Bit
0: /INT0 unavailable at Port pin.
1: /INT0 routed to Port Pin.

Bit1: T0E: T0 Enable Bit
0: T0 unavailable at Port pin.
1: T0 routed to Port Pin.

Bit0: CP1OEN: Comparator 1 Output Enable Bit
0: CP1 unavailable at Port pin.
1: CP1 routed to Port Pin.

16.6.1. Control Register

The SMBus Control register SMB0CN is used to configure and control the SMBus interface. All of the bits in the register can be read or written by software. Two of the control bits are also affected by the SMBus hardware. The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by the hardware when a valid serial interrupt condition occurs. It can only be cleared by software. The Stop flag (STO, SMB0CN.4) is cleared to logic 0 by hardware when a STOP condition is present on the bus.

Setting the ENSMB flag to logic 1 enables the SMBus interface. Clearing the ENSMB flag to logic 0 disables the SMBus interface and removes it from the bus. Momentarily clearing the ENSMB flag and then resetting it to logic 1 will reset a SMBus communication. However, ENSMB should not be used to temporarily remove a device from the bus since the bus state information will be lost. Instead, the Assert Acknowledge (AA) flag should be used to temporarily remove the device from the bus (see description of AA flag below).

Setting the Start flag (STA, SMB0CN.5) to logic 1 will put the SMBus in a master mode. If the bus is free, the SMBus hardware will generate a START condition. If the bus is not free, the SMBus hardware waits for a STOP condition to free the bus and then generates a START condition after a 5µs delay per the SMB0CR value. (In accordance with the SMBus protocol, the SMBus interface also considers the bus free if the bus is idle for 50µs and no STOP condition was recognized.) If STA is set to logic 1 while the SMBus is in master mode and one or more bytes have been transferred, a repeated START condition will be generated. To ensure proper operation, the STO flag should be explicitly cleared before setting STA to a logic 1.

When the Stop flag (STO, SMB0CN.4) is set to logic 1 while the SMBus interface is in master mode, the hardware generates a STOP condition on the SMBus. In a slave mode, the STO flag may be used to recover from an error condition. In this case, a STOP condition is not generated on the SMBus, but the SMBus hardware behaves as if a STOP condition has been received and enters the “not addressed” slave receiver mode. The SMBus hardware automatically clears the STO flag to logic 0 when a STOP condition is detected on the bus.

The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by hardware when the SMBus interface enters one of 27 possible states. If interrupts are enabled for the SMBus interface, an interrupt request is generated when the SI flag is set. The SI flag must be cleared by software. While SI is set to logic 1, the clock-low period of the serial clock will be stretched and the serial transfer is suspended.

The Assert Acknowledge flag (AA, SMB0CN.2) is used to set the level of the SDA line during the acknowledge clock cycle on the SCL line. Setting the AA flag to logic 1 will cause an ACKNOWLEDGE (low level on SDA) to be sent during the acknowledge cycle if the device has been addressed. Setting the AA flag to logic 0 will cause a NOT ACKNOWLEDGE (high level on SDA) to be sent during acknowledge cycle. After the transmission of a byte in slave mode, the slave can be temporarily removed from the bus by clearing the AA flag. The slave’s own address and general call address will be ignored. To resume operation on the bus, the AA flag must be reset to logic 1 to allow the slave’s address to be recognized.

Setting the SMBus Free Timer Enable bit (FTE, SMB0CN.1) to logic 1 enables the SMBus Free Timeout feature. If SCL and SDA remain high for the SMBus Free Timeout given in the SMBus Clock Rate Register (Figure 16.5), the bus will be considered free and a Start will be generated if pending. The bus free period should be greater than 50µs.

Setting the SMBus timeout enable bit (TOE, SMB0CN.0) to logic 1 enables Timer 3 to count up when the SCL line is low and Timer 3 is enabled. If Timer 3 overflows, a Timer 3 interrupt will be generated, which will alert the CPU that a SMBus SCL low timeout has occurred.

18.1.3. Mode 2: 9-Bit UART, Fixed Baud Rate

Mode 2 provides asynchronous, full-duplex communication using a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit (see timing diagram in Figure 18.6). On transmit, the ninth data bit is determined by the value in TB8 (SCON.3). It can be assigned the value of the parity flag P in the PSW or used in multiprocessor communications. On receive, the ninth data bit goes into RB8 (SCON.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: RI must be logic 0, and if SM2 is logic 1, the 9th bit must be logic 1.

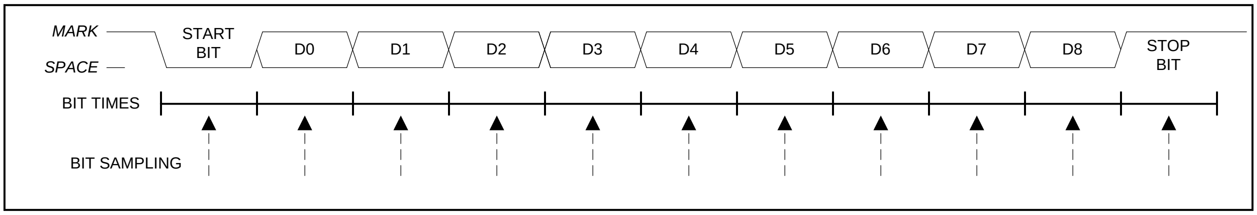
If these conditions are met, the eight bits of data are stored in SBUF, the ninth bit is stored in RB8 and the RI flag is set. If these conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set. An interrupt will occur if enabled when either TI or RI are set.

The baud rate in Mode 2 is a direct function of the system clock frequency as follows:

$$\textit{Mode 2 Baud Rate} = 2^{SMOD} * (SYSCLK / 64).$$

The SMOD bit (PCON.7) selects whether to divide SYSCLK by 32 or 64. In the formula, 2 is raised to the power SMOD, resulting in a baud rate of either 1/32 or 1/64 of the system clock frequency. On reset, the SMOD bit is logic 0, thus selecting the lower speed baud rate by default.

Figure 18.6. UART Modes 2 and 3 Timing Diagram



18.1.4. Mode 3: 9-Bit UART, Variable Baud Rate

Mode 3 is the same as Mode 2 in all respects except the baud rate is variable. The baud rate is determined in the same manner as for Mode 1. Mode 3 operation transmits 11 bits: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. Timer 1 or Timer 2 overflows generate the baud rate just as with Mode 1. In summary, Mode 3 transmits using the same protocol as Mode 2 but with Mode 1 baud rate generation.

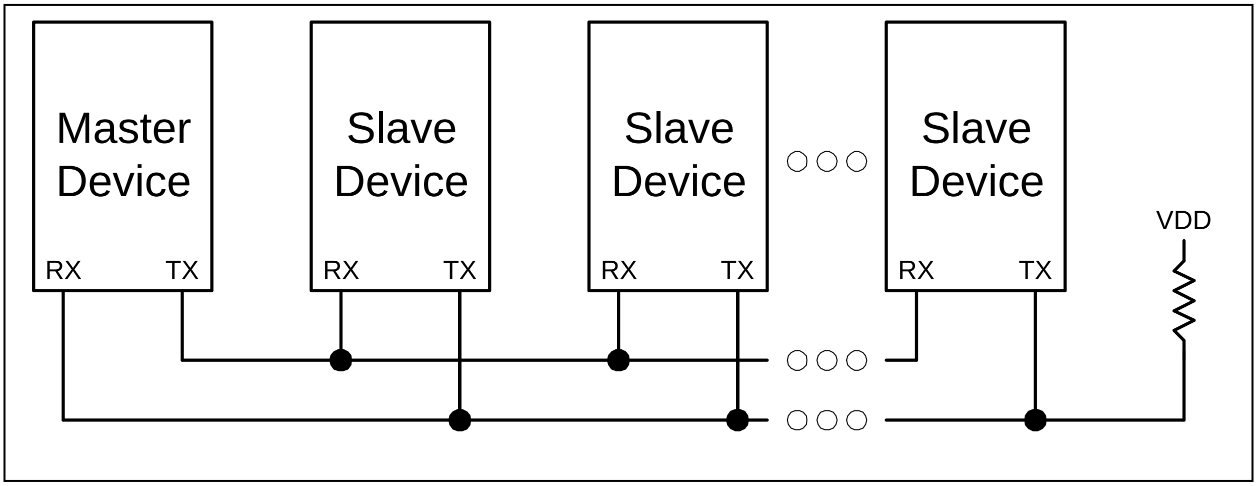
18.2. Multiprocessor Communications

Modes 2 and 3 support multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the SM2 bit (SCON.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic one (RB8 = 1) signifying an address byte has been received. In the UART's interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its SM2 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their SM2 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its SM2 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

Figure 18.7. UART Multi-Processor Mode Interconnect Diagram



19.2. Timer 2

Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFRs: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. (Refer to Section 14 for information on selecting and configuring external I/O pins.) Timer 2 can also be used to start an ADC Data Conversion.

Timer 2 offers capabilities not found in Timer 0 and Timer 1. It operates in one of three modes: 16-bit Counter/Timer with Capture, 16-bit Counter/Timer with Auto-Reload or Baud Rate Generator Mode. Timer 2's operating mode is selected by setting configuration bits in the Timer 2 Control (T2CON) register. Below is a summary of the Timer 2 operating modes and the T2CON bits used to configure the counter/timer. Detailed descriptions of each mode follow.

RCLK	TCLK	CP/RL2	TR2	Mode
0	0	1	1	16-bit Counter/Timer with Capture
0	0	0	1	16-bit Counter/Timer with Auto-Reload
0	1	X	1	Baud Rate Generator for TX
1	0	X	1	Baud Rate Generator for RX
1	1	X	1	Baud Rate Generator for TX and RX
X	X	X	0	Off

Figure 19.14. T2CON: Timer 2 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xC8

Bit7: TF2: Timer 2 Overflow Flag.
Set by hardware when Timer 2 overflows from 0xFFFF to 0x0000 or reload value. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. TF2 will not be set when RCLK and/or TCLK are logic 1.

Bit6: EXF2: Timer 2 External Flag.
Set by hardware when either a capture or reload is caused by a high-to-low transition on the T2EX input pin and EXEN2 is logic 1. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 Interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit5: RCLK: Receive Clock Flag.
Selects which timer is used for the UART's receive clock in modes 1 or 3.
0: Timer 1 overflows used for receive clock.
1: Timer 2 overflows used for receive clock.

Bit4: TCLK: Transmit Clock Flag.
Selects which timer is used for the UART's transmit clock in modes 1 or 3.
0: Timer 1 overflows used for transmit clock.
1: Timer 2 overflows used for transmit clock.

Bit3: EXEN2: Timer 2 External Enable.
Enables high-to-low transitions on T2EX to trigger captures or reloads when Timer 2 is not operating in Baud Rate Generator mode.
0: High-to-low transitions on T2EX ignored.
1: High-to-low transitions on T2EX cause a capture or reload.

Bit2: TR2: Timer 2 Run Control.
This bit enables/disables Timer 2.
0: Timer 2 disabled.
1: Timer 2 enabled.

Bit1: C/T2: Counter/Timer Select.
0: Timer Function: Timer 2 incremented by clock defined by T2M (CKCON.5).
1: Counter Function: Timer 2 incremented by high-to-low transitions on external input pin (T2).

Bit0: CP/RL2: Capture/Reload Select.
This bit selects whether Timer 2 functions in capture or auto-reload mode. EXEN2 must be logic 1 for high-to-low transitions on T2EX to be recognized and used to trigger captures or reloads. If RCLK or TCLK is set, this bit is ignored and Timer 2 will function in auto-reload mode.
0: Auto-reload on Timer 2 overflow or high-to-low transition at T2EX (EXEN2 = 1).
1: Capture on high-to-low transition at T2EX (EXEN2 = 1).

Figure 19.15. RCAP2L: Timer 2 Capture Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCA

Bits 7-0: RCAP2L: Timer 2 Capture Register Low Byte.
The RCAP2L register captures the low byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is configured in auto-reload mode, it holds the low byte of the reload value.

Figure 19.16. RCAP2H: Timer 2 Capture Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCB

Bits 7-0: RCAP2H: Timer 2 Capture Register High Byte.
The RCAP2H register captures the high byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is configured in auto-reload mode, it holds the high byte of the reload value.

Figure 19.17. TL2: Timer 2 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCC

Bits 7-0: TL2: Timer 2 Low Byte.
The TL2 register contains the low byte of the 16-bit Timer 2.

Figure 19.18. TH2: Timer 2 High Byte

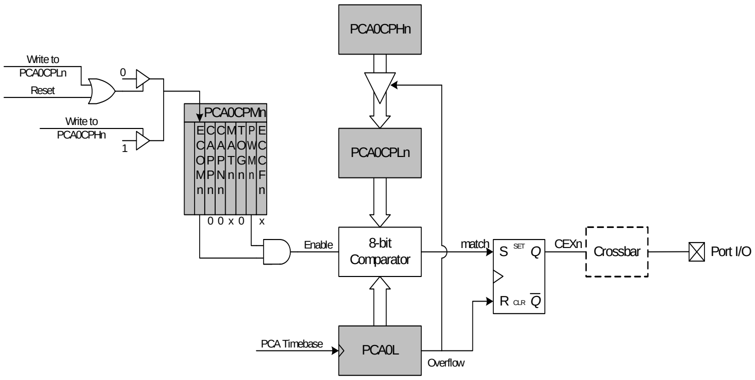
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCD

Bits 7-0: TH2: Timer 2 High Byte.
The TH2 register contains the high byte of the 16-bit Timer 2.

20.1.4. Pulse Width Modulator Mode

All of the modules can be used independently to generate pulse width modulated (PWM) outputs on their respective CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 20.6). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the PCA0CPHn without software intervention. It is good practice to write to PCA0CPHn instead of PCA0CPLn to avoid glitches in the digital comparator. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables Pulse Width Modulator mode.

Figure 20.6. PCA PWM Mode Diagram



21.1.1. EXTEST Instruction

The EXTEST instruction is accessed via the IR. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature. All inputs to on-chip logic are set to one.

21.1.2. SAMPLE Instruction

The SAMPLE instruction is accessed via the IR. The Boundary DR provides observability and presetting of the scan-path latches.

21.1.3. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard 1-bit JTAG Bypass data register.

21.1.4. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

Figure 21.2. DEVICEID: JTAG Device ID Register

				Reset Value
Version	Part Number	Manufacturer ID	1	(Varies)
Bit31 Bit28	Bit27 Bit12	Bit11 Bit1	Bit0	

Version = 0000b (Revision A) or
= 0001b (Revision B)

Part Number = 0000 0000 0000 0000b or
= 0000 0000 0000 0010b

Manufacturer ID = 0010 0100 001b (Silicon Laboratories)