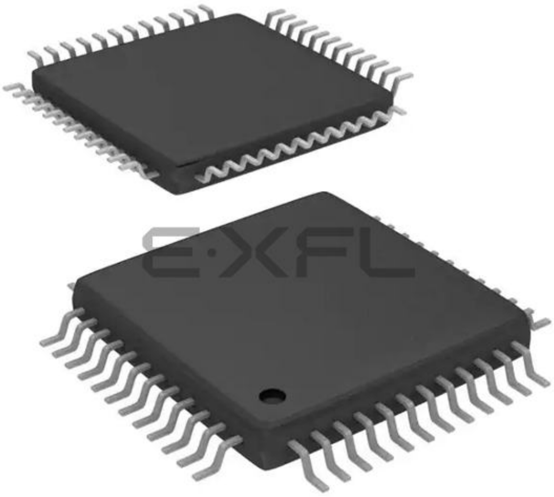

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f011-gq

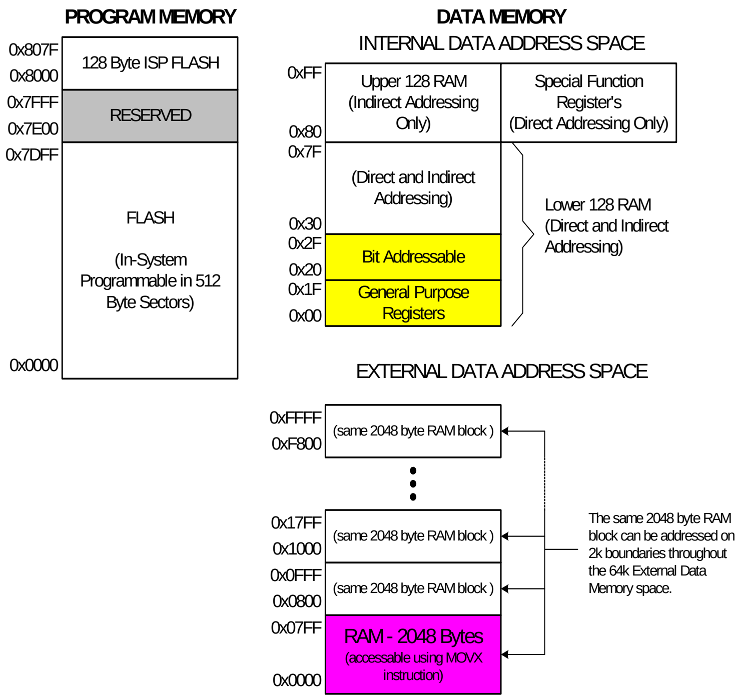
1.2. On-Board Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general-purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F005/06/07/15/16/17 MCUs additionally has a 2048 byte RAM block in the external data memory address space. This 2048 byte block can be addressed over the entire 64k external data memory address range (see Figure 1.6).

The MCU's program memory consists of 32k + 128 bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See Figure 1.6 for the MCU system memory map.

Figure 1.6. On-Board Memory Map


PROGRAM MEMORY
0x807F
0x8000
128 Byte ISP FLASH
0x7FFF
0x7E00
RESERVED
0x7DFF
FLASH
(In-System Programmable in 512 Byte Sectors)
0x0000
DATA MEMORY
INTERNAL DATA ADDRESS SPACE
0xFF
0x80
Upper 128 RAM (Indirect Addressing Only)
Special Function Register's (Direct Addressing Only)
0x7F
(Direct and Indirect Addressing)
0x30
0x2F
Bit Addressable
0x20
0x1F
General Purpose Registers
0x00
Lower 128 RAM (Direct and Indirect Addressing)
EXTERNAL DATA ADDRESS SPACE
0xFFFF
0xF800
(same 2048 byte RAM block)
0x17FF
0x1000
(same 2048 byte RAM block)
0x0FFF
0x0800
(same 2048 byte RAM block)
0x07FF
0x0000
RAM - 2048 Bytes
(accessable using MOVX instruction)
The same 2048 byte RAM block can be addressed on 2k boundaries throughout the 64k External Data Memory space.

1.4. Programmable Digital I/O and Crossbar

The standard 8051 Ports (0, 1, 2, and 3) are available on the MCUs. All four ports are pinned out on the F000/05/10/15. Ports 0 and 1 are pinned out on the F001/06/11/16, and only Port 0 is pinned out on the F002/07/12/17. The Ports not pinned out are still available for software use as general purpose registers. The Port I/O behave like the standard 8051 with a few enhancements.

Each Port I/O pin can be configured as either a push-pull or open-drain output. Also, the “weak pull-ups” which are normally fixed on an 8051 can be globally disabled, providing additional power saving capabilities for low power applications.

Perhaps the most unique enhancement is the Digital Crossbar. This is essentially a large digital switching network that allows mapping of internal digital system resources to Port I/O pins on P0, P1, and P2. (See Figure 1.8.) Unlike microcontrollers with standard multiplexed digital I/O, all combinations of functions are supported.

The on-board counter/timers, serial buses, HW interrupts, ADC Start of Conversion input, comparator outputs, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for his particular application.

Figure 1.8. Digital Crossbar Diagram

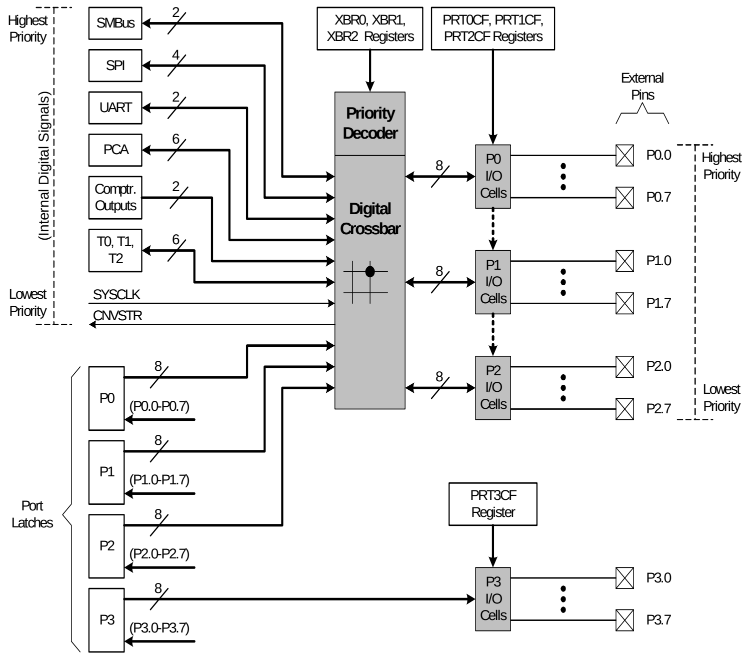


Figure 6.7. ADC0CN: ADC Control Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCEN	ADCTM	ADCINT	ADBUSY	ADSTM1	ADSTM0	ADWINT	ADLJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xE8

Bit7: ADCEN: ADC Enable Bit
0: ADC Disabled. ADC is in low power shutdown.
1: ADC Enabled. ADC is active and ready for data conversions.

Bit6: ADCTM: ADC Track Mode Bit
0: When the ADC is enabled, tracking is always done unless a conversion is in process
1: Tracking Defined by ADSTM1-0 bits
ADSTM1-0:
00: Tracking starts with the write of 1 to ADBUSY and lasts for 3 SAR clocks
01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks
10: ADC tracks only when CNVSTR input is logic low
11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks

Bit5: ADCINT: ADC Conversion Complete Interrupt Flag
(Must be cleared by software)
0: ADC has not completed a data conversion since the last time this flag was cleared
1: ADC has completed a data conversion

Bit4: ADBUSY: ADC Busy Bit
Read
0: ADC Conversion complete or no valid data has been converted since a reset. The falling edge of ADBUSY generates an interrupt when enabled.
1: ADC Busy converting data
Write
0: No effect
1: Starts ADC Conversion if ADSTM1-0 = 00b

Bits3-2: ADSTM1-0: ADC Start of Conversion Mode Bits
00: ADC conversion started upon every write of 1 to ADBUSY
01: ADC conversions taken on every overflow of Timer 3
10: ADC conversion started upon every rising edge of CNVSTR
11: ADC conversions taken on every overflow of Timer 2

Bit1: ADWINT: ADC Window Compare Interrupt Flag
(Must be cleared by software)
0: ADC Window Comparison Data match has not occurred
1: ADC Window Comparison Data match occurred

Bit0: ADLJST: ADC Left Justify Data Bit
0: Data in ADC0H:ADC0L Registers is right justified
1: Data in ADC0H:ADC0L Registers is left justified

Figure 6.8. ADC0H: ADC Data Word MSB Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBF

Bits7-0: ADC Data Word Bits
For ADLJST = 1: Upper 8-bits of the 10-bit ADC Data Word.
For ADLJST = 0: Bits7-2 are the sign extension of Bit1. Bits 1-0 are the upper 2-bits of the 10-bit ADC Data Word.

Figure 6.9. ADC0L: ADC Data Word LSB Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBE

Bits7-0: ADC Data Word Bits
For ADLJST = 1: Bits7-6 are the lower 2-bits of the 10-bit ADC Data Word. Bits5-0 will always read 0.
For ADLJST = 0: Bits7-0 are the lower 8-bits of the 10-bit ADC Data Word.

NOTE: Resulting 10-bit ADC Data Word appears in the ADC Data Word Registers as follows:
ADC0H[1:0]:ADC0L[7:0], if ADLJST = 0
(ADC0H[7:2] will be sign extension of ADC0H.1 if a differential reading, otherwise = 000000b)

ADC0H[7:0]:ADC0L[7:6], if ADLJST = 1
(ADC0L[5:0] = 000000b)

EXAMPLE: ADC Data Word Conversion Map, AIN0 Input in Single-Ended Mode
(AMX0CF=0x00, AMX0SL=0x00)

AIN0 – AGND (Volts)	**ADC0H:ADC0L** (ADLJST = 0)	**ADC0H:ADC0L** (ADLJST = 1)
REF x (1023/1024)	0x03FF	0xFFC0
REF x ½	0x0200	0x8000
REF x (511/1024)	0x01FF	0x7FC0
0	0x0000	0x0000

EXAMPLE: ADC Data Word Conversion Map, AIN0-AIN1 Differential Input Pair
(AMX0CF=0x01, AMX0SL=0x00)

AIN0 – AIN1 (Volts)	**ADC0H:ADC0L** (ADLJST = 0)	**ADC0H:ADC0L** (ADLJST = 1)
REF x (511/512)	0x01FF	0x7FC0
0	0x0000	0x0000
-REF x (1/512)	0xFFFF	0xFFC0
-REF	0xFE00	0x8000

6.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Figure 6.14 and Figure 6.15 show example comparisons for reference. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 6.10. ADC0GTH: ADC Greater-Than Data High Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC5

Bits7-0:
The high byte of the ADC Greater-Than Data Word.

Figure 6.11. ADC0GTL: ADC Greater-Than Data Low Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC4

Bits7-0:
The low byte of the ADC Greater-Than Data Word.
Definition:
ADC Greater-Than Data Word = ADC0GTH:ADC0GTL

Figure 6.12. ADC0LTH: ADC Less-Than Data High Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC7

Bits7-0:
The high byte of the ADC Less-Than Data Word.

Figure 6.13. ADC0LTL: ADC Less-Than Data Low Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC6

Bits7-0:
These bits are the low byte of the ADC Less-Than Data Word.

Definition:
ADC Less-Than Data Word = ADC0LTH:ADC0LTL

Table 6.1. 10-Bit ADC Electrical Characteristics

VDD = 3.0V, AV+ = 3.0V, VREF = 2.40V (REFBE=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY					
Resolution			10		bits
Integral Nonlinearity			± ½	± 1	LSB
Differential Nonlinearity	Guaranteed Monotonic		± ½	± 1	LSB
Offset Error			± 0.5		LSB
Full Scale Error	Differential mode		-1.5 ± 0.5		LSB
Offset Temperature Coefficient			± 0.25		ppm/°C
DYNAMIC PERFORMANCE (10kHz sine-wave input, 0 to –1dB of full scale, 100ksps)					
Signal-to-Noise Plus Distortion		59	61		dB
Total Harmonic Distortion	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range			80		dB
CONVERSION RATE					
Conversion Time in SAR Clocks		16			clocks
SAR Clock Frequency	C8051F000, ‘F001, ‘F002 C8051F005, ‘F006, ‘F007			2.0 2.5	MHz MHz
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
ANALOG INPUTS					
Voltage Conversion Range	Single-ended Mode (AINn – AGND) Differential Mode |(AINn+) – (AINm-)|	0		VREF - 1LSB	V
Input Voltage	Any AINn pin	AGND		AV+	V
Input Capacitance			10		pF
TEMPERATURE SENSOR					
Linearity			± 0.20		°C
Absolute Accuracy			± 3		°C
Gain	PGA Gain = 1		2.86		mV/°C
Gain Error (±1σ)	PGA Gain = 1		± 33.5		µV/°C
Offset	PGA Gain = 1, Temp = 0°C		776		mV
Offset Error (±1σ)	PGA Gain = 1, Temp = 0°C		± 8.51		mV
POWER SPECIFICATIONS					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100ksps		450	900	µA
Power Supply Rejection			± 0.3		mV/V

Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's maximum system clock at 25MHz, it has a peak throughput of 25MIPS. The CIP-51 has a total of 109 instructions. The number of instructions versus the system clock cycles required to execute them is as follows:

Instructions	26	50	5	14	7	3	1	2	1
Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8

Programming and Debugging Support

A JTAG-based serial interface is provided for in-system programming of the Flash program memory and communication with on-chip debug support circuitry. The reprogrammable Flash can also be read and changed a single byte at a time by the application software using the MOVC and MOVX instructions. This feature allows program memory to be used for non-volatile data storage as well as updating program code under software control.

The on-chip debug support circuitry facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints and watch points, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive and non-invasive, requiring no RAM, Stack, timers, or other on-chip resources.

The CIP-51 is supported by development tools from Silicon Laboratories and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, macro assembler, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via its JTAG interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

10.1. INSTRUCTION SET

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

10.1.1. Instruction and CPU Timing

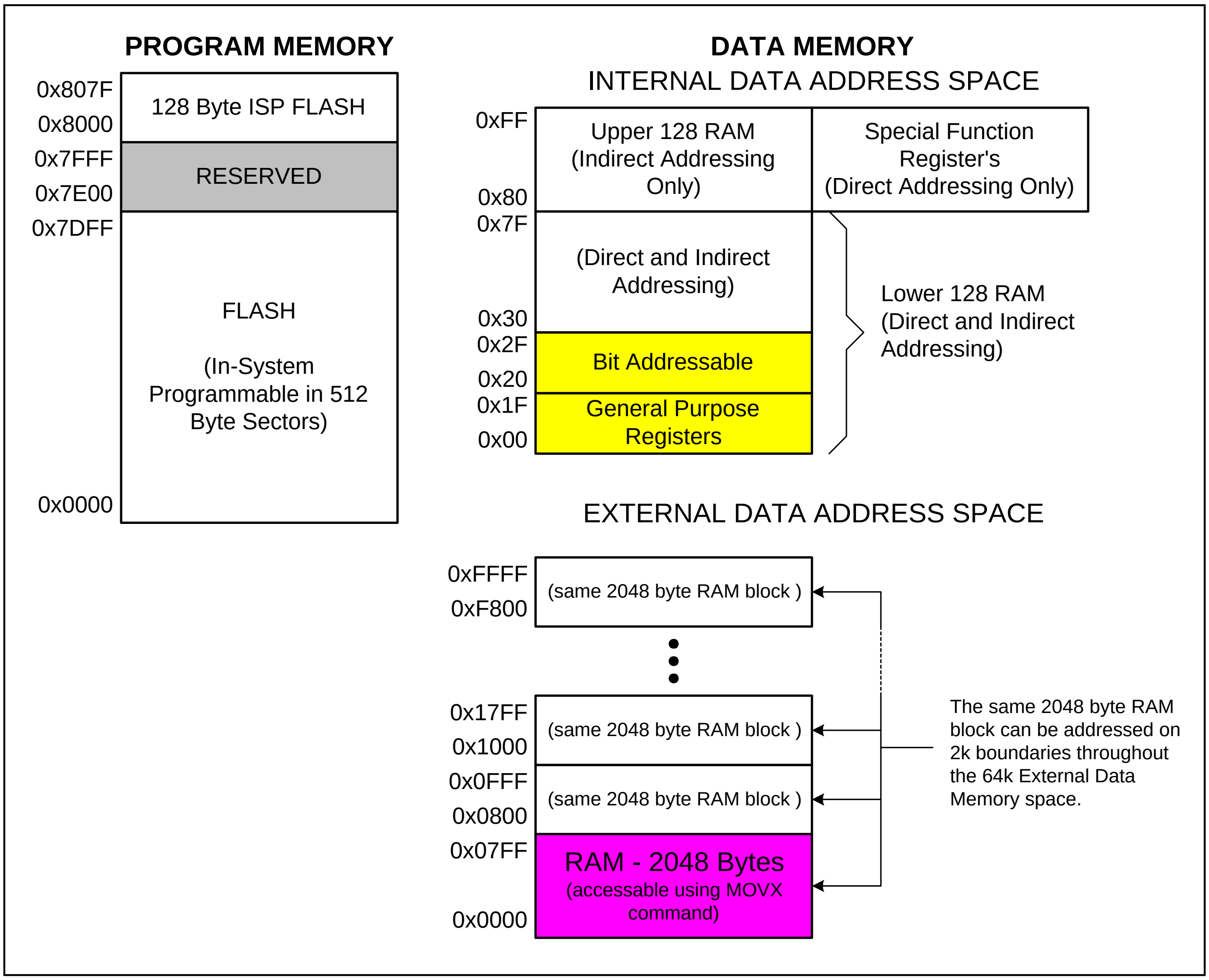
In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 10.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.

10.1.2. MOVX Instruction and Program Memory

The MOVX instruction is typically used to access external data memory. In the CIP-51, the MOVX instruction can access the on-chip program memory space implemented as reprogrammable Flash memory using the control bits in the PSCTL register (see Figure 11.1). This feature provides a mechanism for the CIP-51 to update program code and use the program memory space for non-volatile data storage. For the products with RAM mapped into external data memory space (C8051F005/06/07/15/16/17), MOVX is still used to read/write this memory with the PSCTL

Figure 10.2. Memory Map


PROGRAM MEMORY
0x807F
0x8000
128 Byte ISP FLASH
0x7FFF
0x7E00
RESERVED
0x7DFF
FLASH
(In-System Programmable in 512 Byte Sectors)
0x0000
DATA MEMORY
INTERNAL DATA ADDRESS SPACE
0xFF
Upper 128 RAM (Indirect Addressing Only)
Special Function Register's (Direct Addressing Only)
0x80
0x7F
(Direct and Indirect Addressing)
0x30
0x2F
Bit Addressable
0x20
0x1F
General Purpose Registers
0x00
Lower 128 RAM (Direct and Indirect Addressing)
EXTERNAL DATA ADDRESS SPACE
0xFFFF
0xF800
(same 2048 byte RAM block)
0x17FF
0x1000
(same 2048 byte RAM block)
0x0FFF
0x0800
(same 2048 byte RAM block)
0x07FF
RAM - 2048 Bytes
(accessable using MOVX command)
0x0000
The same 2048 byte RAM block can be addressed on 2k boundaries throughout the 64k External Data Memory space.

10.2.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The MCUs also have built-in hardware for a stack record. The stack record is a 32-bit shift register, where each Push or increment SP pushes one record bit onto the register, and each Call or interrupt pushes two record bits onto the register. (A Pop or decrement SP pops one record bit, and a Return pops two record bits, also.) The stack record circuitry can also detect an overflow or underflow on the Stack, and can notify the debug software even with the MCU running full-speed debug.

Figure 10.14. EIP2: Extended Interrupt Priority 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PXVLD	-	PX7	PX6	PX5	PX4	PADC0	PT3	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF7

Bit7: PXVLD: External Clock Source Valid (XTLVLD) Interrupt Priority Control.
This bit sets the priority of the XTLVLD interrupt.
0: XTLVLD interrupt set to low priority level.
1: XTLVLD interrupt set to high priority level.

Bit6: Reserved: Must write 0. Reads 0.

Bit5: PX7: External Interrupt 7 Priority Control.
This bit sets the priority of the External Interrupt 7.
0: External Interrupt 7 set to low priority level.
1: External Interrupt 7 set to high priority level.

Bit4: PX6: External Interrupt 6 Priority Control.
This bit sets the priority of the External Interrupt 6.
0: External Interrupt 6 set to low priority level.
1: External Interrupt 6 set to high priority level.

Bit3: PX5: External Interrupt 5 Priority Control.
This bit sets the priority of the External Interrupt 5.
0: External Interrupt 5 set to low priority level.
1: External Interrupt 5 set to high priority level.

Bit2: PX4: External Interrupt 4 Priority Control.
This bit sets the priority of the External Interrupt 4.
0: External Interrupt 4 set to low priority level.
1: External Interrupt 4 set to high priority level.

Bit1: PADC0: ADC End of Conversion Interrupt Priority Control.
This bit sets the priority of the ADC0 End of Conversion Interrupt.
0: ADC0 End of Conversion interrupt set to low priority level.
1: ADC0 End of Conversion interrupt set to high priority level.

Bit0: PT3: Timer 3 Interrupt Priority Control.
This bit sets the priority of the Timer 3 interrupts.
0: Timer 3 interrupt set to low priority level.
1: Timer 3 interrupt set to high priority level.

13.1. Power-on Reset

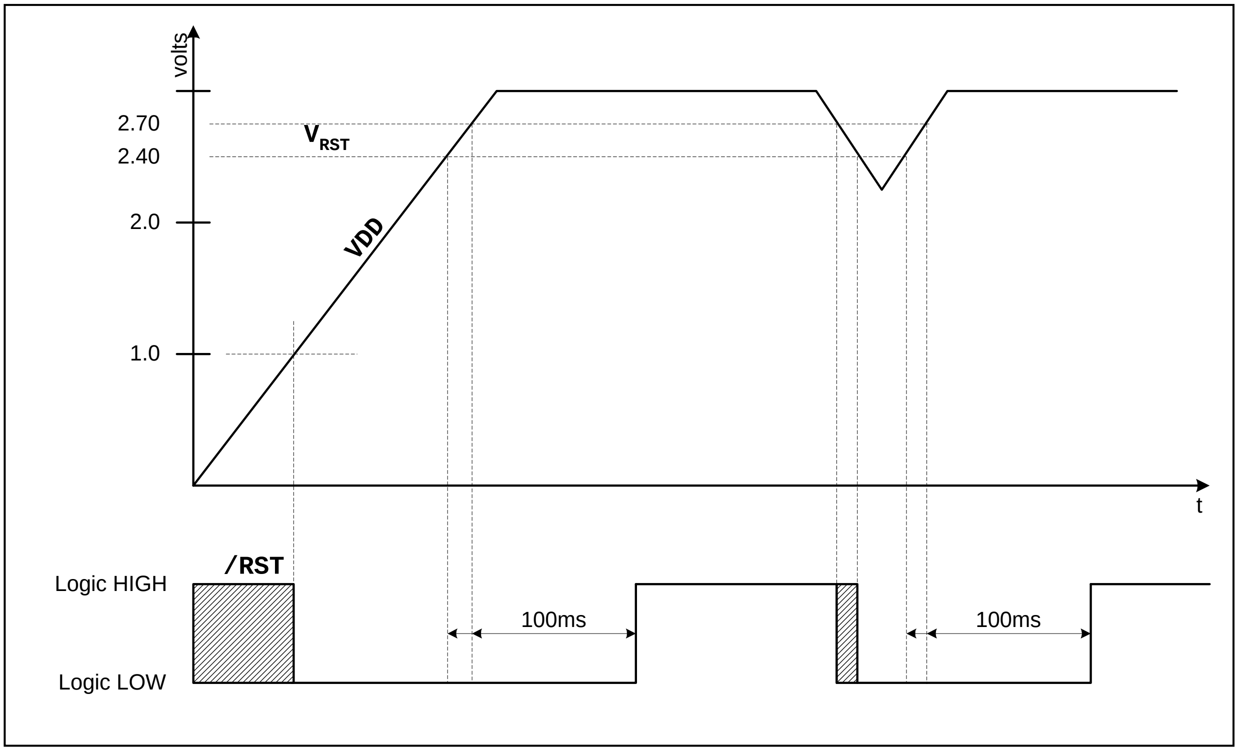
The C8051F000 family incorporates a power supply monitor that holds the MCU in the reset state until VDD rises above the V_{RST} level during power-up. (See Figure 13.2 for timing diagram, and refer to Table 13.1 for the Electrical Characteristics of the power supply monitor circuit.) The /RST pin is asserted (low) until the end of the 100ms VDD Monitor timeout in order to allow the VDD supply to become stable.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC Register are indeterminate. PORSF is cleared by a reset from any other source. Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset.

13.2. Software Forced Reset

Writing a 1 to the PORSF bit forces a Power-On Reset as described in Section 13.1.

Figure 13.2. VDD Monitor Timing Diagram



13.3. Power-fail Reset

When a power-down transition or power irregularity causes VDD to drop below V_{RST}, the power supply monitor will drive the /RST pin low and return the CIP-51 to the reset state (see Figure 13.2). When VDD returns to a level above V_{RST}, the CIP-51 will leave the reset state in the same manner as that for the power-on reset. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if VDD dropped below the level required for data retention. If the PORSF flag is set, the data may no longer be valid.

Figure 13.4. RSTSRC: Reset Source Register

R	R/W	R/W	R/W	R	R	R/W	R	Reset Value
JTAGRST	CNVRSEF	C0RSEF	SWRSEF	WDTRSF	MCDRSF	PORSF	PINRSF	xxxxxxxx
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xEF

(Note: Do not use read-modify-write operations on this register.)

Bit7: JTAGRST. JTAG Reset Flag.

0: JTAG is not currently in reset state.

1: JTAG is in reset state.

Bit6: CNVRSEF: Convert Start Reset Source Enable and Flag

Write

0: CNVSTR is not a reset source

1: CNVSTR is a reset source (active low)

Read

0: Source of prior reset was not from CNVSTR

1: Source of prior reset was from CNVSTR

Bit5: C0RSEF: Comparator 0 Reset Enable and Flag

Write

0: Comparator 0 is not a reset source

1: Comparator 0 is a reset source (active low)

Read

Note: The value read from C0RSEF is not defined if Comparator 0 has not been enabled as a reset source.

0: Source of prior reset was not from Comparator 0

1: Source of prior reset was from Comparator 0

Bit4: SWRSF: Software Reset Force and Flag

Write

0: No Effect

1: Forces an internal reset. /RST pin is not effected.

Read

0: Prior reset source was not from write to the SWRSF bit.

1: Prior reset source was from write to the SWRSF bit.

Bit3: WDTRSF: Watchdog Timer Reset Flag

0: Source of prior reset was not from WDT timeout.

1: Source of prior reset was from WDT timeout.

Bit2: MCDRSF: Missing Clock Detector Flag

0: Source of prior reset was not from Missing Clock Detector timeout.

1: Source of prior reset was from Missing Clock Detector timeout.

Bit1: PORSF: Power-On Reset Force and Flag

Write

0: No effect

1: Forces a Power-On Reset. /RST is driven low.

Read

0: Source of prior reset was not from POR.

1: Source of prior reset was from POR.

Bit0: PINRSF: HW Pin Reset Flag

0: Source of prior reset was not from /RST pin.

1: Source of prior reset was from /RST pin.

Figure 15.5. XBR2: Port I/O CrossBar Register 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	-	-	-	-	-	CNVSTE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xE3

Bit7: WEAKPUD: Port I/O Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled (except for Ports whose I/O are configured as push-pull)
1: Weak Pull-ups Disabled
Bit6: XBARE: Crossbar Enable Bit
0: Crossbar Disabled
1: Crossbar Enabled
Bits5-1: UNUSED. Read = 00000b, Write = don't care.
Bit0: CNVSTE: ADC Convert Start Input Enable Bit
0: CNVSTR unavailable at Port pin.
1: CNVSTR routed to Port Pin.

Example Usage of XBR0, XBR1, XBR2:
When selected, the digital resources fill the Port I/O pins in order (top to bottom as shown in Table 15.1) starting with P0.0 through P0.7, and then P1.0 through P1.7, and finally P2.0 through P2.7. If the digital resources are not mapped to the Port I/O pins, they default to their matching internal Port Register bits.

Example1: If XBR0 = 0x11, XBR1 = 0x00, and XBR2 = 0x40:
P0.0=SDA, P0.1=SCL, P0.2=CEX0, P0.3=CEX1, P0.4 … P2.7 map to corresponding Port I/O.

Example2: If XBR0 = 0x80, XBR1 = 0x04, and XBR2 = 0x41:
P0.0=CP0, P0.1=/INT0, P0.2 = CNVSTR, P0.3 … P2.7 map to corresponding Port I/O.

15.3. General Purpose Port I/O

Each MCU has four byte-wide, bi-directional parallel ports that can be used general purpose I/O. Each port is accessed through a corresponding special function register (SFR) that is both byte addressable and bit addressable. When writing to a port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the port's input pins are returned regardless of the XBRn settings (i.e. even when the pin is assigned to another signal by the Crossbar, the Port Register can always still read its corresponding Port I/O pin). The exception to this is the execution of the *read-modify-write* instructions. The *read-modify-write* instructions when operating on a port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SET, when the destination is an individual bit in a port SFR. For these instructions, the value of the port register (not the pin) is read, modified, and written back to the SFR.

15.4. Configuring Ports Which are not Pinned Out

P2 and P3 are not pinned out on the F001/06/11/16. P1, P2, and P3 are not pinned out on the F002/07/12/17. These port registers (and corresponding interrupts, where applicable) are still available for software use in these reduced pin count MCUs. Whether used or not in software, it is recommended not to let these port drivers go to high impedance state. This is prevented after reset by having the weak pull-ups enabled as described in the XBR2 register. It is recommended that each output driver for ports not pinned out should be configured as push-pull using the corresponding PRTnCF register. This will inhibit a high impedance state even if the weak pull-up is disabled.

Figure 15.6. P0: Port0 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0x80

Bits7-0: P0.[7:0]
(Write – Output appears on I/O pins per XBR0, XBR1, and XBR2 Registers)
0: Logic Low Output.
1: Logic High Output (high-impedance if corresponding PRT0CF.n bit = 0)
(Read – Regardless of XBR0, XBR1, and XBR2 Register settings).
0: P0.n pin is logic low.
1: P0.n pin is logic high.

Figure 15.7. PRT0CF: Port0 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xA4

Bits7-0: PRT0CF.[7:0]: Output Configuration Bits for P0.7-P0.0 (respectively)
0: Corresponding P0.n Output mode is Open-Drain.
1: Corresponding P0.n Output mode is Push-Pull.

(Note: When SDA, SCL, and RX appear on any of the P0 I/O, each are open-drain regardless of the value of PRT0CF).

18. UART

The UART is a serial port capable of asynchronous transmission. The UART can function in full duplex mode. In all modes, receive data is buffered in a holding register. This allows the UART to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART has an associated Serial Control Register (SCON) and a Serial Data Buffer (SBUF) in the SFRs. The single SBUF location provides access to both transmit and receive registers. Reads access the Receive register and writes access the Transmit register automatically.

The UART is capable of generating interrupts if enabled. The UART has two sources of interrupts: a Transmit Interrupt flag, TI (SCON.1) set when transmission of a data byte is complete, and a Receive Interrupt flag, RI (SCON.0) set when reception of a data byte is complete. The UART interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software. This allows software to determine the cause of the UART interrupt (transmit complete or receive complete).

Figure 18.1. UART Block Diagram

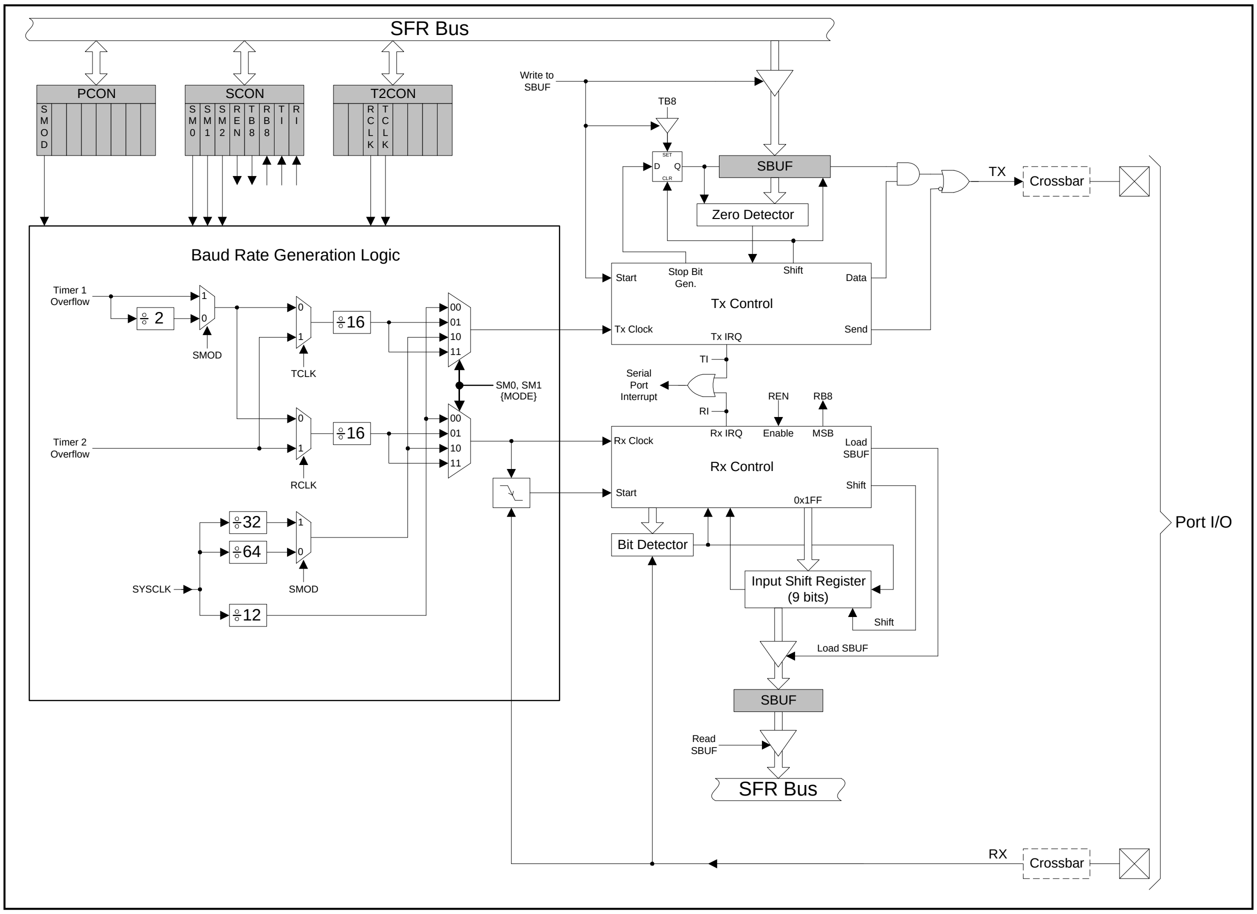


Table 18.2. Oscillator Frequencies for Standard Baud Rates

Oscillator Frequency (MHz)	Divide Factor	Timer 1 Load Value*	Resulting Baud Rate**
24.0	208	0xF3	115200 (115384)
23.592	205	0xF3	115200 (113423)
22.1184	192	0xF4	115200
18.432	160	0xF6	115200
16.5888	144	0xF7	115200
14.7456	128	0xF8	115200
12.9024	112	0xF9	115200
11.0592	96	0xFA	115200
9.216	80	0xFB	115200
7.3728	64	0xFC	115200
5.5296	48	0xFD	115200
3.6864	32	0xFE	115200
1.8432	16	0xFF	115200
24.576	320	0xEC	76800
25.0	434	0xE5	57600 (57870)
25.0	868	0xCA	28800
24.576	848	0xCB	28800 (28921)
24.0	833	0xCC	28800 (28846)
23.592	819	0xCD	28800 (28911)
22.1184	768	0xD0	28800
18.432	640	0xD8	28800
16.5888	576	0xDC	28800
14.7456	512	0xE0	28800
12.9024	448	0xE4	28800
11.0592	384	0xE8	28800
9.216	320	0xEC	28800
7.3728	256	0xF0	28800
5.5296	192	0xF4	28800
3.6864	128	0xF8	28800
1.8432	64	0xFC	28800

* Assumes SMOD=1 and T1M=1.
** Numbers in parenthesis show the actual baud rate.

Figure 18.8. SBUF: Serial (UART) Data Buffer Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x99

Bits7-0: SBUF.[7:0]: Serial Data Buffer Bits 7-0 (MSB-LSB)
This is actually two registers; a transmit and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. Moving a byte to SBUF is what initiates the transmission. When data is moved from SBUF, it comes from the receive buffer.

Figure 19.4. TCON: Timer Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0x88

Bit7: TF1: Timer 1 Overflow Flag.

Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.

0: No Timer 1 overflow detected.

1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.

0: Timer 1 disabled.

1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.

Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.

0: No Timer 0 overflow detected.

1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.

0: Timer 0 disabled.

1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.

This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 input signal’s logic level when IT1 = 0.

Bit2: IT1: Interrupt 1 Type Select.

This bit selects whether the configured /INT1 signal will detect falling edge or active-low level-sensitive interrupts.

0: /INT1 is level triggered.

1: /INT1 is edge triggered.

Bit1: IE0: External Interrupt 0.

This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 input signal’s logic level when IT0 = 0.

Bit0: IT0: Interrupt 0 Type Select.

This bit selects whether the configured /INT0 signal will detect falling edge or active-low level-sensitive interrupts.

0: /INT0 is level triggered.

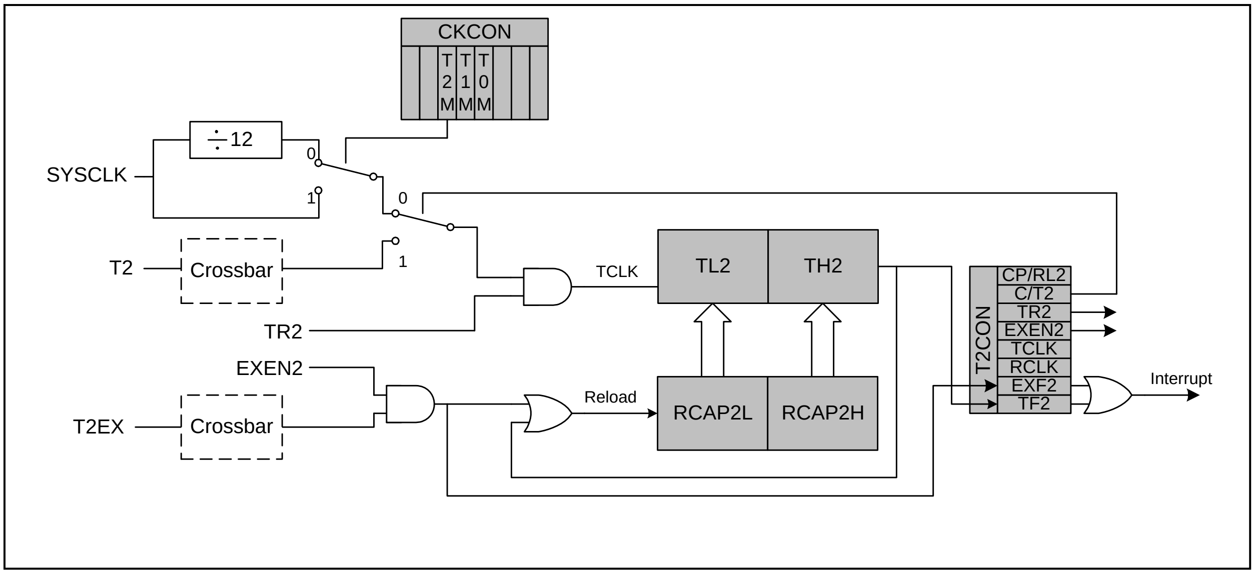
1: /INT0 is edge triggered.

19.2.2. Mode 1: 16-bit Counter/Timer with Auto-Reload

The Counter/Timer with Auto-Reload mode sets the TF2 timer overflow flag when the counter/timer register overflows from 0xFFFF to 0x0000. An interrupt is generated if enabled. On overflow, the 16-bit value held in the two capture registers (RCAP2H, RCAP2L) is automatically loaded into the counter/timer register and the timer is restarted.

Counter/Timer with Auto-Reload mode is selected by clearing the CP/RL2 bit. Setting TR2 to logic 1 enables and starts the timer. Timer 2 can use either the system clock or transitions on an external input pin as its clock source, as specified by the C/T2 bit. If EXEN2 is set to logic 1, a high-to-low transition on T2EX will also cause Timer 2 to be reloaded. If EXEN2 is cleared, transitions on T2EX will be ignored.

Figure 19.12. T2 Mode 1 Block Diagram



21.1. Boundary Scan

The Data Register in the Boundary Scan path is an 87-bit shift register. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature via the EXTEST and SAMPLE commands.

Table 21.1. Boundary Data Register Bit Definitions

EXTEST provides access to both capture and update actions, while Sample only performs a capture.

Bit	Action	Target
0	Capture	Reset Enable from MCU
	Update	Reset Enable to /RST pin
1	Capture	Reset input from /RST pin
	Update	Reset output to /RST pin
2	Capture	External Clock from XTAL1 pin
	Update	Not used
3	Capture	Weak pullup enable from MCU
	Update	Weak pullup enable to Port Pins
4-11	Capture	SFR Address Bus bit from CIP-51 (e.g. Bit4=SFRA0, Bit5=SFRA1…)
	Update	SFR Address Bus bit to SFR Address Bus (e.g. Bit4=XSFRA0, Bit5=XSFRA1)
12-19	Capture	SFR Data Bus bit read from SFR (e.g. Bit12=SFRD0, Bit13=SFRD1…)
	Update	SFR Data Bus bit written to SFR (e.g. Bit12=SFRD0, Bit13=SFRD1…)
20	Capture	SFR Write Strobe from CIP-51
	Update	SFR Write Strobe to SFR Bus
21	Capture	SFR Read Strobe from CIP-51
	Update	SFR Read Strobe to SFR Bus
22	Capture	SFR Read/Modify/Write Strobe from CIP-51
	Update	SFR Read/Modify/Write Strobe to SFR Bus
23,25,27,29, 31,33,35,37	Capture	P0.n output enable from MCU (e.g. Bit23=P0.0, Bit25=P0.1, etc.)
	Update	P0.n output enable to pin (e.g. Bit23=P0.0oe, Bit25=P0.1oe, etc.)
24,26,28,30, 32,34,36,38	Capture	P0.n input from pin (e.g. Bit24=P0.0, Bit26=P0.1, etc.)
	Update	P0.n output to pin (e.g. Bit24=P0.0, Bit26=P0.1, etc.)
39,41,43,45, 47,49,51,53	Capture	P1.n output enable from MCU (e.g. Bit39=P1.0, Bit41=P1.1, etc.)
	Update	P1.n output enable to pin (e.g. Bit39=P1.0oe, Bit41=P1.1oe, etc.)
40,42,44,46, 48,50,52,54	Capture	P1.n input from pin (e.g. Bit40=P1.0, Bit42=P1.1, etc.)
	Update	P1.n output to pin (e.g. Bit40=P1.0, Bit42=P1.1, etc.)
55,57,59,61, 63,65,67,69	Capture	P2.n output enable from MCU (e.g. Bit55=P2.0, Bit57=P2.1, etc.)
	Update	P2.n output enable to pin (e.g. Bit55=P2.0oe, Bit57=P2.1oe, etc.)
56,58,60,62, 64,66,68,70	Capture	P2.n input from pin (e.g. Bit56=P2.0, Bit58=P2.1, etc.)
	Update	P2.n output to pin (e.g. Bit56=P2.0, Bit58=P2.1, etc.)
71,73,75,77, 79,81,83,85	Capture	P3.n output enable from MCU (e.g. Bit71=P3.0, Bit73=P3.1, etc.)
	Update	P3.n output enable to pin (e.g. Bit71=P3.0oe, Bit73=P3.1oe, etc.)
72,74,76,78, 80,82,84,86	Capture	P3.n input from pin (e.g. Bit72=P3.0, Bit74=P3.1, etc.)
	Update	P3.n output to pin (e.g. Bit72=P3.0, Bit74=P3.1, etc.)