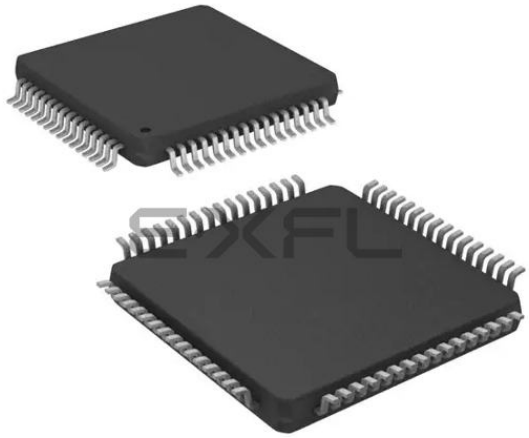

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f015

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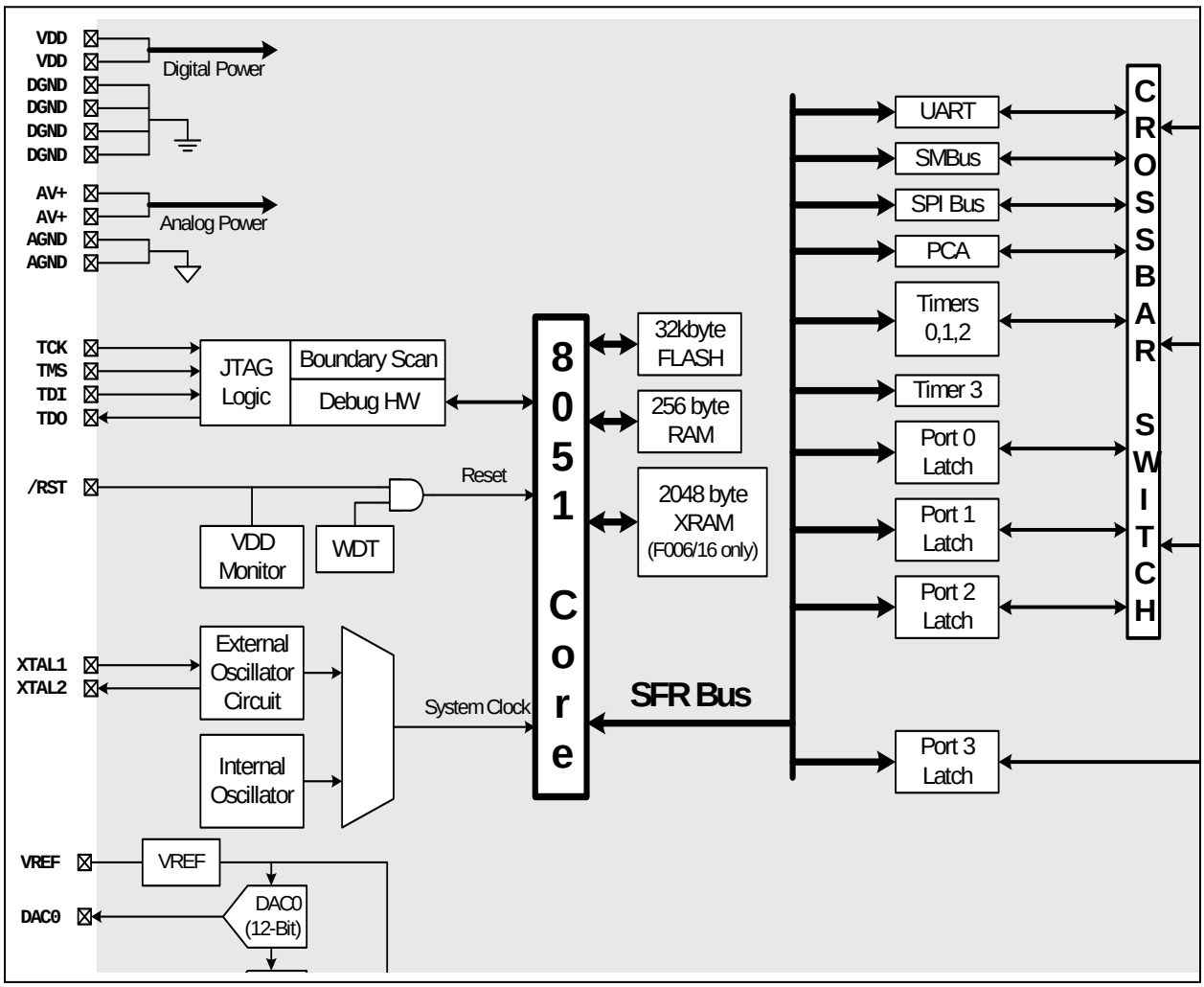
Figure 1.2. C8051F001/06/11/16 Block Diagram



1.1.3. Additional Features

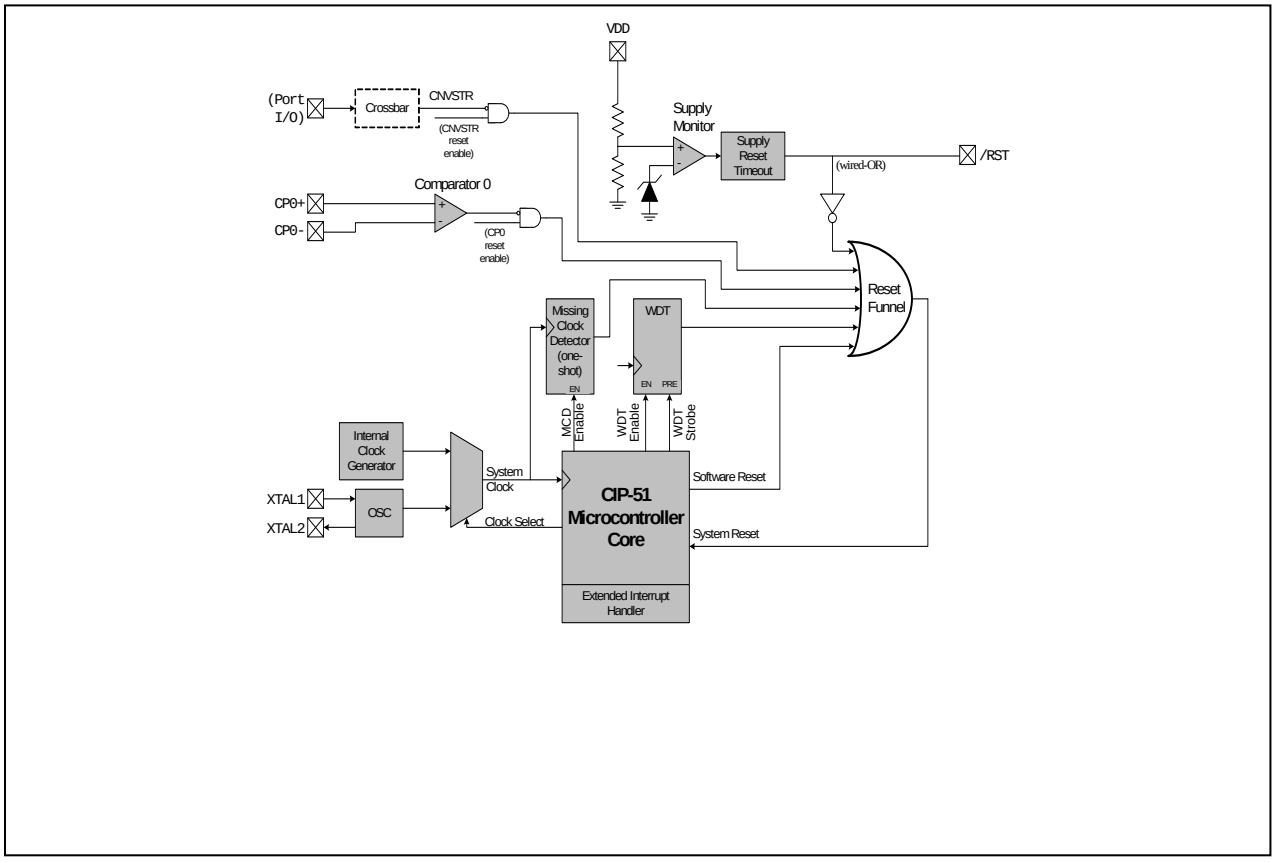
The C8051F000 MCU family has several key enhancements both inside and outside the CIP-51 core to improve its overall performance and ease of use in the end applications.

The extended interrupt handler provides 21 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to seven reset sources for the MCU: an on-board VDD monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator 0, a forced software reset, the CNVSTR pin, and the /RST pin. The /RST pin is bi-directional, accommodating an external reset, or allowing the internally generated POR to be output on the /RST pin. Each reset source except for the VDD monitor and Reset Input Pin may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand alone clock generator which is used by default as the system clock after any reset. If desired, the clock source may be switched on the fly to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 16MHz) internal oscillator as needed.

Figure 1.5. On-Board Clock and Reset



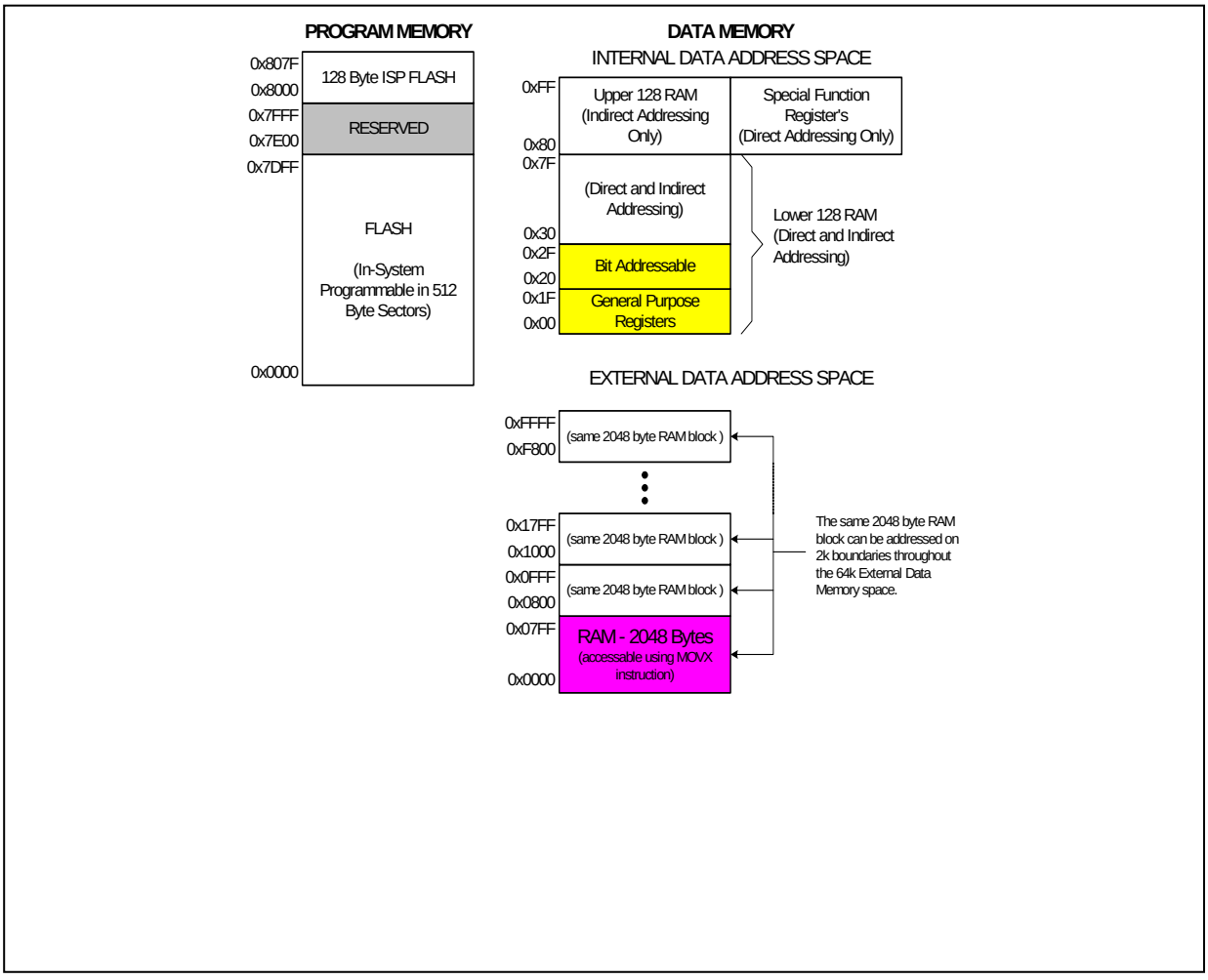
1.2. On-Board Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general-purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F005/06/07/15/16/17 MCUs additionally has a 2048 byte RAM block in the external data memory address space. This 2048 byte block can be addressed over the entire 64k external data memory address range (see Figure 1.6).

The MCU's program memory consists of 32k + 128 bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See Figure 1.6 for the MCU system memory map.

Figure 1.6. On-Board Memory Map

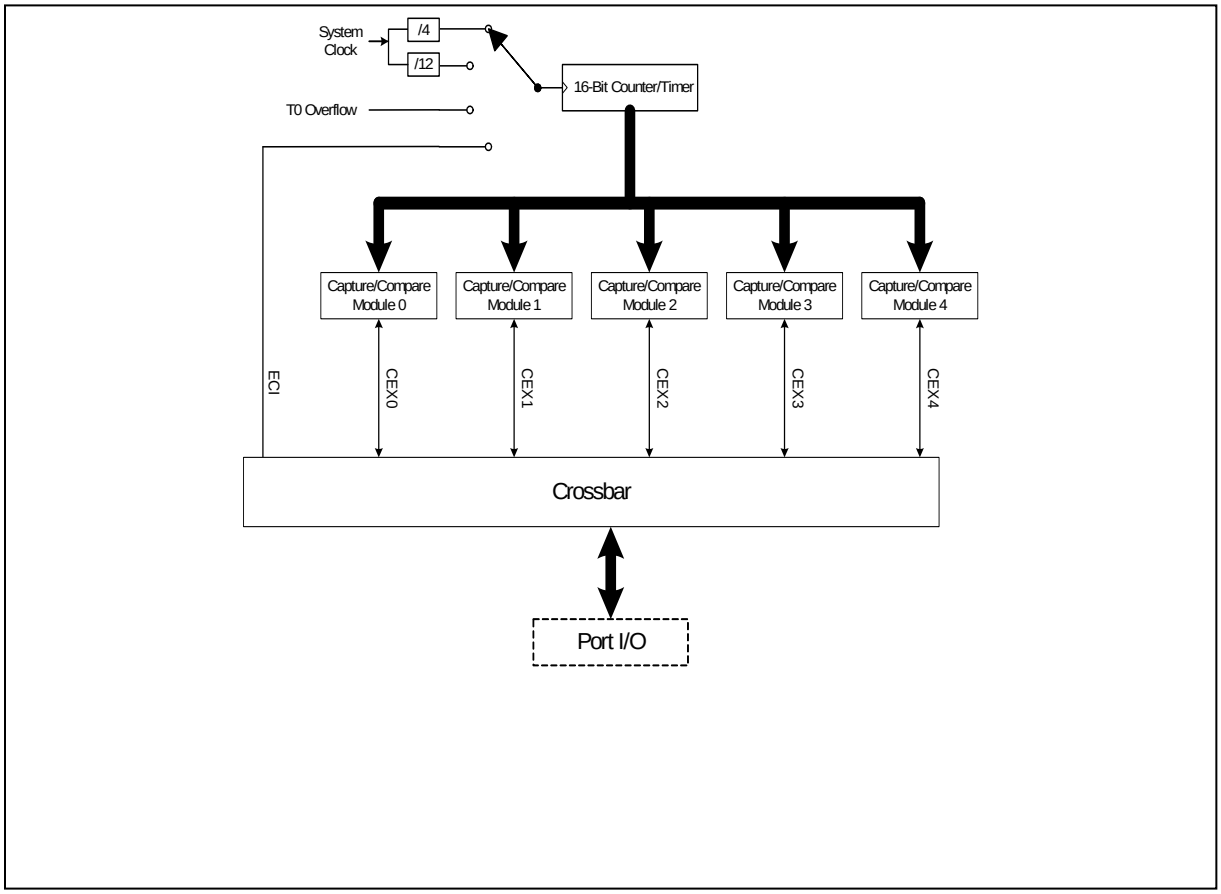


1.5. Programmable Counter Array

The C8051F000 MCU family has an on-board Programmable Counter/Timer Array (PCA) in addition to the four 16-bit general-purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer timebase with 5 programmable capture/compare modules. The timebase gets its clock from one of four sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflow, or an External Clock Input (ECI).

Each capture/compare module can be configured to operate in one of four modes: Edge-Triggered Capture, Software Timer, High Speed Output, or Pulse Width Modulator. The PCA Capture/Compare Module I/O and External Clock Input are routed to the MCU Port I/O via the Digital Crossbar.

Figure 1.9. PCA Block Diagram



1.6. Serial Ports

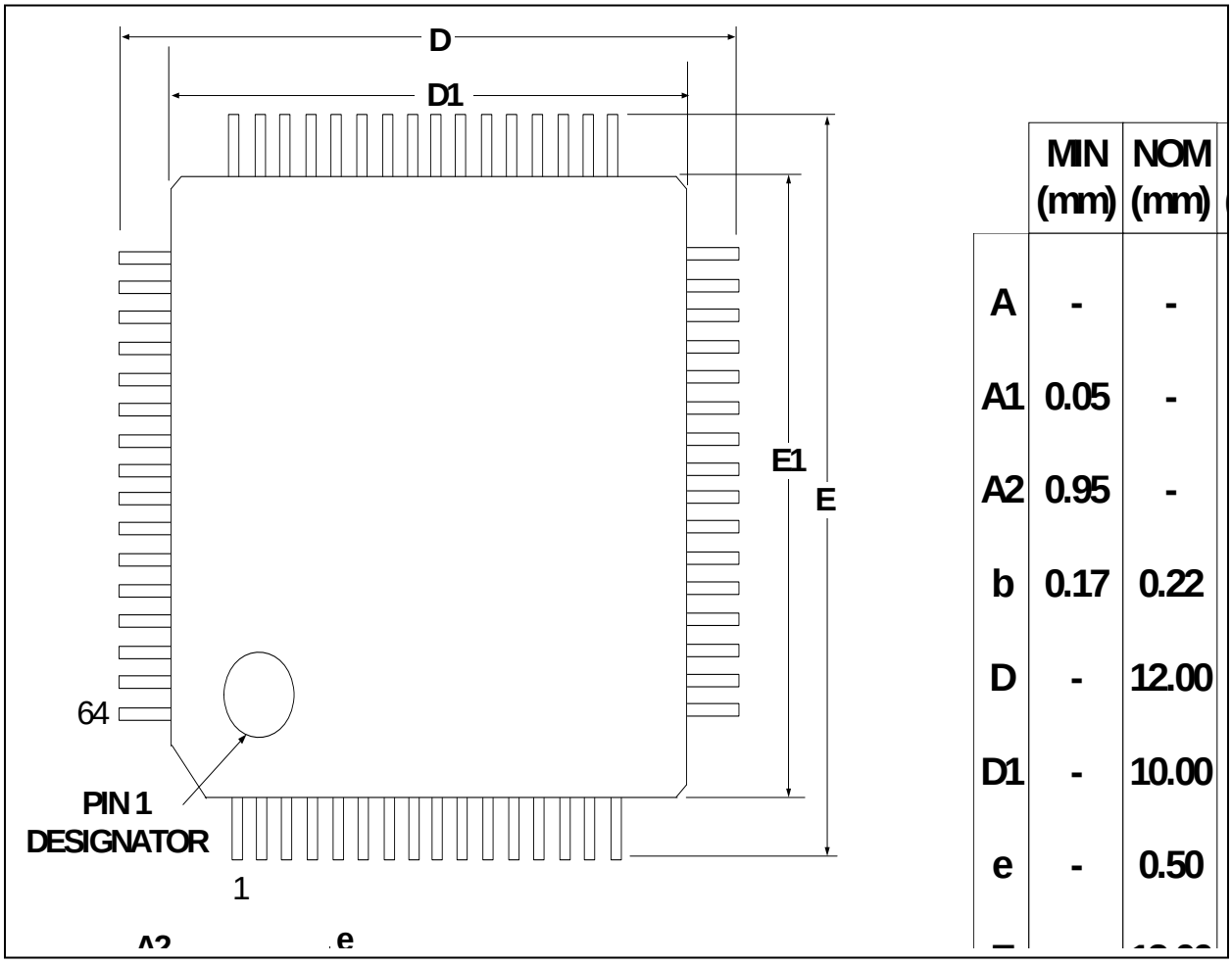
The C8051F000 MCU Family includes a Full-Duplex UART, SPI Bus, and I2C/SMBus. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little intervention by the CPU. The serial buses do not "share" resources such as timers, interrupts, or Port I/O, so any or all of the serial buses may be used together.

4. PINOUT AND PACKAGE DEFINITIONS

Table 4.1. Pin Definitions

Name	Pin Numbers			Type	Description
	F000 F005 F010 F015	F001 F006 F011 F016	F002 F007 F012 F017		
VDD	31, 40, 62	23, 32	18, 20		Digital Voltage Supply.
DGND	30, 41, 61	22, 33, 27, 19	17, 21		Digital Ground.
AV+	16, 17	13, 43	9, 29		Positive Analog Voltage Supply.
AGND	5, 15	44, 12	8, 30		Analog Ground.
TCK	22	18	14	D In	JTAG Test Clock with internal pull-up.
TMS	21	17	13	D In	JTAG Test-Mode Select with internal pull-up.
TDI	28	20	15	D In	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	29	21	16	D Out	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
XTAL1	18	14	10	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	19	15	11	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
/RST	20	16	12	D I/O	Chip Reset. Open-drain output of internal Voltage Supply monitor. Is driven low when VDD is < 2.7V. An external source can force a system reset by driving this pin low.
VREF	6	3	3	A I/O	Voltage Reference. When configured as an input, this pin is the voltage reference for the MCU. Otherwise, the internal reference drives this pin.
CP0+	4	2	2	A In	Comparator 0 Non-Inverting Input.
CP0-	3	1	1	A In	Comparator 0 Inverting Input.
CP1+	2	45		A In	Comparator 1 Non-Inverting Input.
CP1-	1	46		A In	Comparator 1 Inverting Input.
DAC0	64	48	32	A Out	Digital to Analog Converter Output 0. The DAC0 voltage output. (See Section 7 DAC Specification for complete description).
DAC1	63	47	31	A Out	Digital to Analog Converter Output 1. The DAC1 voltage output. (See Section 7 DAC Specification for complete description).
AIN0	7	4	4	A In	Analog Mux Channel Input 0. (See ADC Specification for complete description).
AIN1	8	5	5	A In	Analog Mux Channel Input 1. (See ADC Specification for complete description).
AIN2	9	6	6	A In	Analog Mux Channel Input 2. (See ADC Specification for complete description).
AIN3	10	7	7	A In	Analog Mux Channel Input 3. (See ADC Specification for complete description).
AIN4	11	8		A In	Analog Mux Channel Input 4. (See ADC Specification for complete description).
AIN5	12	9		A In	Analog Mux Channel Input 5. (See ADC Specification for complete description).

Figure 4.2. TQFP-64 Package Drawing



	MIN (mm)	NOM (mm)
A	-	-
A1	0.05	-
A2	0.95	-
b	0.17	0.22
D	-	12.00
D1	-	10.00
e	-	0.50

Table 5.1. 12-Bit ADC Electrical Characteristics

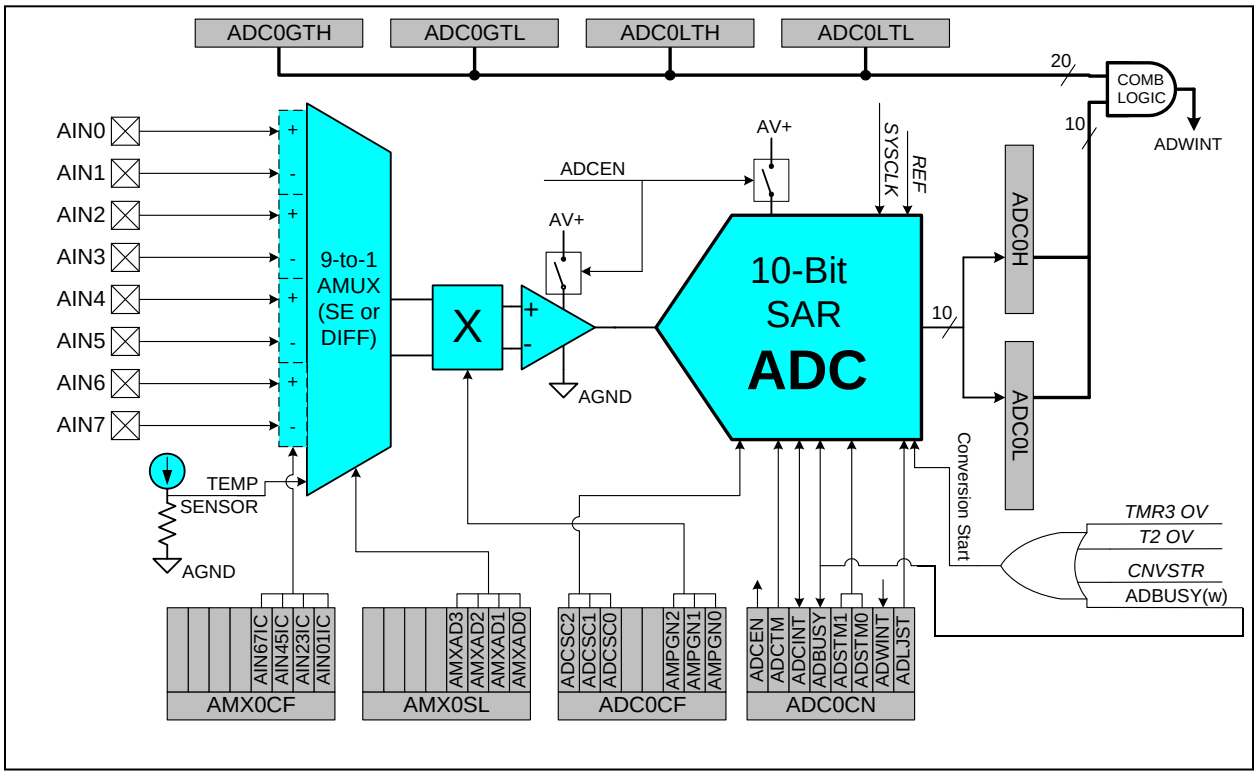
VDD = 3.0V, AV+ = 3.0V, VREF = 2.40V (REFBE=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY					
Resolution			12		bits
Integral Nonlinearity				± 1	LSB
Differential Nonlinearity	Guaranteed Monotonic			± 1	LSB
Offset Error			-3 ± 1		LSB
Full Scale Error	Differential mode		-7 ± 3		LSB
Offset Temperature Coefficient			± 0.25		ppm/°C
DYNAMIC PERFORMANCE (10kHz sine-wave input, 0 to –1dB of full scale, 100ksps)					
Signal-to-Noise Plus Distortion		66	69		dB
Total Harmonic Distortion	Up to the 5th harmonic		-75		dB
Spurious-Free Dynamic Range			80		dB
CONVERSION RATE					
Conversion Time in SAR Clocks		16			clocks
SAR Clock Frequency	C8051F000, ‘F001, ‘F002 C8051F005, ‘F006, ‘F007			2.0 2.5	MHz MHz
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
ANALOG INPUTS					
Voltage Conversion Range	Single-ended Mode (AINn – AGND) Differential Mode |(AINn+) – (AINm-)|	0		VREF - 1LSB	V
Input Voltage	Any AINn pin	AGND		AV+	V
Input Capacitance			10		pF
TEMPERATURE SENSOR					
Linearity			± 0.20		°C
Absolute Accuracy			± 3		°C
Gain	PGA Gain = 1		2.86		mV/°C
Gain Error (±1σ)	PGA Gain = 1		± 33.5		µV/°C
Offset	PGA Gain = 1, Temp = 0°C		776		mV
Offset Error (±1σ)	PGA Gain = 1, Temp = 0°C		± 8.51		mV
POWER SPECIFICATIONS					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100ksps		450	900	µA
Power Supply Rejection			± 0.3		mV/V

6. ADC (10-Bit, C8051F010/1/2/5/6/7 Only)

The ADC subsystem for the C8051F010/1/2/5/6/7 consists of a 9-channel, configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 10-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector (see block diagram in Figure 6.1). The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Register's shown in Figure 6.1. The ADC subsystem (ADC, track-and-hold and PGA) is enabled only when the ADCEN bit in the ADC Control register (ADC0CN, Figure 6.7) is set to 1. The ADC subsystem is in low power shutdown when this bit is 0. The Bias Enable bit (BIASE) in the REF0CN register (see Figure 9.2) must be set to 1 in order to supply bias to the ADC.

Figure 6.1. 10-Bit ADC Functional Block Diagram



6.1. Analog Multiplexer and PGA

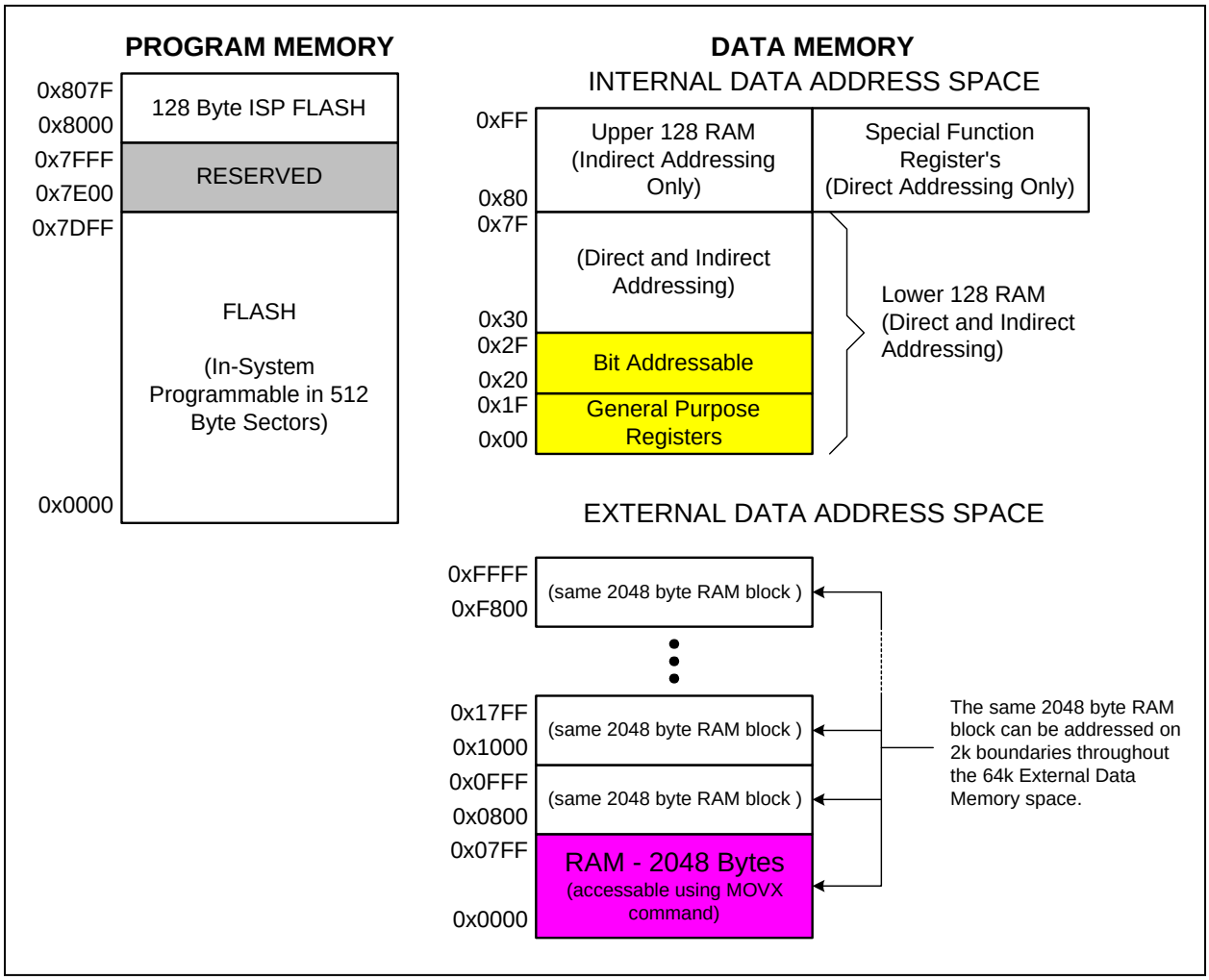
Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-board temperature sensor (temperature transfer function is shown in Figure 6.3). Note that the PGA gain is applied to the temperature sensor reading. AMUX input pairs can be programmed to operate in either the differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (Figure 6.5), and the Configuration register AMX0CF (Figure 6.4). The table in Figure 6.5 shows AMUX functionality by channel for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the AMPGN2-0 bits in the ADC Configuration register, ADC0CF (Figure 6.6). The PGA can be software-programmed for gains of 0.5, 1, 2, 4, 8 or 16. It defaults to unity gain on reset.

Table 6.1. 10-Bit ADC Electrical Characteristics

VDD = 3.0V, AV+ = 3.0V, VREF = 2.40V (REFBE=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY					
Resolution			10		bits
Integral Nonlinearity			± ½	± 1	LSB
Differential Nonlinearity	Guaranteed Monotonic		± ½	± 1	LSB
Offset Error			± 0.5		LSB
Full Scale Error	Differential mode		-1.5 ± 0.5		LSB
Offset Temperature Coefficient			± 0.25		ppm/°C
DYNAMIC PERFORMANCE (10kHz sine-wave input, 0 to –1dB of full scale, 100ksps)					
Signal-to-Noise Plus Distortion		59	61		dB
Total Harmonic Distortion	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range			80		dB
CONVERSION RATE					
Conversion Time in SAR Clocks		16			clocks
SAR Clock Frequency	C8051F000, ‘F001, ‘F002 C8051F005, ‘F006, ‘F007			2.0 2.5	MHz MHz
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
ANALOG INPUTS					
Voltage Conversion Range	Single-ended Mode (AINn – AGND) Differential Mode |(AINn+) – (AINm-)|	0		VREF - 1LSB	V
Input Voltage	Any AINn pin	AGND		AV+	V
Input Capacitance			10		pF
TEMPERATURE SENSOR					
Linearity			± 0.20		°C
Absolute Accuracy			± 3		°C
Gain	PGA Gain = 1		2.86		mV/°C
Gain Error (±1σ)	PGA Gain = 1		± 33.5		µV/°C
Offset	PGA Gain = 1, Temp = 0°C		776		mV
Offset Error (±1σ)	PGA Gain = 1, Temp = 0°C		± 8.51		mV
POWER SPECIFICATIONS					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100ksps		450	900	µA
Power Supply Rejection			± 0.3		mV/V

Figure 10.2. Memory Map



10.2.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The MCUs also have built-in hardware for a stack record. The stack record is a 32-bit shift register, where each Push or increment SP pushes one record bit onto the register, and each Call or interrupt pushes two record bits onto the register. (A Pop or decrement SP pops one record bit, and a Return pops two record bits, also.) The stack record circuitry can also detect an overflow or underflow on the Stack, and can notify the debug software even with the MCU running full-speed debug.

Figure 10.11. EIE1: Extended Interrupt Enable 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ECP1R	ECP1F	ECP0R	ECP0F	EPCA0	EWADC0	ESMB0	ESPI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE6

Bit7: ECP1R: Enable Comparator 1 (CP1) Rising Edge Interrupt.
This bit sets the masking of the CP1 interrupt.
0: Disable CP1 Rising Edge interrupt.
1: Enable interrupt requests generated by the CP1RIF flag (CPT1CN.5).

Bit6: ECP1F: Enable Comparator 1 (CP1) Falling Edge Interrupt.
This bit sets the masking of the CP1 interrupt.
0: Disable CP1 Falling Edge interrupt.
1: Enable interrupt requests generated by the CP1FIF flag (CPT1CN.4).

Bit5: ECP0R: Enable Comparator 0 (CP0) Rising Edge Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 Rising Edge interrupt.
1: Enable interrupt requests generated by the CP0RIF flag (CPT0CN.5).

Bit4: ECP0F: Enable Comparator 0 (CP0) Falling Edge Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 Falling Edge interrupt.
1: Enable interrupt requests generated by the CP0FIF flag (CPT0CN.4).

Bit3: EPCA0: Enable Programmable Counter Array (PCA0) Interrupt.
This bit sets the masking of the PCA0 interrupts.
0: Disable all PCA0 interrupts.
1: Enable interrupt requests generated by PCA0.

Bit2: EWADC0: Enable Window Comparison ADC0 Interrupt.
This bit sets the masking of ADC0 Window Comparison interrupt.
0: Disable ADC0 Window Comparison Interrupt.
1: Enable Interrupt requests generated by ADC0 Window Comparisons.

Bit1: ESMB0: Enable SMBus 0 Interrupt.
This bit sets the masking of the SMBus interrupt.
0: Disable all SMBus interrupts.
1: Enable interrupt requests generated by the SI flag (SMB0CN.3).

Bit0: ESPI0: Enable Serial Peripheral Interface 0 Interrupt.
This bit sets the masking of SPI0 interrupt.
0: Disable all SPI0 interrupts.
1: Enable Interrupt requests generated by SPI0.

11.2. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX instruction and read using the MOVC instruction.

The MCU incorporates an additional 128-byte sector of Flash memory located at 0x8000 – 0x807F. This sector can be used for program code or data storage. However, its smaller sector size makes it particularly well suited as general purpose, non-volatile scratchpad memory. Even though Flash memory can be written a single byte at a time, an entire sector must be erased first. In order to change a single byte of a multi-byte data set, the data must be moved to temporary storage. Next, the sector is erased, the data set updated and the data set returned to the original sector. The 128-byte sector-size facilitates updating data without wasting program memory space by allowing the use of internal data RAM for temporary storage. (A normal 512-byte sector is too large to be stored in the 256-byte internal data memory.)

11.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as prevent the viewing of proprietary program code and constants. The Program Store Write Enable (PSCTL.0) and the Program Store Erase Enable (PSCTL.1) bits protect the Flash memory from accidental modification by software. These bits must be explicitly set to logic 1 before software can modify the Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the JTAG interface or by software running on the system controller.

A set of security lock bytes stored at 0x7DFE and 0x7DFF protect the Flash program memory from being read or altered across the JTAG interface. Each bit in a security lock-byte protects one 4kbyte block of memory. Clearing a bit to logic 0 in a Read lock byte prevents the corresponding block of Flash memory from being read across the JTAG interface. Clearing a bit in the Write/Erase lock byte protects the block from JTAG erasures and/or writes. The Read lock byte is at location 0x7DFF. The Write/Erase lock byte is located at 0x7DFE. Figure 11.2 shows the location and bit definitions of the security bytes. The 512-byte sector containing the lock bytes can be written to, but not erased by software. Writing to the reserved area should not be performed.

Figure 11.1. PSCTL: Program Store RW Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8F

Bits7-2: UNUSED. Read = 000000b, Write = don't care.

Bit1: PSEE: Program Store Erase Enable.
Setting this bit allows an entire page of the Flash program memory to be erased provided the PSWE bit is also set. After setting this bit, a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.

Bit0: PSWE: Program Store Write Enable.
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX instruction. The location must be erased before writing data.
0: Write to Flash program memory disabled.
1: Write to Flash program memory enabled.

13.8.1. Watchdog Usage

The WDT consists of a 21-bit timer running from the programmed system clock. The timer measures the period between specific writes to its control register. If this period exceeds the programmed limit, a WDT reset is generated. The WDT can be enabled and disabled as needed in software, or can be permanently enabled if desired. Watchdog features are controlled via the Watchdog Timer Control Register (WDTCN) shown in Figure 13.3.

Enable/Reset WDT

The watchdog timer is both enabled and the countdown restarted by writing 0xA5 to the WDTCN register. The user's application software should include periodic writes of 0xA5 to WDTCN as needed to prevent a watchdog timer overflow. The WDT is enabled and restarted as a result of any system reset.

Disable WDT

Writing 0xDE followed by 0xAD to the WDTCN register disables the WDT. The following code segment illustrates disabling the WDT.

```
CLR   EA          ; disable all interrupts
MOV   WDTCN,#0DEh ; disable software
MOV   WDTCN,#0ADh ; watchdog timer
SETB  EA          ; re-enable interrupts
```

The writes of 0xDE and 0xAD must occur within 4 clock cycles of each other, or the disable operation is ignored. Interrupts should be disabled during this procedure to avoid delay between the two writes.

Disable WDT Lockout

Writing 0xFF to WDTCN locks out the disable feature. Once locked out, the disable operation is ignored until the next system reset. Writing 0xFF does not enable or reset the watchdog timer. Applications always intending to use the watchdog should write 0xFF to WDTCN in their initialization code.

Setting WDT Interval

WDTCN.[2:0] control the watchdog timeout interval. The interval is given by the following equation:

$$4^{3+WDTCN[2:0]} \times T_{SYSCLK}\text{ , (where } T_{SYSCLK} \text{ is the system clock period).}$$

For a 2MHz system clock, this provides an interval range of 0.032msec to 524msec. WDTCN.7 must be a 0 when setting this interval. Reading WDTCN returns the programmed interval. WDTCN.[2:0] is 111b after a system reset.

Figure 13.3. WDTCN: Watchdog Timer Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								xxxxx111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xFF

Bits7-0: WDT Control
Writing 0xA5 both enables and reloads the WDT.
Writing 0xDE followed within 4 clocks by 0xAD disables the WDT.
Writing 0xFF locks out the disable feature.

Bit4: Watchdog Status Bit (when Read)
Reading the WDTCN.[4] bit indicates the Watchdog Timer Status.
0: WDT is inactive
1: WDT is active

Bits2-0: Watchdog Timeout Interval Bits
The WDTCN.[2:0] bits set the Watchdog Timeout Interval. When writing these bits, WDTCN.7 must be set to 0.

Figure 13.4. RSTSRC: Reset Source Register

R	R/W	R/W	R/W	R	R	R/W	R	Reset Value
JTAGRST	CNVRSEF	C0RSEF	SWRSEF	WDTRSF	MCDRSF	PORSF	PINRSF	xxxxxxxx
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xEF

(Note: Do not use read-modify-write operations on this register.)

Bit7: JTAGRST. JTAG Reset Flag.
0: JTAG is not currently in reset state.
1: JTAG is in reset state.

Bit6: CNVRSEF: Convert Start Reset Source Enable and Flag
Write
0: CNVSTR is not a reset source
1: CNVSTR is a reset source (active low)
Read
0: Source of prior reset was not from CNVSTR
1: Source of prior reset was from CNVSTR

Bit5: C0RSEF: Comparator 0 Reset Enable and Flag
Write
0: Comparator 0 is not a reset source
1: Comparator 0 is a reset source (active low)
Read
Note: The value read from C0RSEF is not defined if Comparator 0 has not been enabled as a reset source.
0: Source of prior reset was not from Comparator 0
1: Source of prior reset was from Comparator 0

Bit4: SWRSF: Software Reset Force and Flag
Write
0: No Effect
1: Forces an internal reset. /RST pin is not effected.
Read
0: Prior reset source was not from write to the SWRSF bit.
1: Prior reset source was from write to the SWRSF bit.

Bit3: WDTRSF: Watchdog Timer Reset Flag
0: Source of prior reset was not from WDT timeout.
1: Source of prior reset was from WDT timeout.

Bit2: MCDRSF: Missing Clock Detector Flag
0: Source of prior reset was not from Missing Clock Detector timeout.
1: Source of prior reset was from Missing Clock Detector timeout.

Bit1: PORSF: Power-On Reset Force and Flag
Write
0: No effect
1: Forces a Power-On Reset. /RST is driven low.
Read
0: Source of prior reset was not from POR.
1: Source of prior reset was from POR.

Bit0: PINRSF: HW Pin Reset Flag
0: Source of prior reset was not from /RST pin.
1: Source of prior reset was from /RST pin.

Figure 17.6. SPI0CN: SPI Control Register

R/W	R/W	R/W	R/W	R	R	R/W	R/W	Reset Value
SPIF	WCOL	MODF	RXOVRN	TXBSY	SLVSEL	MSTEN	SPIEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xF8

Bit7: SPIF: SPI Interrupt Flag.
This bit is set to logic 1 by hardware at the end of a data transfer. If interrupts are enabled, setting this bit causes the CPU to vector to the SPI0 interrupt service routine. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit6: WCOL: Write Collision Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) to indicate a write to the SPI data register was attempted while a data transfer was in progress. It is cleared by software.

Bit5: MODF: Mode Fault Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when a master mode collision is detected (NSS is low and MSTEN = 1). This bit is not automatically cleared by hardware. It must be cleared by software.

Bit4: RXOVRN: Receive Overrun Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when the receive buffer still holds unread data from a previous transfer and the last bit of the current transfer is shifted into the SPI shift register. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit3: TXBSY: Transmit Busy Flag.
This bit is set to logic 1 by hardware while a master mode transfer is in progress. It is cleared by hardware at the end of the transfer.

Bit2: SLVSEL: Slave Selected Flag.
This bit is set to logic 1 whenever the NSS pin is low indicating it is enabled as a slave. It is cleared to logic 0 when NSS is high (slave disabled).

Bit1: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit0: SPIEN: SPI Enable.
This bit enables/disables the SPI.
0: SPI disabled.
1: SPI enabled.

Figure 19.7. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8A

Bits 7-0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

Figure 19.8. TL1: Timer 1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8B

Bits 7-0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

Figure 19.9. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8C

Bits 7-0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

Figure 19.10. TH1: Timer 1 High Byte

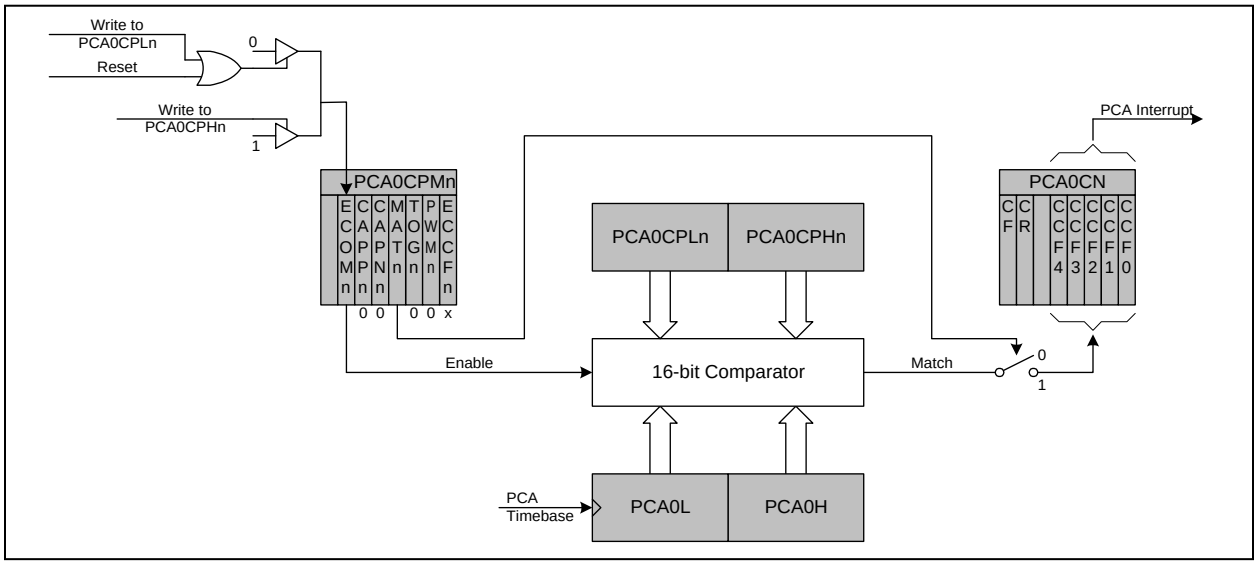
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8D

Bits 7-0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.

20.1.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

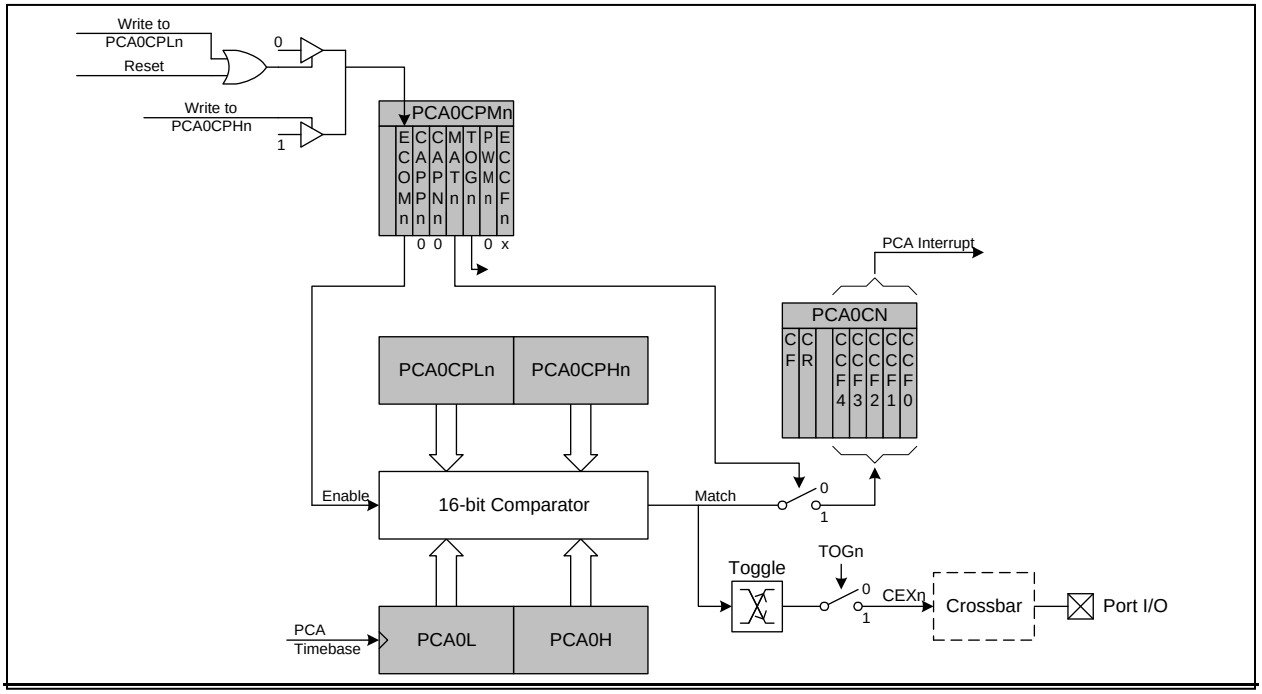
Figure 20.4. PCA Software Timer Mode Diagram



20.1.3. High Speed Output Mode

In this mode, each time a match occurs between the PCA Timer Counter and a module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn) the logic level on the module's associated CEXn pin will toggle. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode.

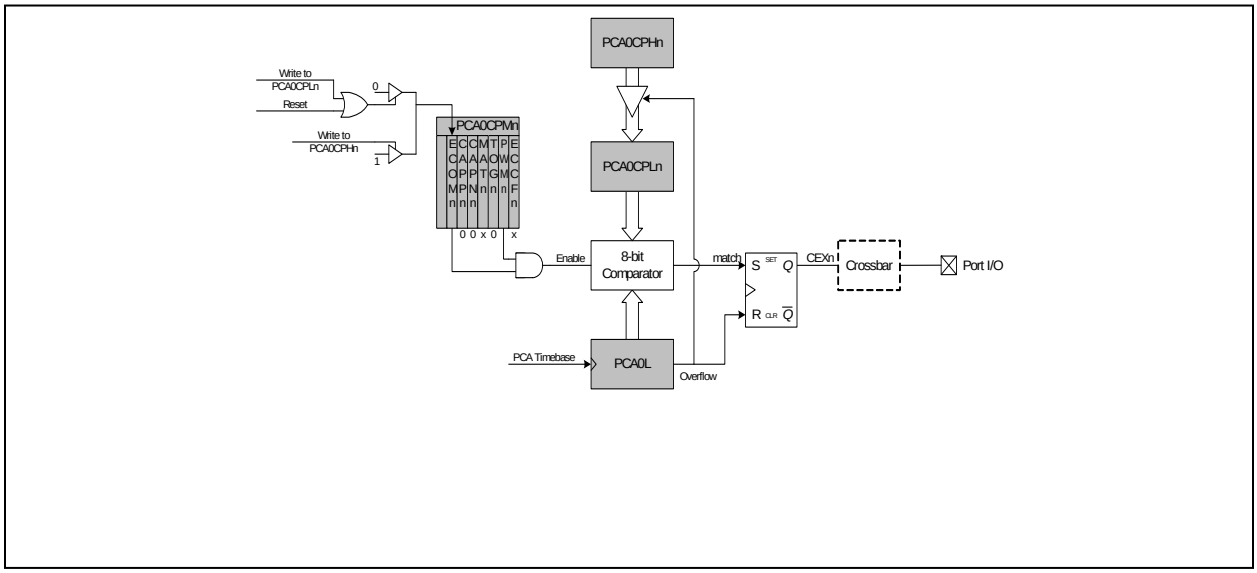
Figure 20.5. PCA High Speed Output Mode Diagram



20.1.4. Pulse Width Modulator Mode

All of the modules can be used independently to generate pulse width modulated (PWM) outputs on their respective CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 20.6). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the PCA0CPHn without software intervention. It is good practice to write to PCA0CPHn instead of PCA0CPLn to avoid glitches in the digital comparator. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables Pulse Width Modulator mode.

Figure 20.6. PCA PWM Mode Diagram



21.1.1. EXTEST Instruction

The EXTEST instruction is accessed via the IR. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature. All inputs to on-chip logic are set to one.

21.1.2. SAMPLE Instruction

The SAMPLE instruction is accessed via the IR. The Boundary DR provides observability and presetting of the scan-path latches.

21.1.3. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard 1-bit JTAG Bypass data register.

21.1.4. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

Figure 21.2. DEVICEID: JTAG Device ID Register

Version	Part Number	Manufacturer ID	1	Reset Value (Varies)
Bit31 Bit28	Bit27 Bit12	Bit11 Bit1	Bit0	

Version = 0000b (Revision A) or
= 0001b (Revision B)

Part Number = 0000 0000 0000 0000b or
= 0000 0000 0000 0010b

Manufacturer ID = 0010 0100 001b (Silicon Laboratories)