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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f016

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1. SYSTEM OVERVIEW

The C8051F000 family are fully integrated mixed-signal System on a Chip MCUs with a true 12-bit multi-channel ADC (F000/01/02/05/06/07), or a true 10-bit multi-channel ADC (F010/11/12/15/16/17). See the Product Selection Guide in Table 1.1 for a quick reference of each MCUs' feature set. Each has a programmable gain pre-amplifier, two 12-bit DACs, two voltage comparators (except for the F002/07/12/17, which have one), a voltage reference, and an 8051-compatible microcontroller core with 32kbytes of FLASH memory. There are also I2C/SMBus, UART, and SPI serial interfaces implemented in hardware (not "bit-banged" in user software) as well as a Programmable Counter/Timer Array (PCA) with five capture/compare modules. There are also 4 general-purpose 16-bit timers and 4 byte-wide general-purpose digital Port I/O. The C8051F000/01/02/10/11/12 have 256 bytes of RAM and execute up to 20MIPS, while the C8051F005/06/07/15/16/17 have 2304 bytes of RAM and execute up to 25MIPS.

With an on-board VDD monitor, WDT, and clock oscillator, the MCUs are truly stand-alone System-on-a-Chip solutions. Each MCU effectively configures and manages the analog and digital peripherals. The FLASH memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. Each MCU can also individually shut down any or all of the peripherals to conserve power.

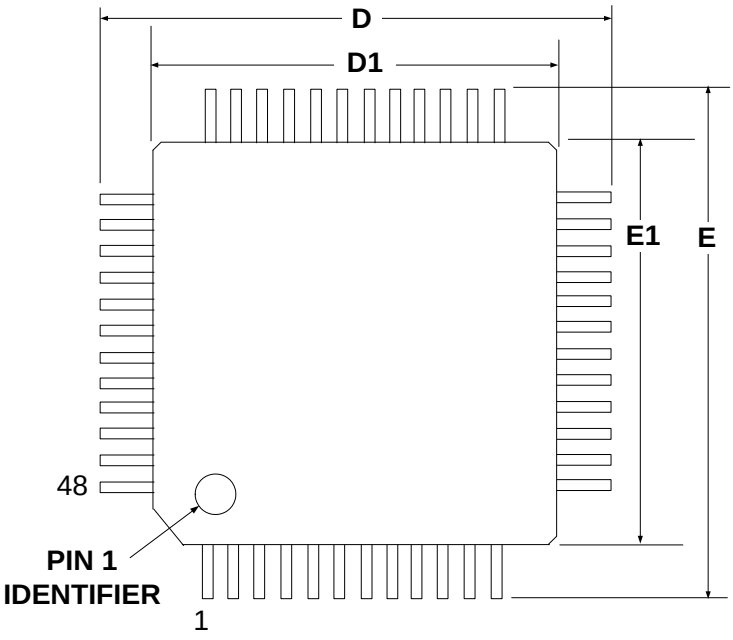
On-board JTAG debug support allows non-intrusive (uses no on-chip resources), full speed, in-circuit debug using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional when using JTAG debug.

Each MCU is specified for 2.7V-to-3.6V operation over the industrial temperature range (-45C to +85C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5V. The C8051F000/05/10/15 are available in the 64-pin TQFP (see block diagram in Figure 1.1). The C8051F001/06/11/16 are available in the 48-pin TQFP (see block diagram in Figure 1.2). The C8051F002/07/12/17 are available in the 32-pin LQFP (see block diagram in Figure 1.3).

Table 1.1. Product Selection Guide

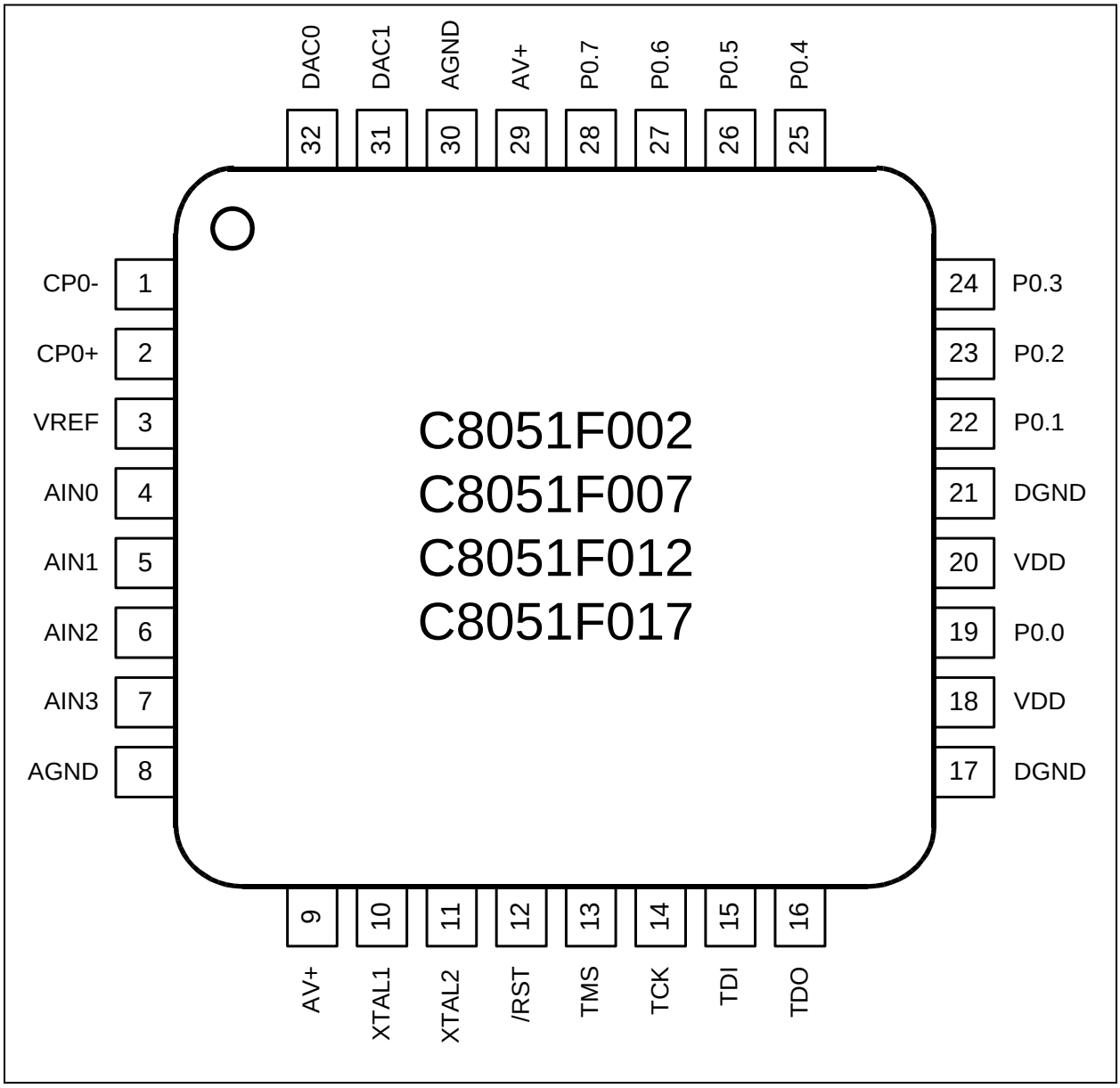
	MIPS (Peak)	FLASH Memory	RAM	SMBus/I2C	SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	ADC Resolution (bits)	ADC Max Speed (ksps)	ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution	DAC Outputs	Voltage Comparators	Package
C8051F000	20	32k	256	√	√	√	4	√	32	12	100	8	√	√	12	2	2	64TQFP
C8051F001	20	32k	256	√	√	√	4	√	16	12	100	8	√	√	12	2	2	48TQFP
C8051F002	20	32k	256	√	√	√	4	√	8	12	100	4	√	√	12	2	1	32LQFP
C8051F005	25	32k	2304	√	√	√	4	√	32	12	100	8	√	√	12	2	2	64TQFP
C8051F006	25	32k	2304	√	√	√	4	√	16	12	100	8	√	√	12	2	2	48TQFP
C8051F007	25	32k	2304	√	√	√	4	√	8	12	100	4	√	√	12	2	1	32LQFP
C8051F010	20	32k	256	√	√	√	4	√	32	10	100	8	√	√	12	2	2	64TQFP
C8051F011	20	32k	256	√	√	√	4	√	16	10	100	8	√	√	12	2	2	48TQFP
C8051F012	20	32k	256	√	√	√	4	√	8	10	100	4	√	√	12	2	1	32LQFP
C8051F015	25	32k	2304	√	√	√	4	√	32	10	100	8	√	√	12	2	2	64TQFP
C8051F016	25	32k	2304	√	√	√	4	√	16	10	100	8	√	√	12	2	2	48TQFP
C8051F017	25	32k	2304	√	√	√	4	√	8	10	100	4	√	√	12	2	1	32LQFP

Figure 4.4. TQFP-48 Package Drawing



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	9.00	-
D1	-	7.00	-
e	-	0.50	-
E	-	9.00	-
E1	-	7.00	-

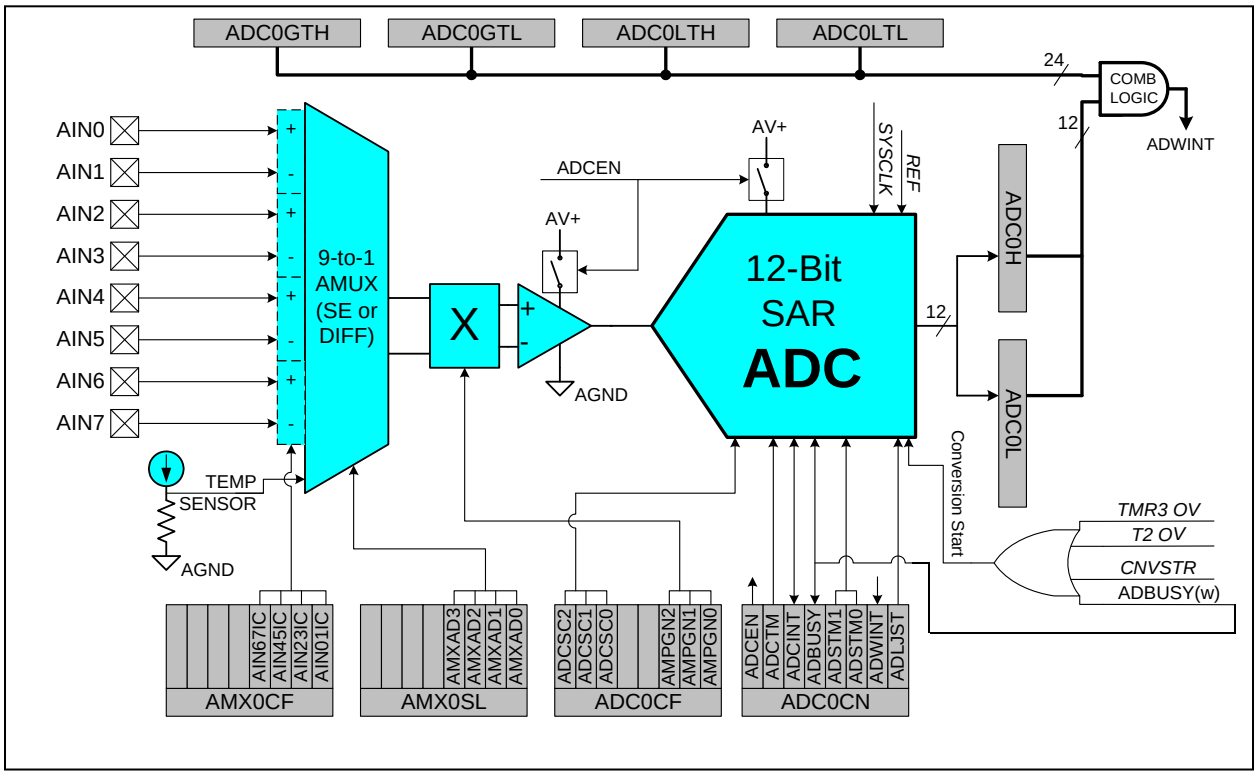
Figure 4.5. LQFP-32 Pinout Diagram



5. ADC (12-Bit, C8051F000/1/2/5/6/7 Only)

The ADC subsystem for the C8051F000/1/2/5/6/7 consists of a 9-channel, configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 12-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector (see block diagram in Figure 5.1). The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Register's shown in Figure 5.1. The ADC subsystem (ADC, track-and-hold and PGA) is enabled only when the ADCEN bit in the ADC Control register (ADC0CN, Figure 5.7) is set to 1. The ADC subsystem is in low power shutdown when this bit is 0. The Bias Enable bit (BIASE) in the REF0CN register (see Figure 9.2) must be set to 1 in order to supply bias to the ADC.

Figure 5.1. 12-Bit ADC Functional Block Diagram



5.1. Analog Multiplexer and PGA

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-board temperature sensor (temperature transfer function is shown in Figure 5.3). Note that the PGA gain is applied to the temperature sensor reading. AMUX input pairs can be programmed to operate in either the differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (Figure 5.5), and the Configuration register AMX0CF (Figure 5.4). The table in Figure 5.5 shows AMUX functionality by channel for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the AMPGN2-0 bits in the ADC Configuration register, ADC0CF (Figure 5.6). The PGA can be software-programmed for gains of 0.5, 1, 2, 4, 8 or 16. It defaults to unity gain on reset.

Figure 5.7. ADC0CN: ADC Control Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCEN	ADCTM	ADCINT	ADBUSY	ADSTM1	ADSTM0	ADWINT	ADLJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xE8

Bit7: ADCEN: ADC Enable Bit
0: ADC Disabled. ADC is in low power shutdown.
1: ADC Enabled. ADC is active and ready for data conversions.

Bit6: ADCTM: ADC Track Mode Bit
0: When the ADC is enabled, tracking is always done unless a conversion is in process
1: Tracking Defined by ADSTM1-0 bits
ADSTM1-0:
00: Tracking starts with the write of 1 to ADBUSY and lasts for 3 SAR clocks
01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks
10: ADC tracks only when CNVSTR input is logic low
11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks

Bit5: ADCINT: ADC Conversion Complete Interrupt Flag
(Must be cleared by software)
0: ADC has not completed a data conversion since the last time this flag was cleared
1: ADC has completed a data conversion

Bit4: ADBUSY: ADC Busy Bit
Read
0: ADC Conversion complete or no valid data has been converted since a reset. The falling edge of ADBUSY generates an interrupt when enabled.
1: ADC Busy converting data
Write
0: No effect
1: Starts ADC Conversion if ADSTM1-0 = 00b

Bits3-2: ADSTM1-0: ADC Start of Conversion Mode Bits
00: ADC conversion started upon every write of 1 to ADBUSY
01: ADC conversions taken on every overflow of Timer 3
10: ADC conversion started upon every rising edge of CNVSTR
11: ADC conversions taken on every overflow of Timer 2

Bit1: ADWINT: ADC Window Compare Interrupt Flag
(Must be cleared by software)
0: ADC Window Comparison Data match has not occurred
1: ADC Window Comparison Data match occurred

Bit0: ADLJST: ADC Left Justify Data Bit
0: Data in ADC0H:ADC0L Registers is right justified
1: Data in ADC0H:ADC0L Registers is left justified

5.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Figure 5.14 and Figure 5.15 show example comparisons for reference. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 5.10. ADC0GTH: ADC Greater-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC5

Bits7-0:
The high byte of the ADC Greater-Than Data Word.

Figure 5.11. ADC0GTL: ADC Greater-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC4

Bits7-0:
The low byte of the ADC Greater-Than Data Word.
Definition:
ADC Greater-Than Data Word = ADC0GTH:ADC0GTL

Figure 5.12. ADC0LTH: ADC Less-Than Data High Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC7

Bits7-0:
The high byte of the ADC Less-Than Data Word.

Figure 5.13. ADC0LTL: ADC Less-Than Data Low Byte Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC6

Bits7-0:
These bits are the low byte of the ADC Less-Than Data Word.
Definition:
ADC Less-Than Data Word = ADC0LTH:ADC0LTL

10. CIP-51 CPU

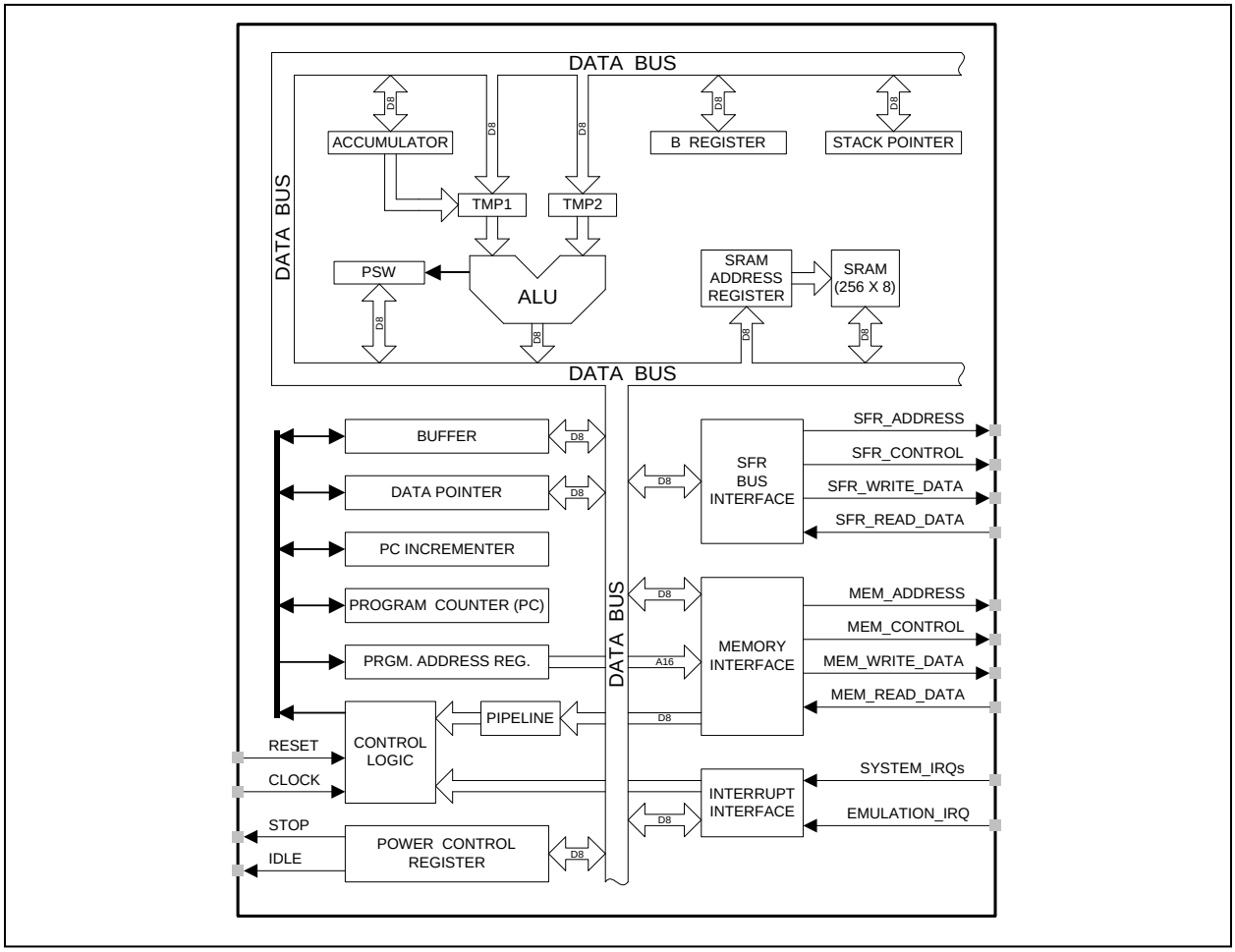
The MCUs' system CPU is the CIP-51. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. Included are four 16-bit counter/timers (see description in Section 19), a full-duplex UART (see description in Section 18), 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space (see Section 10.3), and four byte-wide I/O Ports (see description in Section 14). The CIP-51 also includes on-chip debug hardware (see description in Section 21), and interfaces directly with the MCUs' analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

Features

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 10.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25MHz Clock
- 0 to 25MHz Clock Frequency (on 'F0x5/6/7)
- Four Byte-Wide I/O Ports
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Circuitry
- Program and Data Memory Security

Figure 10.1. CIP-51 Block Diagram



Mnemonic	Description	Bytes	Clock Cycles
PROGRAM BRANCHING			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A,direct,rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A,#data,rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn,#data,rel	Compare immediate to register and jump if not equal	3	3/4
CJNE @Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn,rel	Decrement register and jump if not zero	2	2/3
DJNZ direct,rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:

Rn - Register R0-R7 of the currently selected register bank.

@Ri - Data RAM location addressed indirectly through register R0-R1

rel - 8-bit, signed (two's compliment) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

direct - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00-0x7F) or an SFR (0x80-0xFF).

#data - 8-bit constant

#data 16 - 16-bit constant

bit - Direct-addressed bit in Data RAM or SFR.

addr 11 - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2K-byte page of program memory as the first byte of the following instruction.

addr 16 - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 64K-byte program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.

not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an open-drain output that is driving a 0 to avoid unnecessary power dissipation.

The third and final step is to initialize the individual resources selected using the appropriate setup registers. Initialization procedures for the various digital resources may be found in the detailed explanation of each available function. The reset state of each register is shown in the figures that describe each individual register.

Figure 15.1. Port I/O Functional Block Diagram

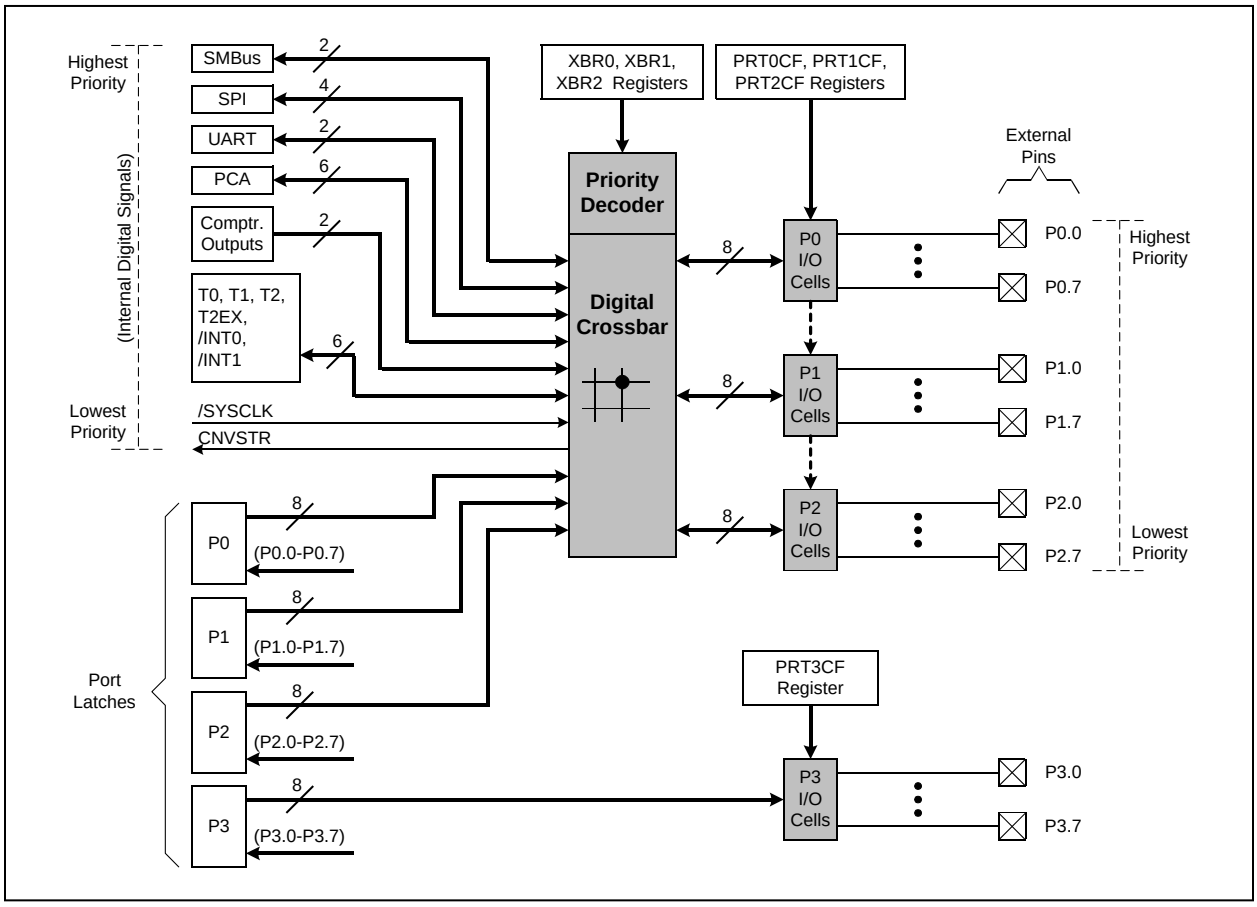


Figure 15.2. Port I/O Cell Block Diagram

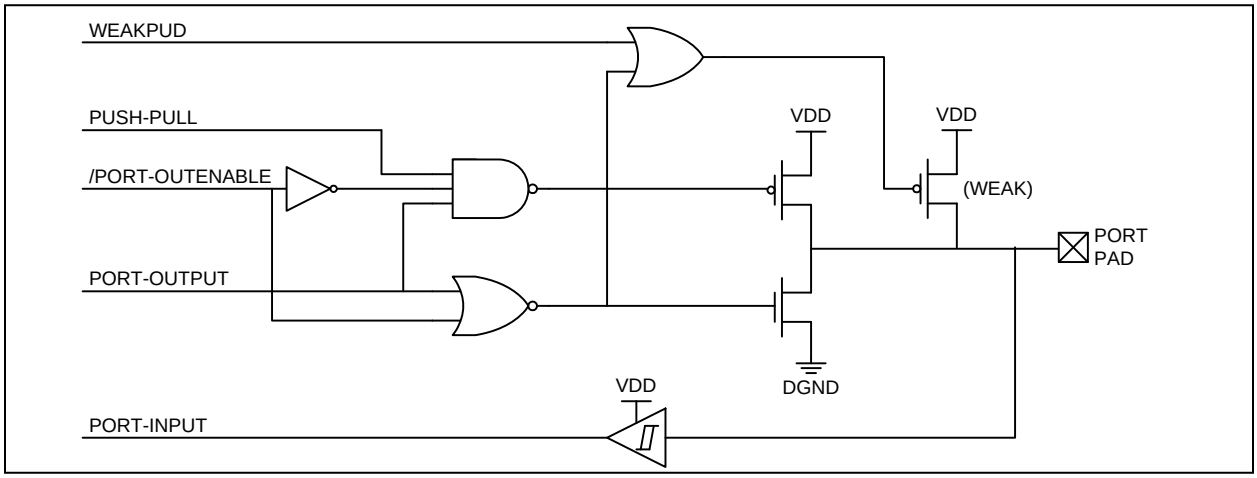


Figure 15.13. P3: Port3 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xB0

Bits7-0: P3.[7:0]
(Write)
0: Logic Low Output.
1: Logic High Output (high-impedance if corresponding PRT3CF.n bit = 0)
(Read)
0: P3.n is logic low.
1: P3.n is logic high.

Figure 15.14. PRT3CF: Port3 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA7

Bits7-0: PRT3CF.[7:0]: Output Configuration Bits for P3.7-P3.0 (respectively)
0: Corresponding P3.n Output mode is Open-Drain.
1: Corresponding P3.n Output mode is Push-Pull.

Table 15.2. Port I/O DC Electrical Characteristics

VDD = 2.7 to 3.6V, -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	I_{OH} = -10uA, Port I/O push-pull I_{OH} = -3mA, Port I/O push-pull I_{OH} = -10mA, Port I/O push-pull	VDD – 0.1 VDD – 0.7	 VDD – 0.8		V
Output Low Voltage	I_{OL} = 10uA I_{OL} = 8.5mA I_{OL} = 25mA		 1.0	0.1 0.6	V
Input High Voltage		0.7 x VDD			V
Input Low Voltage				0.3 x VDD	V
Input Leakage Current	DGND < Port Pin < VDD, Pin Tri-state Weak Pull-up Off Weak Pull-up On		 30	 ±1	µA
Capacitive Loading			5		pF

16.6.3. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Data remains stable in the register as long as SI is set to logic 1. Software can safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0 since the hardware may be in the process of shifting a byte of data in or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. Therefore, SMB0DAT always contains the last data byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in SMB0DAT.

Figure 16.6. SMB0DAT: SMBus Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC2

Bits7-0: SMB0DAT: SMBus Data.
The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.3) is set to logic one. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

16.6.4. Address Register

The SMB0ADR Address register holds the slave address for the SMBus interface. In slave mode, the seven most-significant bits hold the 7-bit slave address. The least significant bit, bit 0, is used to enable the recognition of the general call address (0x00). If bit 0 is set to logic 1, the general call address will be recognized. Otherwise, the general call address is ignored. The contents of this register are ignored when the SMBus hardware is operating in master mode.

Figure 16.7. SMB0ADR: SMBus Address Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SLV6	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0	GC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC3

Bits7-1: SLV6-SLV0: SMBus Slave Address.
These bits are loaded with the 7-bit slave address to which the SMBus will respond when operating as a slave transmitter or slave receiver. SLV6 is the most significant bit of the address and corresponds to the first bit of the address byte received on the SMBus.

Bit0: GC: General Call Address Enable.
This bit is used to enable general call address (0x00) recognition.
0: General call address is ignored.
1: General call address is recognized.

Table 16.1. SMBus Status Codes

Status Code (SMB0STA)	Mode	**SMBus State**
0x00	All	Bus Error (i.e. illegal START, illegal STOP, …)
0x08	Master Transmitter/Receiver	START condition transmitted.
0x10	Master Transmitter/Receiver	Repeated START condition transmitted.
0x18	Master Transmitter	Slave address + W transmitted. ACK received.
0x20	Master Transmitter	Slave address + W transmitted. NACK received.
0x28	Master Transmitter	Data byte transmitted. ACK received.
0x30	Master Transmitter	Data byte transmitted. NACK received.
0x38	Master Transmitter	Arbitration lost
0x40	Master Receiver	Slave address + R transmitted. ACK received.
0x48	Master Receiver	Slave address + R transmitted. NACK received
0x50	Master Receiver	Data byte received. ACK transmitted.
0x58	Master Receiver	Data byte received. NACK transmitted.
0x60	Slave Receiver	SMB0's own slave address + W received. ACK transmitted.
0x68	Slave Receiver	Arbitration lost in transmitting slave address + R/W as master. Own slave address + W received. ACK transmitted.
0x70	Slave Receiver	General call address (0x00) received. ACK returned.
0x78	Slave Receiver	Arbitration lost in transmitting slave address + R/W as master. General call address received. ACK transmitted.
0x80	Slave Receiver	SMB0's own slave address + W received. Data byte received. ACK transmitted.
0x88	Slave Receiver	SMB0's own slave address + W received. Data byte received. NACK transmitted.
0x90	Slave Receiver	General call address (0x00) received. Data byte received. ACK transmitted.
0x98	Slave Receiver	General call address (0x00) received. Data byte received. NACK transmitted.
0xA0	Slave Receiver	A STOP or repeated START received while addressed as a slave.
0xA8	Slave Transmitter	SMB0's own slave address + R received. ACK transmitted.
0xB0	Slave Transmitter	Arbitration lost in transmitting slave address + R/W as master. Own slave address + R received. ACK transmitted.
0xB8	Slave Transmitter	Data byte transmitted. ACK received.
0xC0	Slave Transmitter	Data byte transmitted. NACK received.
0xC8	Slave Transmitter	Last data byte transmitted (AA=0). ACK received.
0xD0	Slave Transmitter/Receiver	SCL Clock High Timer per SMB0CR timed out (FTE=1)
0xF8	All	Idle

19. TIMERS

Each MCU implements four counter/timers: three are 16-bit counter/timers compatible with those found in the standard 8051, and one is a 16-bit timer for use with the ADC, SMBus, or for general purpose use. These can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 offers additional capabilities not available in Timers 0 and 1. Timer 3 is similar to Timer 2, but without the capture or Baud Rate Generator modes.

Timer 0 and Timer 1:	Timer 2:	Timer 3:
13-bit counter/timer	16-bit counter/timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer	16-bit counter/timer with capture	
8-bit counter/timer with auto-reload	Baud rate generator	
Two 8-bit counter/timers (Timer 0 only)		

When functioning as a timer, the counter/timer registers are incremented on each clock tick. Clock ticks are derived from the system clock divided by either one or twelve as specified by the Timer Clock Select bits (T2M-T0M) in CKCON. The twelve-clocks-per-tick option provides compatibility with the older generation of the 8051 family. Applications that require a faster timer can use the one-clock-per-tick option.

When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin for T0, T1, or T2. Events with a frequency of up to one-fourth the system clock's frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is sampled.

19.1. Timer 0 and Timer 1

Timer 0 and Timer 1 are accessed and controlled through SFRs. Each counter/timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control (TCON) register is used to enable Timer 0 and Timer 1 as well as indicate their status. Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits M1-M0 in the Counter/Timer Mode (TMOD) register. Each timer can be configured independently. Following is a detailed description of each operating mode.

19.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as a 13-bit counter/timer in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4-TL0.0. The three upper bits of TL0 (TL0.7-TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. Clearing C/T selects the system clock as the input for the timer. When C/T0 is set to logic 1, high-to-low transitions at the selected input pin increment the timer register. (Refer to Port I/O Section 15.1 for information on selecting and configuring external I/O pins.)

Figure 19.7. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8A

Bits 7-0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

Figure 19.8. TL1: Timer 1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8B

Bits 7-0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

Figure 19.9. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8C

Bits 7-0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

Figure 19.10. TH1: Timer 1 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8D

Bits 7-0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.

19.2. Timer 2

Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFRs: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. (Refer to Section 14 for information on selecting and configuring external I/O pins.) Timer 2 can also be used to start an ADC Data Conversion.

Timer 2 offers capabilities not found in Timer 0 and Timer 1. It operates in one of three modes: 16-bit Counter/Timer with Capture, 16-bit Counter/Timer with Auto-Reload or Baud Rate Generator Mode. Timer 2's operating mode is selected by setting configuration bits in the Timer 2 Control (T2CON) register. Below is a summary of the Timer 2 operating modes and the T2CON bits used to configure the counter/timer. Detailed descriptions of each mode follow.

RCLK	TCLK	CP/RL2	TR2	Mode
0	0	1	1	16-bit Counter/Timer with Capture
0	0	0	1	16-bit Counter/Timer with Auto-Reload
0	1	X	1	Baud Rate Generator for TX
1	0	X	1	Baud Rate Generator for RX
1	1	X	1	Baud Rate Generator for TX and RX
X	X	X	0	Off

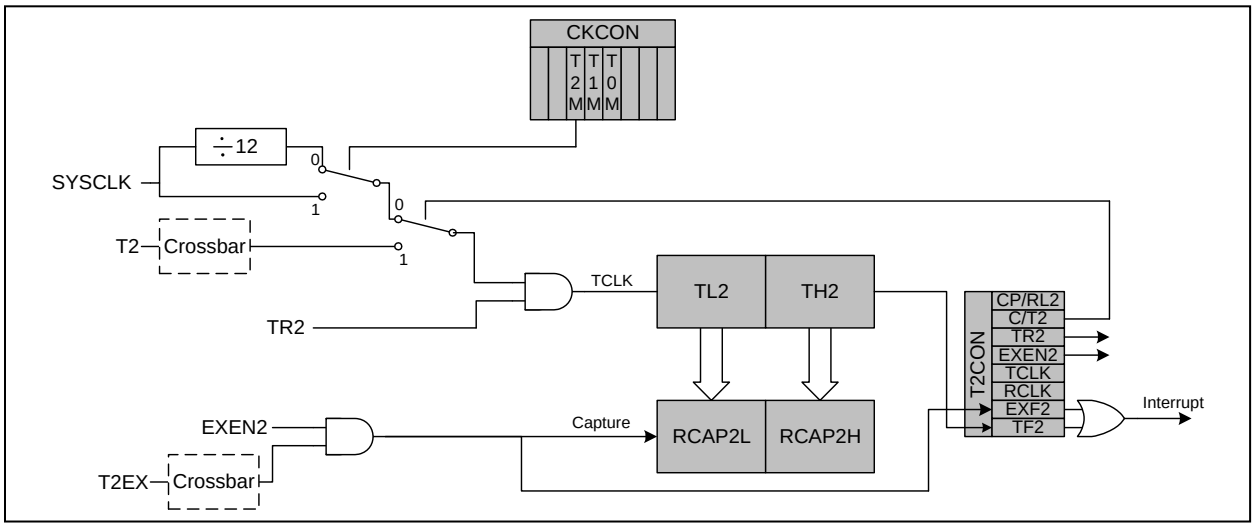
19.2.1. Mode 0: 16-bit Counter/Timer with Capture

In this mode, Timer 2 operates as a 16-bit counter/timer with capture facility. A high-to-low transition on the T2EX input pin causes the 16-bit value in Timer 2 (TH2, TL2) to be loaded into the capture registers (RCAP2H, RCAP2L).

Timer 2 can use either SYSCLK, SYSCLK divided by 12, or high-to-low transitions on the external T2 pin as its clock source when operating in Counter/Timer with Capture mode. Clearing the C/T2 bit (T2CON.1) selects the system clock as the input for the timer (divided by one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to logic 1, a high-to-low transition at the T2 input pin increments the counter/timer register. As the 16-bit counter/timer register increments and overflows from 0xFFFF to 0x0000, the TF2 timer overflow flag (T2CON.7) is set and an interrupt will occur if the interrupt is enabled.

Counter/Timer with Capture mode is selected by setting the Capture/Reload Select bit CP/RL2 (T2CON.0) and the Timer 2 Run Control bit TR2 (T2CON.2) to logic 1. The Timer 2 External Enable EXEN2 (T2CON.3) must also be set to logic 1 to enable a capture. If EXEN2 is cleared, transitions on T2EX will be ignored.

Figure 19.11. T2 Mode 0 Block Diagram



19.2.3. Mode 2: Baud Rate Generator

Timer 2 can be used as a baud rate generator for the serial port (UART) when the UART is operated in modes 1 or 3 (refer to Section 18.1 for more information on UART operational modes). In Baud Rate Generator mode, Timer 2 works similarly to the auto-reload mode. On overflow, the 16-bit value held in the two capture registers (RCAP2H, RCAP2L) is automatically loaded into the counter/timer register. However, the TF2 overflow flag is not set and no interrupt is generated. Instead, the overflow event is used as the input to the UART's shift clock. Timer 2 overflows can be used to generate baud rates for transmit and/or receive independently.

The Baud Rate Generator mode is selected by setting RCLK (T2CON.5) and/or TCLK (T2CON.4) to logic one. When RCLK or TCLK is set to logic 1, Timer 2 operates in the auto-reload mode regardless of the state of the CP/RL2 bit. The baud rate for the UART, when operating in mode 1 or 3, is determined by the Timer 2 overflow rate:

Baud Rate = Timer 2 Overflow Rate / 16.

Note, in all other modes, the timebase for the timer is the system clock divided by one or twelve as selected by the T2M bit in CKCON. However, in Baud Rate Generator mode, the timebase is the system clock divided by two. No other divisor selection is possible. If a different time base is required, setting the C/T2 bit to logic 1 will allow the timebase to be derived from the external input pin T2. In this case, the baud rate for the UART is calculated as:

*Baud Rate = FCLK / [32 * (65536 – [RCAP2H:RCAP2L])]*

Where FCLK is the frequency of the signal supplied to T2 and [RCAP2H:RCAP2L] is the 16-bit value held in the capture registers.

As explained above, in Baud Rate Generator mode, Timer 2 does not set the TF2 overflow flag and therefore cannot generate an interrupt. However, if EXEN2 is set to logic 1, a high-to-low transition on the T2EX input pin will set the EXF2 flag and a Timer 2 interrupt will occur if enabled. Therefore, the T2EX input may be used as an additional external interrupt source.

Figure 19.13. T2 Mode 2 Block Diagram

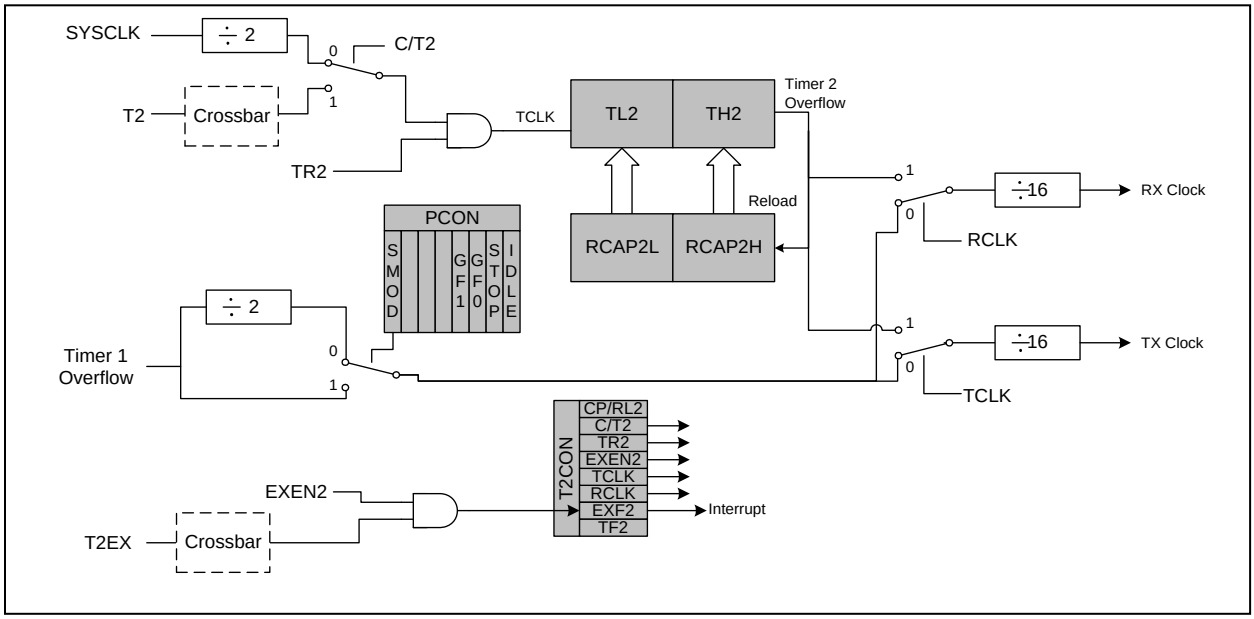


Figure 19.14. T2CON: Timer 2 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xC8

Bit7: TF2: Timer 2 Overflow Flag.
Set by hardware when Timer 2 overflows from 0xFFFF to 0x0000 or reload value. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. TF2 will not be set when RCLK and/or TCLK are logic 1.

Bit6: EXF2: Timer 2 External Flag.
Set by hardware when either a capture or reload is caused by a high-to-low transition on the T2EX input pin and EXEN2 is logic 1. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 Interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit5: RCLK: Receive Clock Flag.
Selects which timer is used for the UART's receive clock in modes 1 or 3.
0: Timer 1 overflows used for receive clock.
1: Timer 2 overflows used for receive clock.

Bit4: TCLK: Transmit Clock Flag.
Selects which timer is used for the UART's transmit clock in modes 1 or 3.
0: Timer 1 overflows used for transmit clock.
1: Timer 2 overflows used for transmit clock.

Bit3: EXEN2: Timer 2 External Enable.
Enables high-to-low transitions on T2EX to trigger captures or reloads when Timer 2 is not operating in Baud Rate Generator mode.
0: High-to-low transitions on T2EX ignored.
1: High-to-low transitions on T2EX cause a capture or reload.

Bit2: TR2: Timer 2 Run Control.
This bit enables/disables Timer 2.
0: Timer 2 disabled.
1: Timer 2 enabled.

Bit1: C/T2: Counter/Timer Select.
0: Timer Function: Timer 2 incremented by clock defined by T2M (CKCON.5).
1: Counter Function: Timer 2 incremented by high-to-low transitions on external input pin (T2).

Bit0: CP/RL2: Capture/Reload Select.
This bit selects whether Timer 2 functions in capture or auto-reload mode. EXEN2 must be logic 1 for high-to-low transitions on T2EX to be recognized and used to trigger captures or reloads. If RCLK or TCLK is set, this bit is ignored and Timer 2 will function in auto-reload mode.
0: Auto-reload on Timer 2 overflow or high-to-low transition at T2EX (EXEN2 = 1).
1: Capture on high-to-low transition at T2EX (EXEN2 = 1).

Figure 21.3. FLASHCON: JTAG Flash Control Register

WRMD3	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bits7-4: WRMD3-0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
0000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
0001: A FLASHDAT write initiates a write of FLASHDAT into the memory location addressed by the FLASHADR register. FLASHADR is incremented by one when complete.
0010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. FLASHDAT must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR = 0x7DFE – 0x7DFF, the entire user space will be erased (i.e. entire Flash memory except for Reserved area 0x7E00 – 0x7FFF).
(All other values for WRMD3-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
0000: A FLASHDAT read provides the data in the FASHDAT register, but is otherwise ignored.
0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
(All other values for RDMD3-0 are reserved.)

Figure 21.4. FLASHADR: JTAG Flash Address Register

																Reset Value
																0x0000
Bit15															Bit0	

This register holds the address for all JTAG Flash read, write, and erase operations. This register autoincrements after each read or write, regardless of whether the operation succeeded or failed.

Bits15-0: Flash Operation 16-bit Address.