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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f017-gqr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.7. Analog to Digital Converter

The C8051F000/1/2/5/6/7 has an on-chip 12-bit SAR ADC with a 9-channel input multiplexer and programmable gain amplifier. With a maximum throughput of 100ksps, the ADC offers true 12-bit accuracy with an INL of \pm 1LSB. The ADC in the C8051F010/1/2/5/6/7 is similar, but with 10-bit resolution. Each ADC has a maximum throughput of 100ksps. Each ADC has an INL of \pm 1LSB, offering true 12-bit accuracy with the C8051F00x, and true 10-bit accuracy with the C8051F01x. There is also an on-board 15ppm voltage reference, or an external reference may be used via the VREF pin.

The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. One input channel is tied to an internal temperature sensor, while the other eight channels are available externally. Each pair of the eight external input channels can be configured as either two single-ended inputs or a single differential input. The system controller can also put the ADC into shutdown to save power.

A programmable gain amplifier follows the analog multiplexer. The gain can be set in software from 0.5 to 16 in powers of 2. The gain stage can be especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset (in differential mode, a DAC could be used to provide the DC offset).

Conversions can be started in four ways; a software command, an overflow on Timer 2, an overflow on Timer 3, or an external signal input. This flexibility allows the start of conversion to be triggered by software events, external HW signals, or convert continuously. A completed conversion causes an interrupt, or a status bit can be polled in software to determine the end of conversion. The resulting 10 or 12-bit data word is latched into two SFRs upon completion of a conversion. The data can be right or left justified in these registers under software control.

Compare registers for the ADC data can be configured to interrupt the controller when ADC data is within a specified window. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within the specified window.



Figure 1.10. ADC Diagram



1.8. Comparators and DACs

The C8051F000 MCU Family has two 12-bit DACs and two comparators on chip (the second comparator, CP1, is not bonded out on the F002, F007, F012, and F017). The MCU data and control interface to each comparator and DAC is via the Special Function Registers. The MCU can place any DAC or comparator in low power shutdown mode.

The comparators have software programmable hysteresis. Each comparator can generate an interrupt on its rising edge, falling edge, or both. The comparators' output state can also be polled in software. These interrupts are capable of waking up the MCU from idle mode. The comparator outputs can be programmed to appear on the Port I/O pins via the Crossbar.

The DACs are voltage output mode and use the same voltage reference as the ADC. They are especially useful as references for the comparators or offsets for the differential inputs of the ADC.



Figure 1.11. Comparator and DAC Diagram



	Pin	Numb	oers		
Nama	F000	F001	F002	Type	Description
Ivallie	F005 F010	F006 F011	F007 F012	Type	Description
	F015	F016	F012		
AIN6	13	10		A In	Analog Mux Channel Input 6. (See ADC Specification for complete
					description).
ALN7	14	11		A In	Analog Mux Channel Input 7. (See ADC Specification for complete description)
P0.0	30	31	19	D I/O	Port0 Bit0. (See the Port I/O Sub-System section for complete description).
P0.1	42	34	22	D I/O	Port0 Bit1. (See the Port I/O Sub-System section for complete description).
P0.2	47	35	23	D I/O	Port0 Bit2. (See the Port I/O Sub-System section for complete description).
P0.3	48	36	24	D I/O	Port0 Bit3. (See the Port I/O Sub-System section for complete description).
P0.4	49	37	25	D I/O	Port0 Bit4. (See the Port I/O Sub-System section for complete description).
P0.5	50	38	26	D I/O	Port0 Bit5. (See the Port I/O Sub-System section for complete description).
P0.6	55	39	27	D I/O	Port0 Bit6. (See the Port I/O Sub-System section for complete description).
P0.7	56	40	28	D I/O	Port0 Bit7. (See the Port I/O Sub-System section for complete description).
P1.0	38	30		D I/O	Port1 Bit0. (See the Port I/O Sub-System section for complete description).
P1.1	37	29		D I/O	Port1 Bit1. (See the Port I/O Sub-System section for complete description).
P1.2	36	28		D I/O	Port1 Bit2. (See the Port I/O Sub-System section for complete description).
P1.3	35	26		D I/O	Port1 Bit3. (See the Port I/O Sub-System section for complete description).
P1.4	34	25		D I/O	Port1 Bit4. (See the Port I/O Sub-System section for complete description).
P1.5	32	24		D I/O	Port1 Bit5. (See the Port I/O Sub-System section for complete description).
P1.6	60	42		D I/O	Port1 Bit6. (See the Port I/O Sub-System section for complete description).
P1.7	59	41		D I/O	Port1 Bit7. (See the Port I/O Sub-System section for complete description).
P2.0	33			D I/O	Port2 Bit0. (See the Port I/O Sub-System section for complete description).
P2.1	27			D I/O	Port2 Bit1. (See the Port I/O Sub-System section for complete description).
P2.2	54			D I/O	Port2 Bit2. (See the Port I/O Sub-System section for complete description).
P2.3	53			D I/O	Port2 Bit3. (See the Port I/O Sub-System section for complete description).
P2.4	52			D I/O	Port2 Bit4. (See the Port I/O Sub-System section for complete description).
P2.5	51			D I/O	Port2 Bit5. (See the Port I/O Sub-System section for complete description).
P2.6	44			D I/O	Port2 Bit6. (See the Port I/O Sub-System section for complete description).
P2.7	43			D I/O	Port2 Bit7. (See the Port I/O Sub-System section for complete description).
P3.0	26			D I/O	Port3 Bit0. (See the Port I/O Sub-System section for complete description).
P3.1	25			D I/O	Port3 Bit1. (See the Port I/O Sub-System section for complete description).
P3.2	24			D I/O	Port3 Bit2. (See the Port I/O Sub-System section for complete description).
P3.3	23			D I/O	Port3 Bit3. (See the Port I/O Sub-System section for complete description).
P3.4	58			D I/O	Port3 Bit4. (See the Port I/O Sub-System section for complete description).
P3.5	57			D I/O	Port3 Bit5. (See the Port I/O Sub-System section for complete description).
P3.6	46			D I/O	Port3 Bit6. (See the Port I/O Sub-System section for complete description).
P3.7	45			D I/O	Port3 Bit7. (See the Port I/O Sub-System section for complete description).



Figure 4.5. LQFP-32 Pinout Diagram







Figure 5.4. AMX0CF: AMUX Configuration Register (C8051F00x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value	
-	-	-	-	AIN67IC	AIN45IC	AIN23IC	AIN01IC	00000000	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:	
								0xBA	
Bits7-4	Bits7-4: UNUSED. Read = 0000b; Write = don't care								
Bit3:	AIN67IC: AIN6	5. AIN7 Inpu	t Pair Config	uration Bit					
	0: AIN6 and A	N7 are inder	pendent singl	ed-ended inn	uts				
	$1 \cdot AIN6 AIN7$	are (respecti	velv) + - dif	ferential inpu	ut pair				
Bit2.	AIN45IC · AIN4	L AIN5 Inpu	t Pair Config	uration Bit	n puii				
D1(2)	0 AIN4 and Al	N5 are inder	endent singl	ed-ended inn	uts				
	1. Λ IN/4 Λ IN/5	are (respecti	$v_{alv} \perp dif$	forential input	uto it pair				
Dit1.	AIN22IC: AIN2	AIN3 Inpu	t Dair Config	uration Bit	n pan				
DITI.	AIN25IC. AIN2	N2 are inder	t Fail Coiling	ad and ad inn	uto				
	$\begin{array}{c} 0. \text{AIN2} \text{and} \text{AIN2} \\ 1. \text{AIN2} \text{AIN2} \end{array}$	and (machine)	volu) - dif	formatical input	uis				
D:40	1: AIN2, AIN3	are (respecti	very) +, - dil	ierential inpl	it pair				
B1t0:	AINUTIC: AINU), AINT Inpu	t Pair Config	uration Bit					
	0: AINO and A	INI are indep	pendent singl	ed-ended inp	uts				
	1: AIN0, AIN1	are (respecti	vely) +, - dif	ferential inpu	it pair				
NOTE.	The ADC Date V	Word is in 2'		t format for	honnala oon	figured og dif	Formatio		
NOTE:	The ADC Data	word is in 2	s complemen	it format for (channels con	ingured as dif	Terential.		



Figure 5.14. 12-Bit ADC Window Interrupt Examples, Right Justified Data

Input Voltage (AD0 - AGND)	ADC Data Word		Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0x0FFF		REF x (4095/4096)	0x0FFF	
		ADWINT not affected			ADWINT=1
	0x0201			0x0201	
REF x (512/4096)	0x0200	ADC0LTH:ADC0LTL	REF x (512/4096)	0x0200	ADC0GTH:ADC0GTL
	0x01FF			0x01FF	ADWINT
	0x0101	ADVVINT=1		0x0101	not affected
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL	REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	ADWINT not affected		0x00FF	ADWINT=1
0	0x0000		0	0x0000	J
iven: MX0SL = 0x00, A DC0LTH:ADC0L	$\Delta MX0CF = 0$ TL = 0x0200	x00, ADLJST = 0,	Given: AMX0SL = 0x00, AN ADC0LTH:ADC0LT	MX0CF = 0x0 L = 0x0100,	00, ADLJST = 0,

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0200 and > 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 or > 0x0200.

ADWINT=1

ADC0GTH:ADC0GTL ADWINT not affected ADC0LTH:ADC0LTL

Input Voltage (AD0 - AD1)	ADC Data Word	_	Input Voltage (AD0 - AD1)	ADC Data Word
REF x (2047/2048)	0x07FF		REF x (2047/2048)	0x07FF
		ADWINT not affected		
	0x0101			0x0101
REF x (256/2048)	0x0100	ADC0LTH:ADC0LTL	REF x (256/2048)	0x0100
	0x00FF	ADWINT=1		0x00FF
REF x (-1/2048)	0xFFFF	ADC0GTH:ADC0GTL	REF x (-1/2048)	0xFFFF
	0xFFFE			0xFFFE
		ADWINT not affected		
-REF	0xF800		-REF	0xF800

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0, ADC0LTH:ADC0LTL = 0x0100, ADC0GTH:ADC0GTL = 0xFFFF.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 and > 0xFFFF. (Two's Complement math, 0xFFFF = -1.)

ADWINT=1 Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0, ADC0LTH:ADC0LTH = 0xFFFF, ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF or > 0x0100. (Two's Complement math, 0xFFFF = -1.)



6. ADC (10-Bit, C8051F010/1/2/5/6/7 Only)

The ADC subsystem for the C8051F010/1/2/5/6/7 consists of a 9-channel, configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 10-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector (see block diagram in Figure 6.1). The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Register's shown in Figure 6.1. The ADC subsystem (ADC, track-and-hold and PGA) is enabled only when the ADCEN bit in the ADC Control register (ADC0CN, Figure 6.7) is set to 1. The ADC subsystem is in low power shutdown when this bit is 0. The Bias Enable bit (BIASE) in the REF0CN register (see Figure 9.2) must be set to 1 in order to supply bias to the ADC.





6.1. Analog Multiplexer and PGA

Eight of the AMUX channels are available for external measurements while the ninth channel is internally connected to an on-board temperature sensor (temperature transfer function is shown in Figure 6.3). Note that the PGA gain is applied to the temperature sensor reading. AMUX input pairs can be programmed to operate in either the differential or single-ended mode. This allows the user to select the best measurement technique for each input channel, and even accommodates mode changes "on-the-fly". The AMUX defaults to all single-ended inputs upon reset. There are two registers associated with the AMUX: the Channel Selection register AMX0SL (Figure 6.5), and the Configuration register AMX0CF (Figure 6.4). The table in Figure 6.5 shows AMUX functionality by channel for each possible configuration. The PGA amplifies the AMUX output signal by an amount determined by the AMPGN2-0 bits in the ADC Configuration register, ADC0CF (Figure 6.6). The PGA can be software-programmed for gains of 0.5, 1, 2, 4, 8 or 16. It defaults to unity gain on reset.



6.2. ADC Modes of Operation

The ADC uses VREF to determine its full-scale voltage, thus the reference must be properly configured before performing a conversion (see Section 9). The ADC has a maximum conversion speed of 100ksps. The ADC conversion clock is derived from the system clock. Conversion clock speed can be reduced by a factor of 2, 4, 8 or 16 via the ADCSC bits in the ADC0CF Register. This is useful to adjust conversion speed to accommodate different system clock speeds.

A conversion can be initiated in one of four ways, depending on the programmed states of the ADC Start of Conversion Mode bits (ADSTM1, ADSTM0) in ADC0CN. Conversions may be initiated by:

- 1. Writing a 1 to the ADBUSY bit of ADC0CN;
- 2. A Timer 3 overflow (i.e. timed continuous conversions);
- 3. A rising edge detected on the external ADC convert start signal, CNVSTR;
- 4. A Timer 2 overflow (i.e. timed continuous conversions).

Writing a 1 to ADBUSY provides software control of the ADC whereby conversions are performed "on-demand". During conversion, the ADBUSY bit is set to 1 and restored to 0 when conversion is complete. The falling edge of ADBUSY triggers an interrupt (when enabled) and sets the ADCINT interrupt flag. Note: When conversions are performed "on-demand", the ADCINT flag, not ADBUSY, should be polled to determine when the conversion has completed. Converted data is available in the ADC data word MSB and LSB registers, ADCOH, ADCOL. Converted data can be either left or right justified in the ADCOH:ADCOL register pair (see example in Figure 6.9) depending on the programmed state of the ADLJST bit in the ADCOCN register.

The ADCTM bit in register ADC0CN controls the ADC track-and-hold mode. In its default state, the ADC input is continuously tracked, except when a conversion is in progress. Setting ADCTM to 1 allows one of four different low power track-and-hold modes to be specified by states of the ADSTM1-0 bits (also in ADC0CN):

- 1. Tracking begins with a write of 1 to ADBUSY and lasts for 3 SAR clocks;
- 2. Tracking starts with an overflow of Timer 3 and lasts for 3 SAR clocks;
- 3. Tracking is active only when the CNVSTR input is low;
- 4. Tracking starts with an overflow of Timer 2 and lasts for 3 SAR clocks.

Modes 1, 2 and 4 (above) are useful when the start of conversion is triggered with a software command or when the ADC is operated continuously. Mode 3 is used when the start of conversion is triggered by external hardware. In this case, the track-and-hold is in its low power mode at times when the CNVSTR input is high. Tracking can also be disabled (shutdown) when the entire chip is in low power standby or sleep modes.







6.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Figure 6.14 and Figure 6.15 show example comparisons for reference. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 6.10. ADC0GTH: ADC Greater-Than Data High Byte Register (C8051F01x)



Figure 6.11. ADC0GTL: ADC Greater-Than Data Low Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value 1111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC4
Bits7-0: The low by Definition: ADC Great	te of the ADC er-Than Data	Greater-Th Word = AD	an Data Word C0GTH:ADC	d. COGTL				

Figure 6.12. ADC0LTH: ADC Less-Than Data High Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC7
Bits7-0: The high by	te of the ADO	C Less-Than	Data Word.					

Figure 6.13. ADC0LTL: ADC Less-Than Data Low Byte Register (C8051F01x)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value		
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000 SFR Address: 0xC6		
Bits7-0: These bits are the low byte of the ADC Less-Than Data Word.										
Definition: ADC Less-'	Definition: ADC Less-Than Data Word = ADC0LTH:ADC0LTL									
								5)		

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Figure 6.15. 10-Bit ADC Window Interrupt Examples, Left Justified Data





Figure 10.7. ACC: Accumulator



Figure 10.8. B: B Register





13. RESET SOURCES

The reset circuitry of the MCUs allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the CIP-51 halts program execution, forces the external port pins to a known state and initializes the SFRs to their defined reset values. Interrupts and timers are disabled. On exit, the program counter (PC) is reset, and program execution starts at location 0x0000.

All of the SFRs are reset to predefined values. The reset values of the SFR bits are defined in the SFR detailed descriptions. The contents of internal data memory are not changed during a reset and any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic ones), activating internal weak pull-ups which take the external I/O pins to a high state. The weak pull-ups are enabled during and after the reset. If the source of reset is from the VDD Monitor or writing a 1 to PORSF, the /RST pin is driven low until the end of the VDD reset timeout.

On exit from the reset state, the MCU uses the internal oscillator running at 2MHz as the system clock by default. Refer to Section 14 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval. (Section 13.8 details the use of the Watchdog Timer.)

There are seven sources for putting the MCU into the reset state: power-on/power-fail, external /RST pin, external CNVSTR signal, software commanded, Comparator 0, Missing Clock Detector, and Watchdog Timer. Each reset source is described below:







14. OSCILLATOR

Each MCU includes an internal oscillator and an external oscillator drive circuit, either of which can generate the system clock. The MCUs boot from the internal oscillator after any reset. The internal oscillator starts up instantly. It can be enabled/disabled and its frequency can be changed using the Internal Oscillator Control Register (OSCICN) as shown in Figure 14.2. The internal oscillator's electrical specifications are given in Table 14.1.

Both oscillators are disabled when the /RST pin is held low. The MCUs can run from the internal oscillator or external oscillator, and switch between the two at will using the CLKSL bit in the OSCICN Register. The external oscillator requires an external resonator, parallel-mode crystal, capacitor, or RC network connected to the XTAL1/XTAL2 pins (see Figure 14.1). The oscillator circuit must be configured for one of these sources in the OSCXCN register. An external CMOS clock can also provide the system clock via overdriving the XTAL1 pin. The XTAL1 and XTAL2 pins are 3.6V (not 5V) tolerant. The external oscillator can be left enabled and running even when the MCU has switched to using the internal oscillator.



Figure 14.1. Oscillator Diagram



Figure 15.11.	P2: Port2 Register
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R/W P2.7	R/W P2.6	R/W P2.5	R/W P2.4	R/W P2.3	R/W P2.2	R/W P2.1	R/W P2.0	Reset Value 11111111
Bit7	Bit6	Bit	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xA0
Bits7-0: F (1 ((1 (1	2.[7:0] Write – Outp): Logic Low : Logic High Read – Regar): P2.n is logi : P2.n is logi	ut appears or Output. a Output (hig rdless of XBF ic low. ic high.	1 I/O pins per h-impedance R0, XBR1, ar	XBR0, XBR if correspond nd XBR2 Reg	81, and XBR2 ding PRT2CI gister settings	2 registers) F.n bit = 0) 5).		

Figure 15.12. PRT2CF: Port2 Configuration Register





16.6.1. Control Register

The SMBus Control register SMB0CN is used to configure and control the SMBus interface. All of the bits in the register can be read or written by software. Two of the control bits are also affected by the SMBus hardware. The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by the hardware when a valid serial interrupt condition occurs. It can only be cleared by software. The Stop flag (STO, SMB0CN.4) is cleared to logic 0 by hardware when a STOP condition is present on the bus.

Setting the ENSMB flag to logic 1 enables the SMBus interface. Clearing the ENSMB flag to logic 0 disables the SMBus interface and removes it from the bus. Momentarily clearing the ENSMB flag and then resetting it to logic 1 will reset a SMBus communication. However, ENSMB should not be used to temporarily remove a device from the bus since the bus state information will be lost. Instead, the Assert Acknowledge (AA) flag should be used to temporarily remove the device from the bus (see description of AA flag below).

Setting the Start flag (STA, SMB0CN.5) to logic 1 will put the SMBus in a master mode. If the bus is free, the SMBus hardware will generate a START condition. If the bus is not free, the SMBus hardware waits for a STOP condition to free the bus and then generates a START condition after a 5 μ s delay per the SMB0CR value. (In accordance with the SMBus protocol, the SMBus interface also considers the bus free if the bus is idle for 50 μ s and no STOP condition was recognized.) If STA is set to logic 1 while the SMBus is in master mode and one or more bytes have been transferred, a repeated START condition will be generated. To ensure proper operation, the STO flag should be explicitly cleared before setting STA to a logic 1.

When the Stop flag (STO, SMB0CN.4) is set to logic 1 while the SMBus interface is in master mode, the hardware generates a STOP condition on the SMBus. In a slave mode, the STO flag may be used to recover from an error condition. In this case, a STOP condition is not generated on the SMBus, but the SMBus hardware behaves as if a STOP condition has been received and enters the "not addressed" slave receiver mode. The SMBus hardware automatically clears the STO flag to logic 0 when a STOP condition is detected on the bus.

The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by hardware when the SMBus interface enters one of 27 possible states. If interrupts are enabled for the SMBus interface, an interrupt request is generated when the SI flag is set. The SI flag must be cleared by software. While SI is set to logic 1, the clock-low period of the serial clock will be stretched and the serial transfer is suspended.

The Assert Acknowledge flag (AA, SMB0CN.2) is used to set the level of the SDA line during the acknowledge clock cycle on the SCL line. Setting the AA flag to logic 1 will cause an ACKNOWLEDGE (low level on SDA) to be sent during the acknowledge cycle if the device has been addressed. Setting the AA flag to logic 0 will cause a NOT ACKNOWLEDGE (high level on SDA) to be sent during acknowledge cycle. After the transmission of a byte in slave mode, the slave can be temporarily removed from the bus by clearing the AA flag. The slave's own address and general call address will be ignored. To resume operation on the bus, the AA flag must be reset to logic 1 to allow the slave's address to be recognized.

Setting the SMBus Free Timer Enable bit (FTE, SMB0CN.1) to logic 1 enables the SMBus Free Timeout feature. If SCL and SDA remain high for the SMBus Free Timeout given in the SMBus Clock Rate Register (Figure 16.5), the bus will be considered free and a Start will be generated if pending. The bus free period should be greater than 50μ s.

Setting the SMBus timeout enable bit (TOE, SMB0CN.0) to logic 1 enables Timer 3 to count up when the SCL line is low and Timer 3 is enabled. If Timer 3 overflows, a Timer 3 interrupt will be generated, which will alert the CPU that a SMBus SCL low timeout has occurred.



Figure 16.4	. SMB0CN:	SMBus	Control	Register
-------------	-----------	--------------	---------	----------

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
BUSY	ENSMB	STA	STO	SI	AA	FTE	TOE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xC0
Bit7:	BUSY: Busy S	Status Flag.						
	0: SMBus is fr	ee						
	1: SMBus is b	usv						
Bit6:	ENSMB: SME	Bus Enable.						
	This bit enable	es/disables th	e SMBus ser	rial interface.				
	0: SMBus disa	bled.						
	1: SMBus enal	bled.						
Bit5:	STA: SMBus	Start Flag.						
	0: No START	condition is	transmitted.					
	1: When opera	ting as a ma	ster, a STAR	T condition i	s transmitted	if the bus is	free. (If the	
	bus is not free.	, the START	is transmitte	d after a STO	OP is received	1.) If STA is	set after one	
	or more bytes	have been tra	ansmitted or	received and	before a STC	OP is receive	d, a repeated	
	START condit	tion is transn	nitted. STO	should be exi	olicitly cleare	d before sett	ing STA to	
	logic 1.			,	5		0	
Bit4:	STO: SMBus	Stop Flag.						
	0: No STOP c	ondition is tr	ansmitted.					
	1: Setting STC) to logic 1 c	auses a STO	P condition to	be transmitt	ted. When a	STOP	
	condition is re	ceived, hard	ware clears S	TO to logic). If both ST	A and STO a	re set. a	
	STOP condition	on is transmit	ted followed	bv a STAR	condition.	In slave mod	e. setting the	
	STO flag caus	es SMBus to	behave as if	a STOP con	dition was re	ceived.	.,	
Bit3:	SI: SMBus Se	rial Interrupt	Flag.					
	This bit is set l	by hardware	when one of	27 possible 3	SMBus states	is entered.	Status code	
	0xF8 does not	cause SI to l	be set.) Whe	n the SI inter	rupt is enable	ed, setting thi	s bit causes	
	the CPU to ve	ctor to the SI	ABus interru	pt service rou	tine. This bi	it is not autor	natically	
	cleared by har	dware and m	ust be cleare	d by software	2.		5	
Bit2:	AA: SMBus A	ssert Ackno	wledge Flag.	5				
	This bit define	s the type of	acknowledg	e returned du	ring the ackn	owledge cyc	le on the	
	SCL line.	J			8			
	0: A "not ackn	owledge" (h	igh level on	SDA) is retu	ned during th	ne acknowled	lge cycle.	
	1: An "acknow	vledge" (low	level on SD.	A) is returned	l during the a	cknowledge	cvcle.	
Bit1:	FTE: SMBus I	Free Timer E	nable Bit	,	U	e	5	
	0: No timeout	when SCL i	s high					
	1: Timeout wl	hen SCL hig	h time excee	ds limit speci	fied by the S	MB0CR valu	ie.	
Bit0:	TOE: SMBus	Timeout Ena	ble Bit	1	5			
	0: No timeout	when SCL i	s low.					
	1: Timeout wl	hen SCL low	time exceed	ls limit specif	ied by Timer	3, if enabled	l.	
					2			



in an "off-line" state. In a multiple-master environment, the system controller should check the state of the SLVSEL flag (SPI0CN.2) to ensure the bus is free before setting the MSTEN bit and initiating a data transfer.

17.3. Serial Clock Timing

As shown in Figure 17.4, four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.7) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.6) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. Note: the SPI should be disabled (by clearing the SPIEN bit, SPI0CN.0) while changing the clock phase and polarity.

The SPI Clock Rate Register (SPIOCKR) as shown in Figure 17.7 controls the master mode serial clock frequency. This register is ignored when operating in slave mode.



Figure 17.4. Data/Clock Timing Diagram



20.1.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.





20.1.3. High Speed Output Mode

In this mode, each time a match occurs between the PCA Timer Counter and a module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn) the logic level on the module's associated CEXn pin will toggle. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode.

Figure 20.5. PCA High Speed Output Mode Diagram





20.1.4. Pulse Width Modulator Mode

All of the modules can be used independently to generate pulse width modulated (PWM) outputs on their respective CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 20.6). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the PCA0CPHn without software intervention. It is good practice to write to PCA0CPHn instead of PCA0CPLn to avoid glitches in the digital comparator. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables Pulse Width Modulator mode.







21. JTAG (IEEE 1149.1)

Each MCU has an on-chip JTAG interface and logic to support boundary scan for production and in-system testing, Flash read and write operations, and non-intrusive in-circuit debug. The JTAG interface is fully compliant with the IEEE 1149.1 specification. Refer to this specification for detailed descriptions of the Test Interface and Boundary-Scan Architecture. Access of the JTAG Instruction Register (IR) and Data Registers (DR) are as described in the Test Access Port and Operation of the IEEE 1149.1 specification.

The JTAG interface is via four dedicated pins on the MCU, which are TCK, TMS, TDI, and TDO. These pins are all 5V tolerant.

Through the 16-bit JTAG Instruction Register (IR), any of the eight instructions shown in Figure 21.1 can be commanded. There are three Data Registers (DR's) associated with JTAG Boundary-Scan, and four associated with Flash read/write operations on the MCU.

Bit0 Bit0 IR value Instruction Description 0x0000 EXTEST Selects the Boundary Data Register for control and observability of a device pins 0x0002 SAMPLE/ Selects the Boundary Data Register for observability and presetting th PRELOAD 0x0004 IDCODE Selects device ID Register 0x0082 Flash Control Selects FLASHCON Register to control how the interface logic responses and writes to the FLASHDAT Register 0x0083 Flash Data Selects FLASHADR Register for reads and writes to the Flash memo 0x0084 Flash Address Selects FLASHADR Register which holds the address of all Flash reactions 0x0085 Flash Scale Selects FLASHSCL Register which controls the prescaler used to ger timing signals for Flash operations	Reset Val																			
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Figure 21.1.	IR: JTAG	Instruction	Register
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