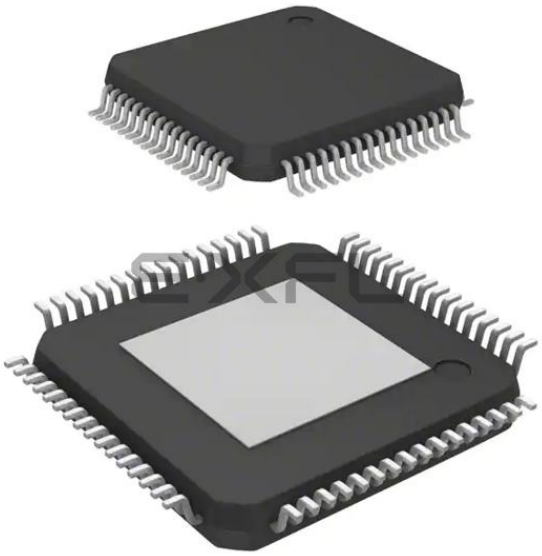
Infineon Technologies - XMC4400F100F256ABXQSA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f100f256abxqsa1

XMC4400 Data Sheet

Revision History: V1.2 2015-12

Previous Versions:
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

Page	Subjects
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
37	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
38	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
38	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
45	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
59	Added footnote on test configuration for LPAC measurement.
61	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
66	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
70	Added footnote on current consumption by enabling of f_{CCU}.
71	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-LQFP-100-25 package information.
97, 100	Added tables describing the differences between PG-LQFP-100-11 to PG-LQFP-100-25 as well as PG-LQFP-64-19 to PG-TQFP-64-19 packages.
102	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

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2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	100	64	A2	
P0.3	99	63	A2	
P0.4	98	62	A2	
P0.5	97	61	A2	
P0.6	96	60	A2	
P0.7	89	58	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	88	57	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	4	A2	
P0.10	3	3	A1+	

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Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P3.0	7	-	A2	
P3.1	6	-	A2	
P3.2	5	-	A2	
P3.3	93	-	A1+	
P3.4	92	-	A1+	
P3.5	91	-	A2	
P3.6	90	-	A2	
P4.0	85	-	A2	
P4.1	84	-	A2	
P5.0	58	-	A1+	
P5.1	57	-	A1+	
P5.2	56	-	A1+	
P5.7	55	-	A1+	
P14.0	31	20	AN/DIG_IN	
P14.1	30	-	AN/DIG_IN	
P14.2	29	-	AN/DIG_IN	
P14.3	28	19	AN/DIG_IN	
P14.4	27	18	AN/DIG_IN	
P14.5	26	17	AN/DIG_IN	
P14.6	25	16	AN/DIG_IN	
P14.7	24	15	AN/DIG_IN	
P14.8	37	24	AN/DAC/DIG_IN	
P14.9	36	23	AN/DAC/DIG_IN	
P14.12	23	-	AN/DIG_IN	
P14.13	22	-	AN/DIG_IN	
P14.14	21	14	AN/DIG_IN	
P14.15	20	-	AN/DIG_IN	
P15.2	19	-	AN/DIG_IN	
P15.3	18	-	AN/DIG_IN	
P15.8	39	-	AN/DIG_IN	
P15.9	38	-	AN/DIG_IN	

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Table 12 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P14.9					DAC. OUT_1			VADC. G1CH1		VADC. G3CH3	ETH0. RXD1C			
P14.12								VADC. G1CH4						
P14.13								VADC. G1CH5						
P14.14								VADC. G1CH6					G1ORC6	
P14.15								VADC. G1CH7					G1ORC7	
P15.2									VADC. G2CH2					
P15.3									VADC. G2CH3					
P15.8										VADC. G3CH0	ETH0. CLK_RMIIC			ETH0. CLKRXC
P15.9										VADC. G3CH1	ETH0. CRS_DVC			ETH0. RXDVC
USB_DP														
USB_DM														
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT					WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT					WAKEUPB							
TCK						DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO									
$\overline{\text{PORST}}$														
XTAL1							U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F				
XTAL2														
RTC_XTAL1									ERU0. 1B1					
RTC_XTAL2														

The XMC4400 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

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Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

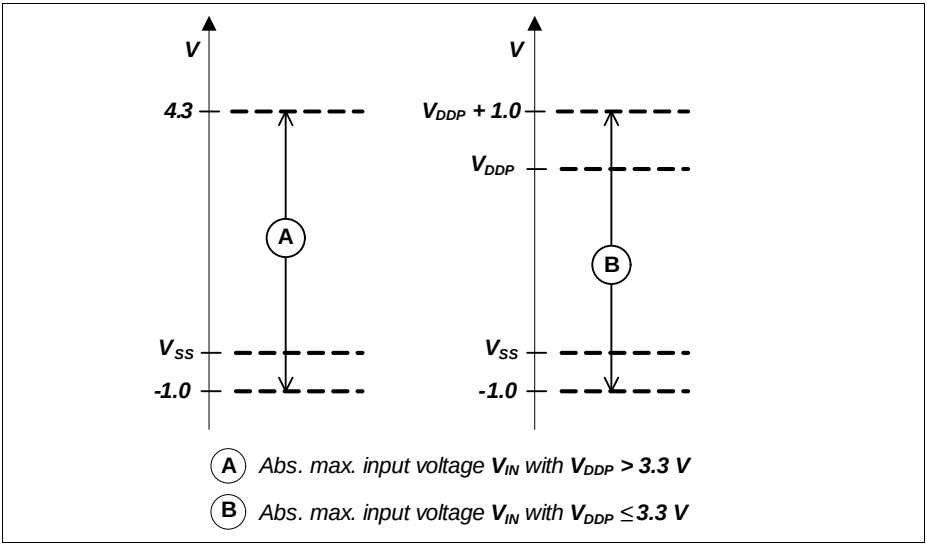

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

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Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 14 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG} SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 17**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

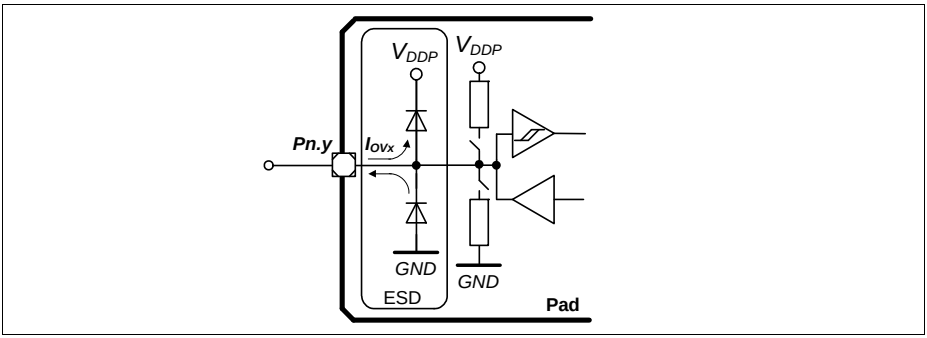

Figure 9 Input Overload Current via ESD structures

Table 15 and **Table 16** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ CC	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ SR	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 22 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

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Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\ V \le V_{IN} \le V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \ge 3.13$ V
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \ge$ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \le 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (ADCx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \le V_{AREF} \le V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \le V_{AGND} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution[7]; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$, dedicated pins for V_{DDA} and V_{AREF}
Differential Non-Linearity Error[8]	EA_{DNL} CC	-3	–	3	LSB	
Gain Error[8]	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-3	–	3	LSB	
Offset Error[8]	EA_{OFF} CC	-4	–	4	LSB	
Total Unadjusted Error	TUE CC	-6	–	6	LSB	12-bit resolution[7]; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$, shared pin for V_{DDA} and V_{AREF} (PG-LQFP-64)
Differential Non-Linearity Error[8]	EA_{DNL} CC	-4.5	–	4.5	LSB	
Gain Error[8]	EA_{GAIN} CC	-6	–	6	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-4.5	–	4.5	LSB	
Offset Error[8]	EA_{OFF} CC	-6	–	6	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion[5]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA}[9]
ON resistance of the analog input path	R_{AIN} CC	–	700	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 14**).

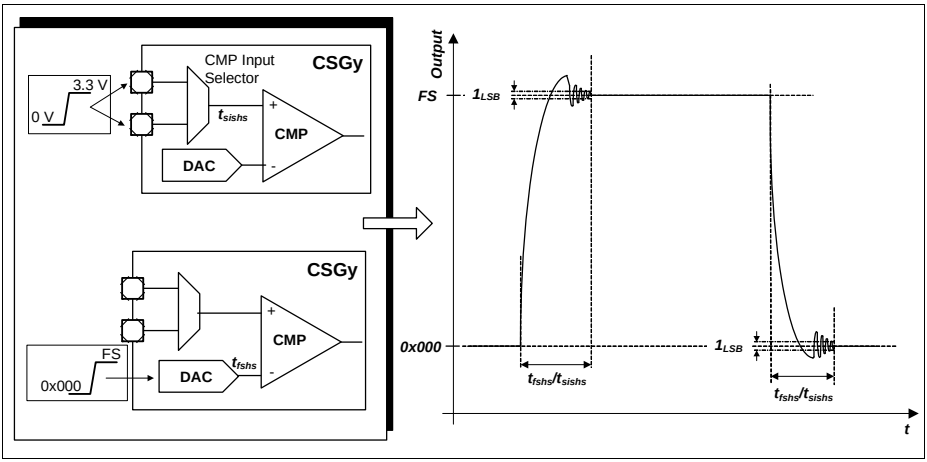

Figure 20 DAC and Input Selector Propagation Delay

3.2.5.3 Clocks

HRPWM DAC Conversion Clock

The DAC conversion clock can be generated internally or it can be controlled via a HRPWM module pin.

Table 31 External DAC conversion trigger operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{etrg}	SR	–	–	30[2)]	MHz	
ON time	t_{onetrg}	SR	$2T_{ccu}$[1)2)]	–	–	ns	
OFF time	$t_{offetrg}$	SR	$2T_{ccu}$[1)2)]	–	–	ns	

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on **Table 32**.

Table 37 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2)3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX}SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{DDP}

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

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Table 41 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time[5)]

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH × (1 / f_{CPU}) ≥ t_a.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C.

5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

3.3.11 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.11.1 ETH Measurement Reference Points

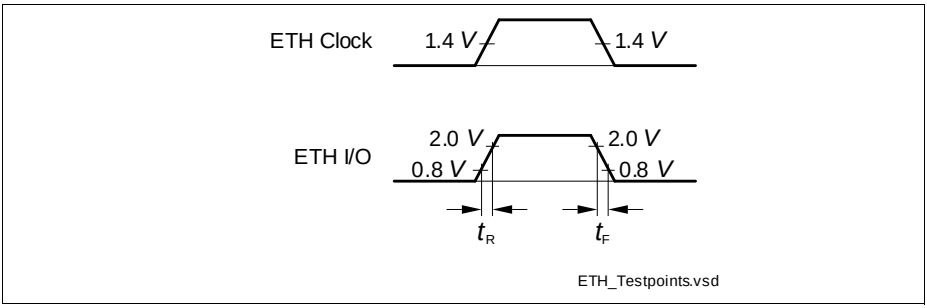

Figure 39 ETH Measurement Reference Points

3.3.11.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 58 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

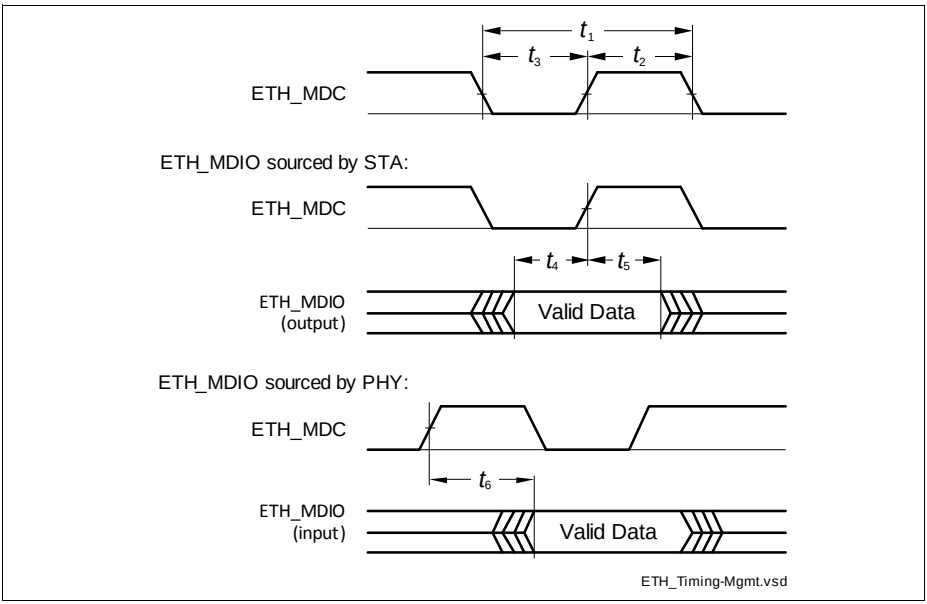

Figure 40 ETH Management Signal Timing

3.3.11.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 59 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

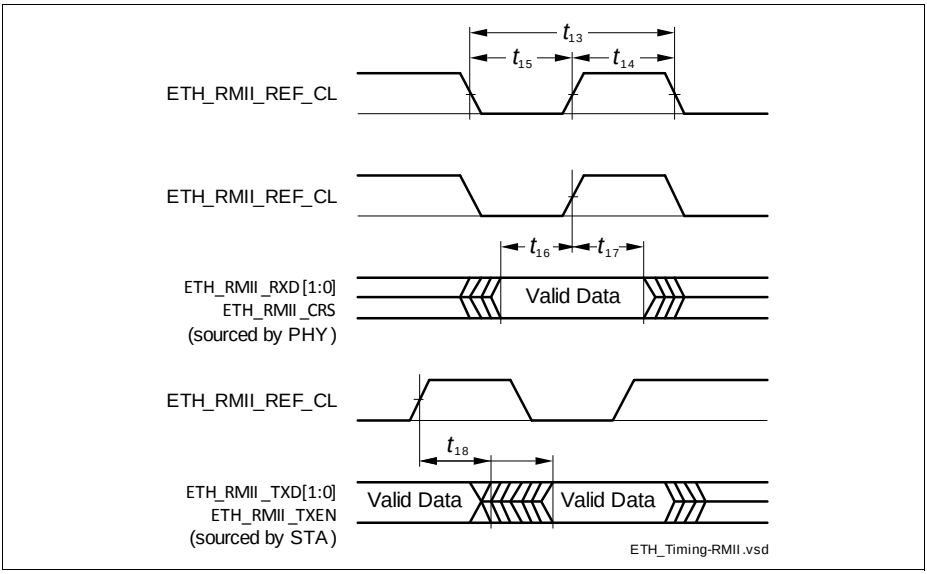

Figure 41 ETH RMII Signal Timing

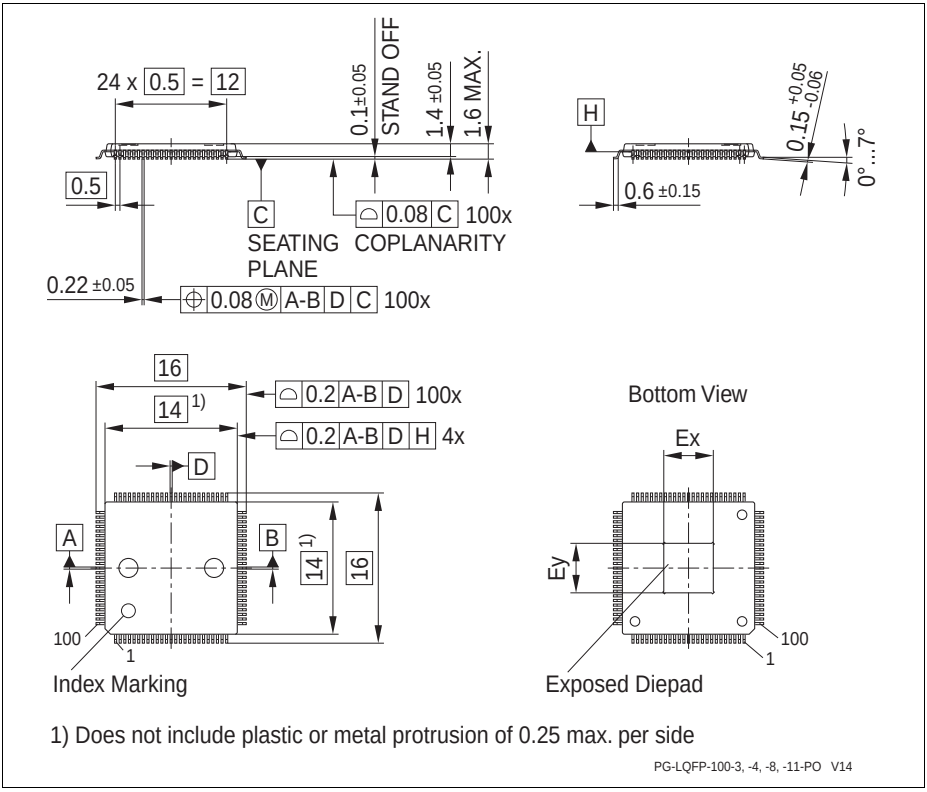

Figure 42 PG-LQFP-100-11 (Plastic Green Low Profile Quad Flat Package)

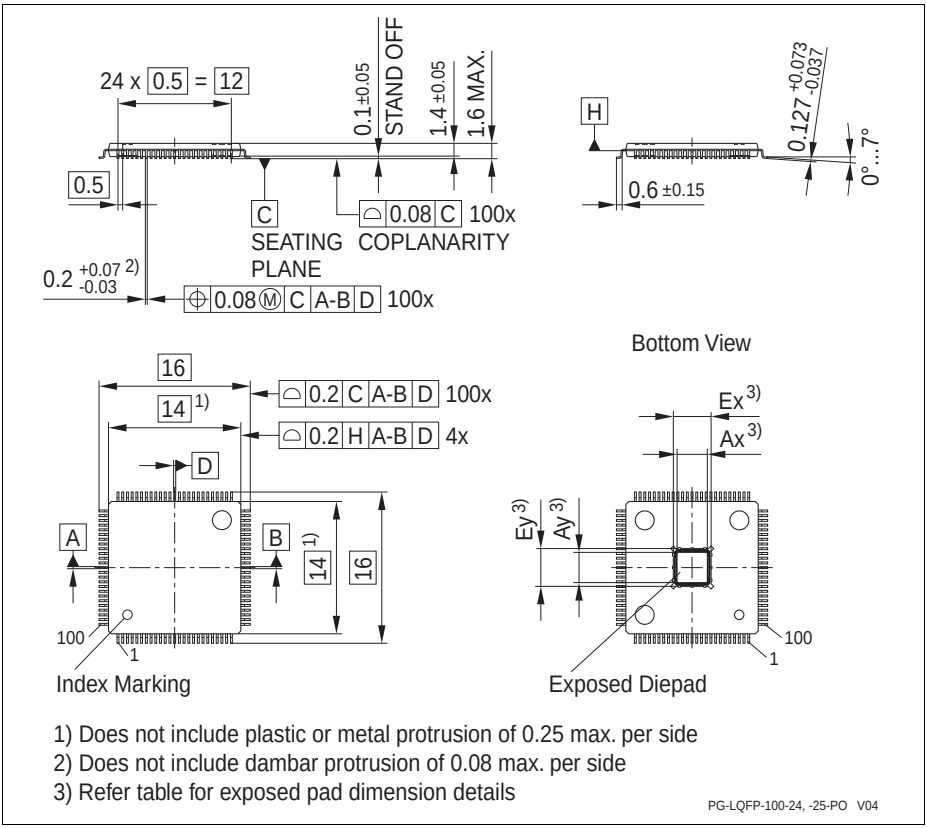

Figure 43 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)