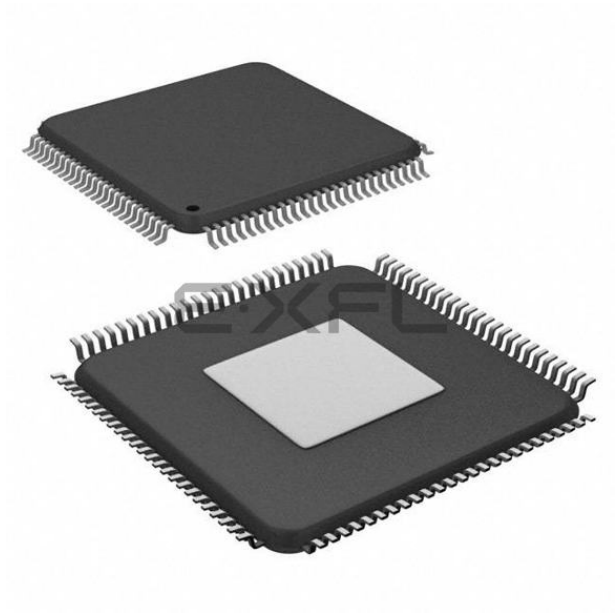
Infineon Technologies - XMC4400F100K512BAXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f100k512baxqma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4400 series devices.

The document describes the characteristics of a superset of the XMC4400 series devices. For simplicity, the various device types are referred to by the collective term XMC4400 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4400 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4400** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4400 Device Types

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4400-F100x512	PG-LQFP-100	512	80
XMC4400-F64x512	PG-yQFP-64[2)]	512	80
XMC4400-F100x256	PG-LQFP-100	256	80
XMC4400-F64x256	PG-yQFP-64[2)]	256	80
XMC4402-F100x256	PG-LQFP-100	256	80
XMC4402-F64x256	PG-yQFP-64[2)]	256	80

1) x is a placeholder for the supported temperature range.

2) y is a placeholder for the QFP package variant, LQFP or TQFP depending on the stepping, see **Section 1.3**.

Table 4 Features of XMC4400 Device Types

Derivative[1)]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4400-F100x512	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x512	14	4	2	4 x 4	2 x 4	2	1
XMC4400-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x256	14	4	2	4 x 4	2 x 4	2	1
XMC4402-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4402-F64x256	14	4	2	4 x 4	2 x 4	2	1

1) x is a placeholder for the supported temperature range.

1.5 Definition of Feature Variants

The XMC4400 types are offered with several memory sizes and number of available VADC channels. **Table 5** describes the location of the available Flash memory, **Table 6** describes the location of the available SRAMs, **Table 7** the available VADC channels.

Table 5 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	$0800\ 0000_H$ – $0803\ FFFF_H$	$0C00\ 0000_H$ – $0C03\ FFFF_H$
512 Kbytes	$0800\ 0000_H$ – $0807\ FFFF_H$	$0C00\ 0000_H$ – $0C07\ FFFF_H$

Table 6 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
80 Kbytes	$1FFF\ C000_H$ – $1FFF\ FFFF_H$	$2000\ 0000_H$ – $2000\ 7FFF_H$	$2000\ 8000_H$ – $2000\ FFFF_H$

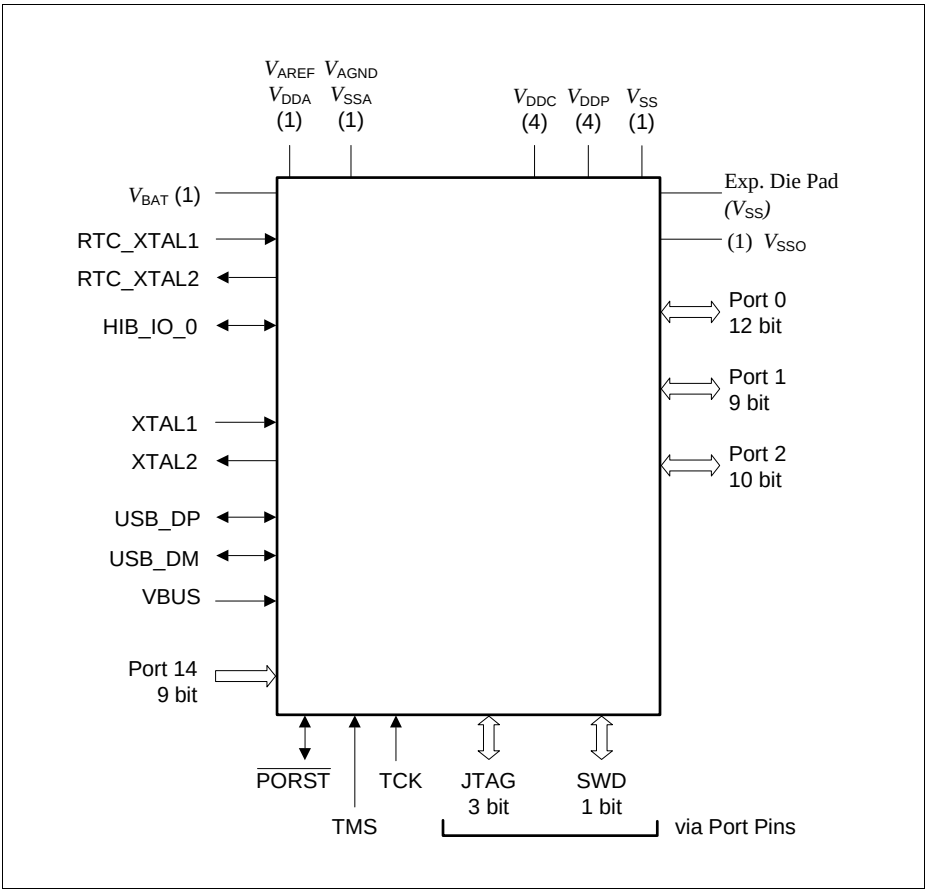

Figure 3 XMC4400 Logic Symbol PG-LQFP-64 and PG-TQFP-64

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P0.11	95	59	A1+	
P0.12	94	-	A1+	
P1.0	79	52	A1+	
P1.1	78	51	A1+	
P1.2	77	50	A2	
P1.3	76	49	A2	
P1.4	75	48	A1+	
P1.5	74	47	A1+	
P1.6	83	-	A2	
P1.7	82	-	A2	
P1.8	81	54	A2	
P1.9	80	53	A2	
P1.10	73	-	A1+	
P1.11	72	-	A1+	
P1.12	71	-	A2	
P1.13	70	-	A2	
P1.14	69	-	A2	
P1.15	68	46	A2	
P2.0	52	34	A2	
P2.1	51	33	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	50	32	A2	
P2.3	49	31	A2	
P2.4	48	30	A2	
P2.5	47	29	A2	
P2.6	54	36	A1+	
P2.7	53	35	A1+	
P2.8	46	28	A2	
P2.9	45	27	A2	
P2.10	44	-	A2	
P2.14	41	-	A2	
P2.15	40	-	A2	

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
USB_DP	9	6	special	
USB_DM	8	5	special	
HIB_IO_0	14	10	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	13	-	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	67	45	A1	Weak pull-down active.
TMS	66	44	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	65	43	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	61	39	clock_IN	
XTAL2	62	40	clock_O	
RTC_XTAL1	15	11	clock_IN	
RTC_XTAL2	16	12	clock_O	
VBAT	17	13	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	10	7	special	
VAREF	33	-	AN_Ref	
VAGND	32	-	AN_Ref	
VDDA	35	-	AN_Power	

2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

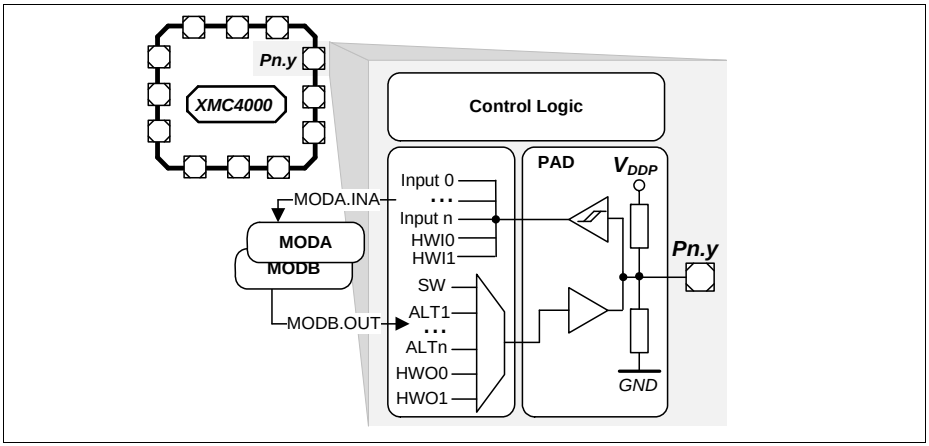

Figure 6 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2			U1C1. DX0D	ETH0. CLK_RMIIB	ERU0. 0B0			HRPWM0. C1INB		ETH0. CLKRXB
P0.1	USB. DRIVEVBUS	U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3				ETH0. CRS_DVB	ERU0. 0A0			HRPWM0. C2INB		ETH0. RXDVB
P0.2		U1C1. SELO1	CCU80. OUT01	HRPWM0. HROUT01	U1C0. DOUT3	U1C0. HWIN3	ETH0. RXD0B		ERU0. 3B3					
P0.3			CCU80. OUT20	HRPWM0. HROUT20	U1C0. DOUT2	U1C0. HWIN2	ETH0. RXD1B			ERU1. 3B0				
P0.4	ETH0. TX_EN		CCU80. OUT10	HRPWM0. HROUT21	U1C0. DOUT1	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3					
P0.5	ETH0. TXD0	U1C0. DOUT0	CCU80. OUT00	HRPWM0. HROUT00	U1C0. DOUT0	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0				
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30	HRPWM0. HROUT30				U1C0. DX2A	ERU0. 3B2		CCU80. IN2B			
P0.7	WWDT. SERVICE_OUT	U0C0. SELO0		HRPWM0. HROUT11		DB. TDI	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT		HRPWM0. HROUT10		$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1		CCU80. IN1B			
P0.9	HRPWM0. HROUT31	U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0	ETH0. MDO	ETH0. MDIA	U1C1. DX2A	USB. ID	ERU0. 1B0					
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1			U1C1. DX1A		ERU0. 1A0					
P0.11		U1C0. SCLKOUT	CCU80. OUT31				ETH0. RXERB	U1C0. DX1A	ERU0. 3A2					
P0.12		U1C1. SELO0	CCU40. OUT3					U1C1. DX2B	ERU0. 2B2					
P1.0	DSD. CGPWMN	U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3			U0C0. DX2A		ERU0. 3B0		CCU40. IN3A	HRPWM0. C0INA		
P1.1	DSD. CGPWMP	U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2			U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0		CCU40. IN2A	HRPWM0. C1INA		
P1.2			CCU40. OUT1	ERU1. PDOUT1	U0C0. DOUT3	U0C0. HWIN3		POSIF0. IN1A		ERU1. 2B0	CCU40. IN1A	HRPWM0. C2INA		
P1.3		U0C0. MCLKOUT	CCU40. OUT0	ERU1. PDOUT0	U0C0. DOUT2	U0C0. HWIN2		POSIF0. IN0A		ERU1. 2A0	CCU40. IN0A	HRPWM0. C0INB		
P1.4	WWDT. SERVICE_OUT	CAN. N0_TXD	CCU80. OUT33	CCU81. OUT20	U0C0. DOUT1	U0C0. HWIN1	U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0		CCU41. IN0C	HRPWM0. BL0A		
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0	U0C0. HWIN0	U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		
P1.6		U0C0. SCLKOUT					DSD. DIN2A							

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

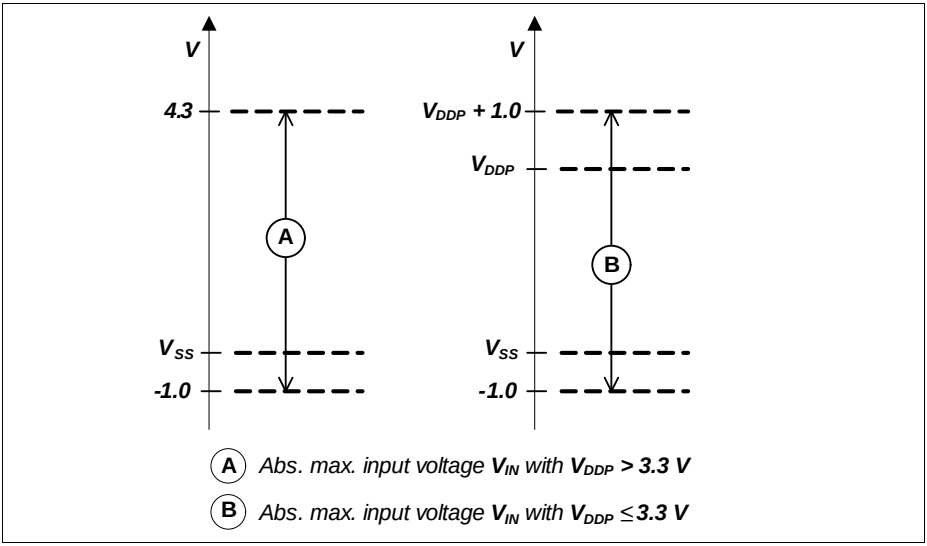

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 15 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V
A2	$V_{IN} = V_{DDP}$ + 0.7 V	$V_{IN} = V_{DDP}$ + 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V

Table 16 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS}$ - 1.0 V	$V_{IN} = V_{SS}$ - 0.75 V
A2	$V_{IN} = V_{SS}$ - 0.7 V	$V_{IN} = V_{SS}$ - 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ - 1.0 V	$V_{IN} = V_{DDP}$ - 0.75 V

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[12:0], P3.[6:0]
2	P14.[15:0], P15.[9:2]
3	P2.[15:0], P5.[7:0]
4	P1.[15:0], P4.[1:0]

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 18 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

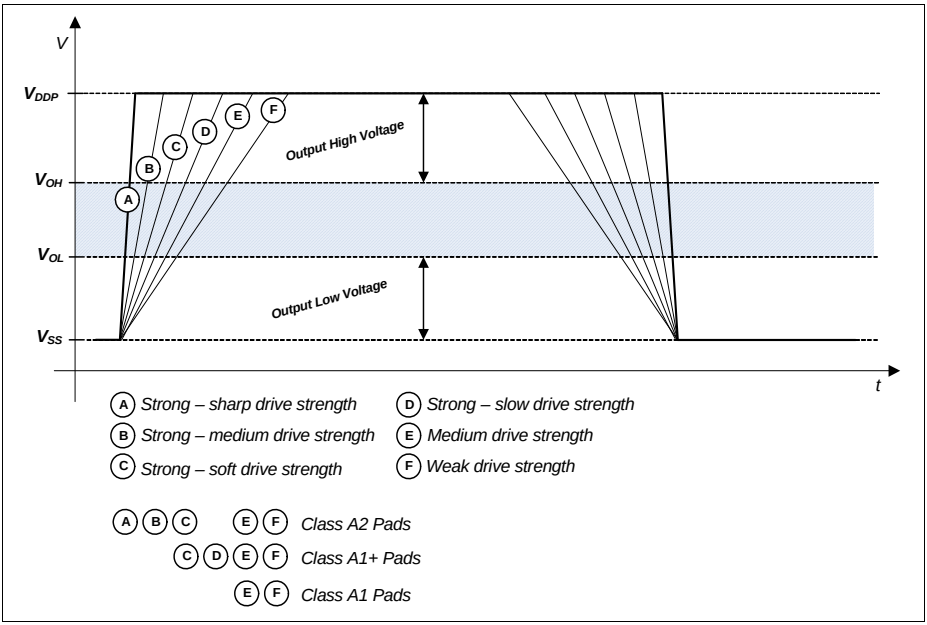

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\ V \le V_{IN} \le V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \ge 3.13$ V
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \ge$ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \le 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock, f_{hrpwm}.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.2.5.1 HRC characteristics

Table 29 summarizes the characteristics of the HRC units.

Table 29 HRC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High resolution step size[1)2)]	t_{HRS} CC	–	150	–	ps	
Startup time (after reset release)	t_{start} CC	–	–	2	µs	

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	*RES* CC		10		bits	
DAC differential nonlinearity	*DNL CC*	-1	–	1.5	LSB	Monotonic behavior, See **Figure 18**
DAC integral nonlinearity	*INL* CC	-3	–	3	LSB	See **Figure 18**

Peripheral Idle Currents

Test conditions:

- f_{sys} and derived clocks at 120 MHz
- V_{DDP} = 3.3 V, T_a =25 °C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity
- the given values are a result of differential measurements with asserted and deasserted peripheral reset and enabled clock of the peripheral under test

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

Table 40 Peripheral Idle Currents

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORTS ETH USB FCE WDT POSIFx	I_{PER} CC	–	≤ 0.3	–	mA	
MultiCAN ERU LEDTSCU0 CCU4x CCU8x		–	≤ 1.0	–		
DAC (digital)[1)]		–	1.3	–		
USICx		–	3.0	–		
DSD VADC (digital)[1)]		–	4.5	–		
DMAx		–	6.0	–		

1) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.

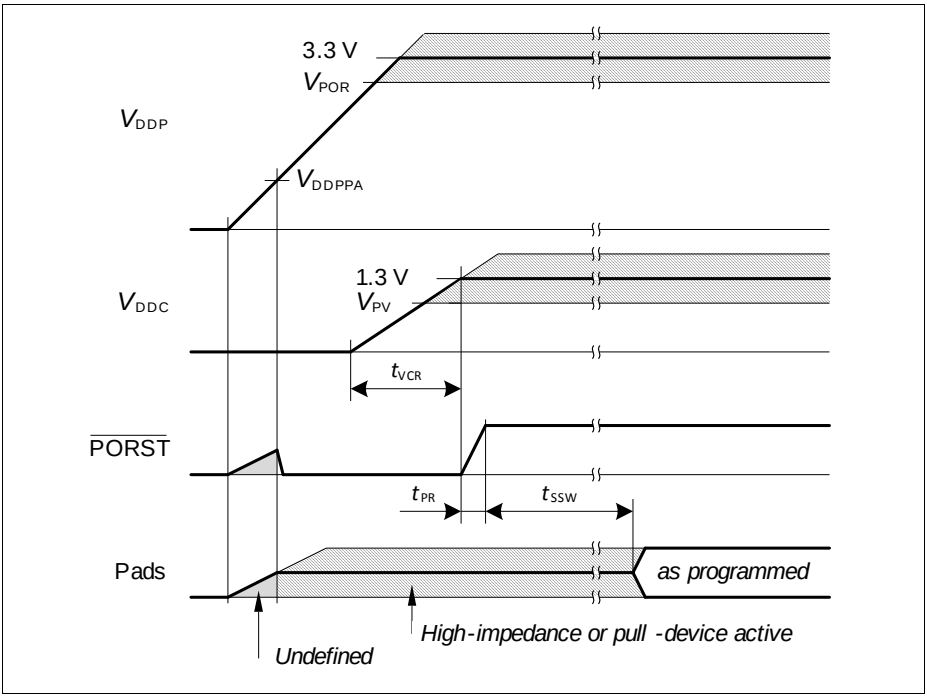

Figure 27 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The Data timing are to the active clock edge, in half-rate clocking mode that is the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 49 ETM Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TRACECLK period	t_1 CC	16.7	–	–	ns	–
TRACECLK high time	t_2 CC	2	–	–	ns	–
TRACECLK low time	t_3 CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4 CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5 CC	–	–	3	ns	–
TRACEDATA output valid time	t_6 CC	-2	–	3	ns	–

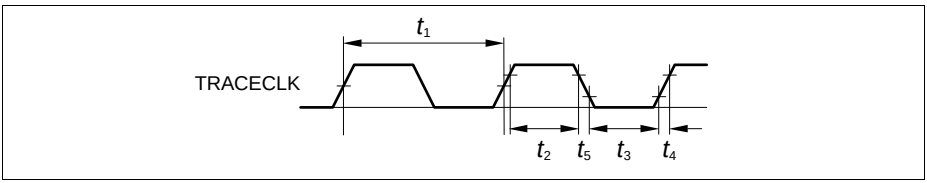

Figure 31 ETM Clock Timing

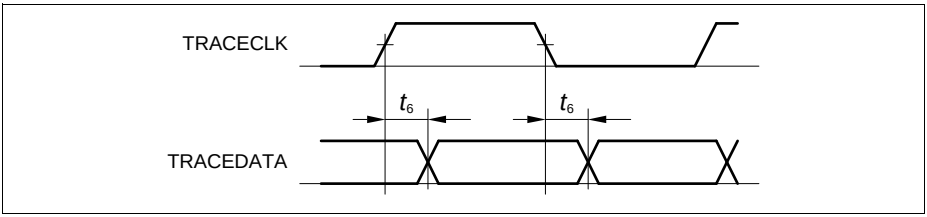

Figure 32 ETM Data Timing

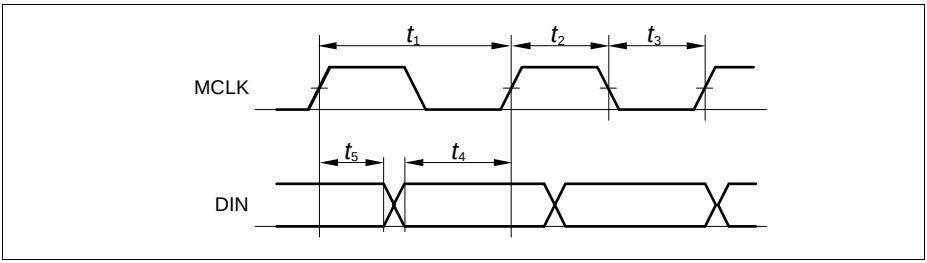

Figure 33 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 51 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

4 Package and Reliability

The XMC4400 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 60 provides the thermal characteristics of the packages used in XMC4400.

Table 60 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions (including U-Groove where applicable)	Ex × Ey CC	-	7.0 × 7.0	mm	PG-LQFP-100-11
		-	7.0 × 7.0	mm	PG-LQFP-100-25
		-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
Exposed Die Pad dimensions excluding U-Groove	Ax × Ay CC	-	6.2 × 6.2	mm	PG-LQFP-100-25
Thermal resistance Junction-Ambient $T_J \leq 150$ °C	$R_{\Theta JA}$ CC	-	20.5	K/W	PG-LQFP-100-11[1)]
		-	20.0	K/W	PG-LQFP-100-25[1)]
		-	30.0	K/W	PG-LQFP-64-19[1)]
		-	22.5	K/W	PG-TQFP-64-19[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

Table 62 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30.0 K/W	22.5 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.07}_{-0.04}$ mm
Exposed Die Pad outer dimensions	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	4.9 mm × 4.9 mm

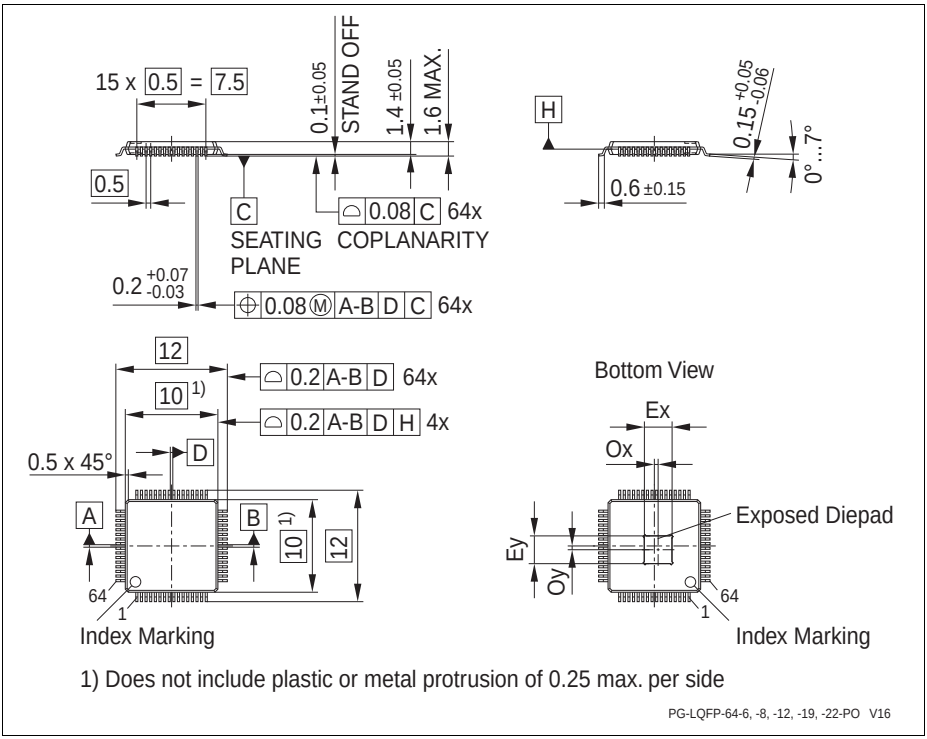

Figure 44 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)

5 Quality Declarations

The qualification of the XMC4400 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 63 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D