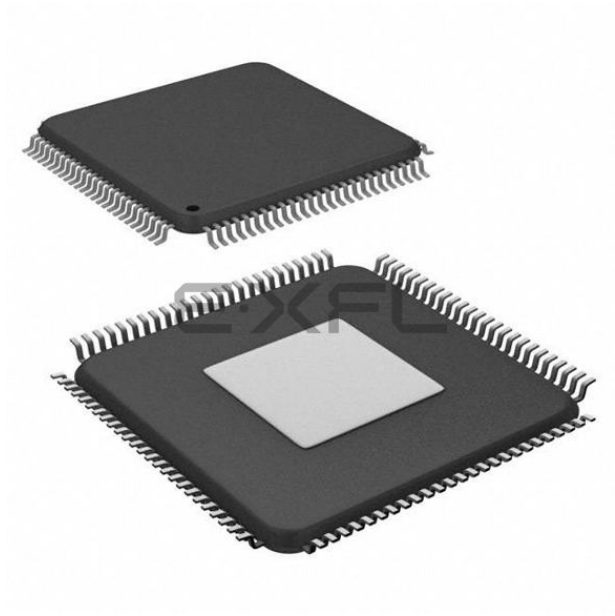
Infineon Technologies - XMC4400F100K512BAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-11
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f100k512baxuma1

1.3 Package Variants

Different markings of the XMC4400 use different package variants. Details of those packages are given in the **Package Parameters** section of the Data Sheet.

Table 2 XMC4400 Package Variants

Package Variant	Marking	Package
XMC4400-F100	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-100-11
XMC4400-F64		PG-LQFP-64-19
XMC4400-F100	BA	PG-LQFP-100-25
XMC4400-F64		PG-TQFP-64-19

1.4 Device Type Features

The following table lists the available features per device type.

Table 3 Features of XMC4400 Device Types

Derivative[1)]	LEDTS Intf.	ETH Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4400-F100x512	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F64x512	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F100x256	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4400-F64x256	1	RMII	1	2 x 2	N0, N1 MO[0..63]
XMC4402-F100x256	1	–	1	2 x 2	N0, N1 MO[0..63]
XMC4402-F64x256	1	–	1	2 x 2	N0, N1 MO[0..63]

1) x is a placeholder for the supported temperature range.

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

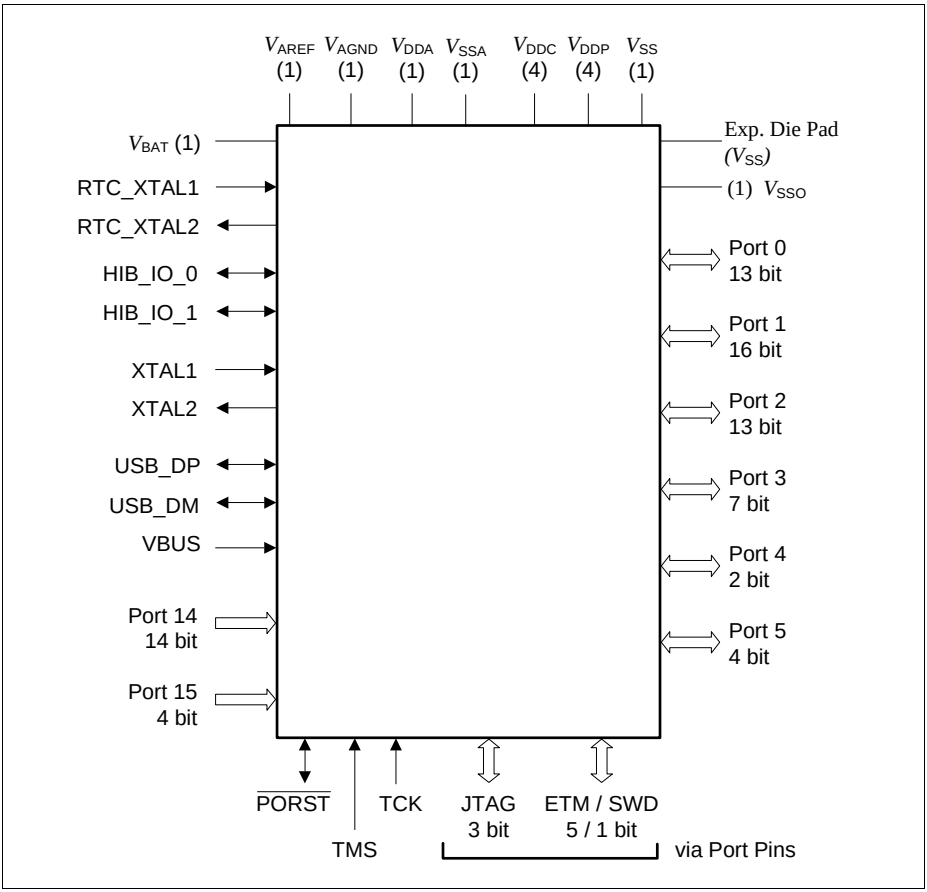

Figure 2 XMC4400 Logic Symbol PG-LQFP-100

2.3 Power Connection Scheme

Figure 7. shows a reference power connection scheme for the XMC4400.

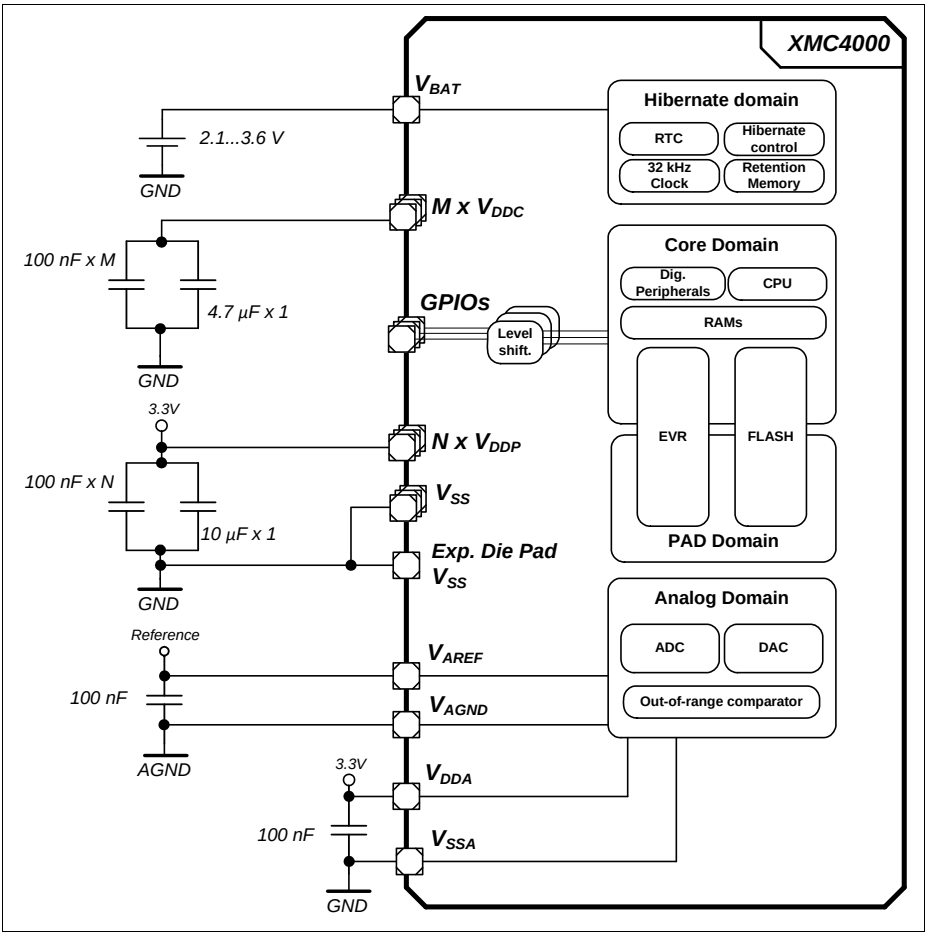

Figure 7 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 4.7uF capacitor to the V_{DDC} nets.

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

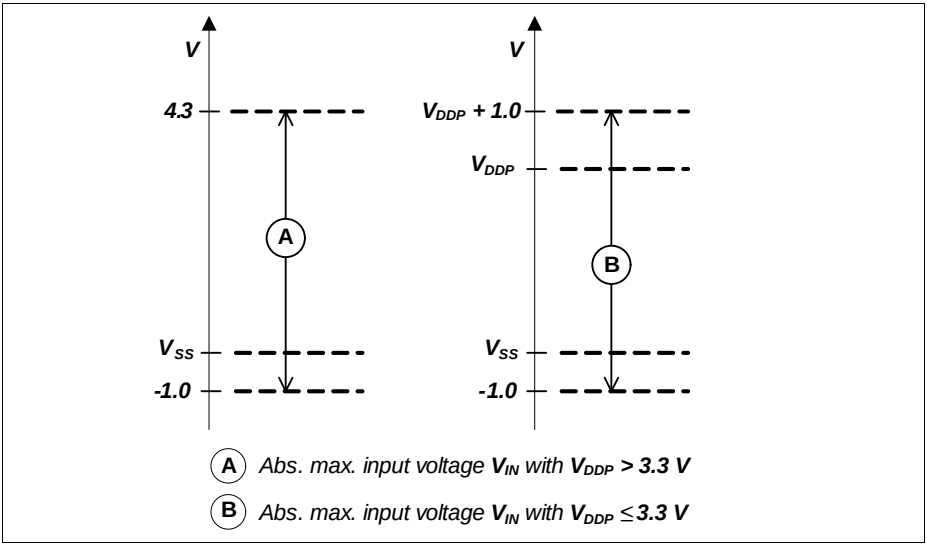

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4400. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 19 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	85	°C	Temp. Range F
			-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP}	SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC}	CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS}	SR	0	–	–	V	
ADC analog supply voltage	V_{DDA}	SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA}	SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3]	V_{BAT}	SR	1.95[4]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied too.
System Frequency	f_{SYS}	SR	–	–	120	MHz	
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5]	ΣI_{SC_PG}	SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 17**.

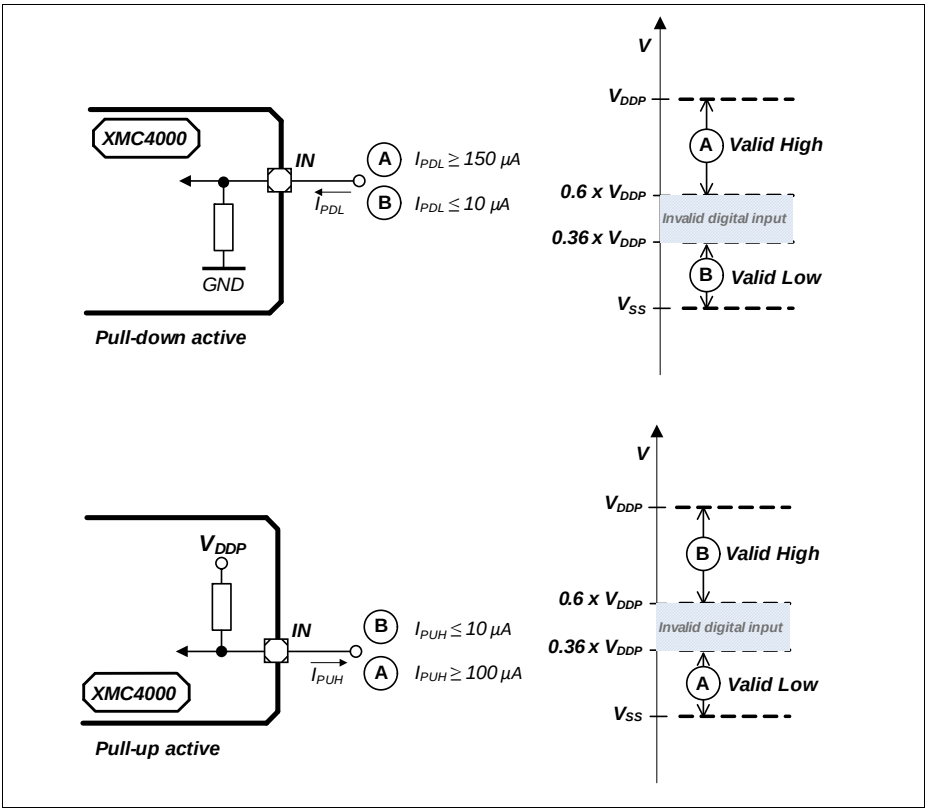

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 23 Standard Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Fall time	t_{FA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7.0	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft

The power-up calibration of the ADC requires a maximum number of 4 352 f_{ADCI} cycles.

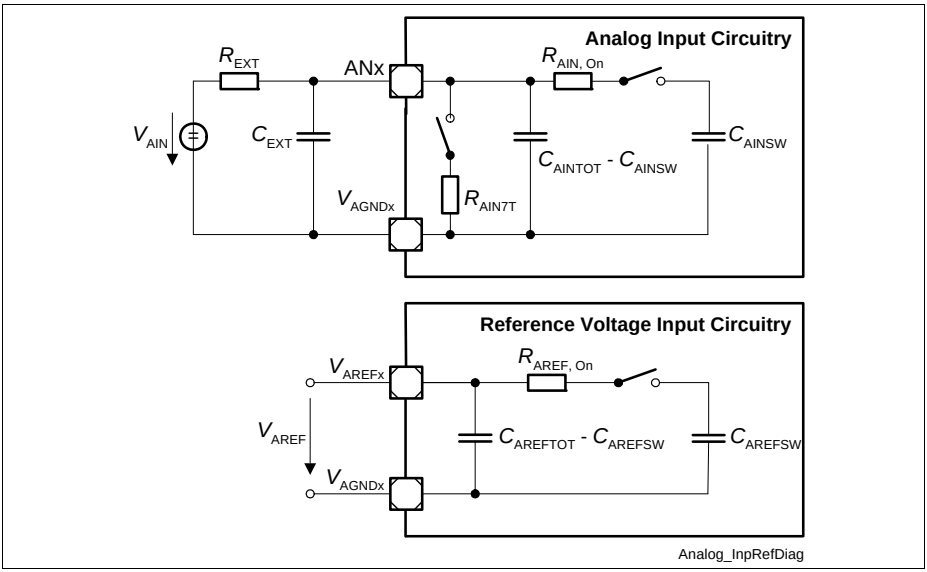

Figure 13 ADCx Input Circuits

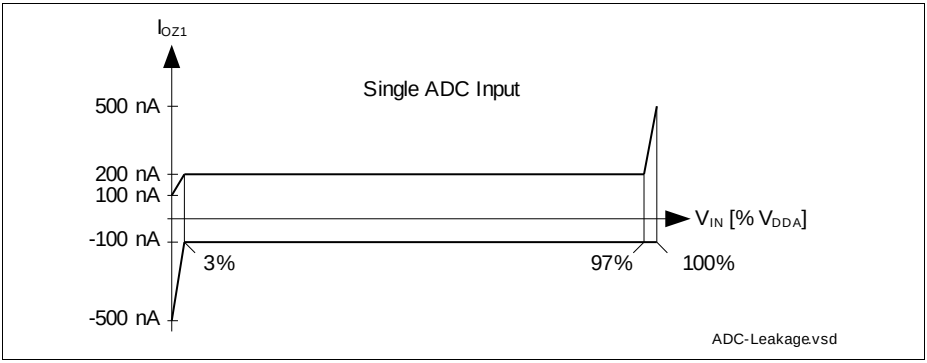

Figure 14 ADCx Analog Input Leakage Current

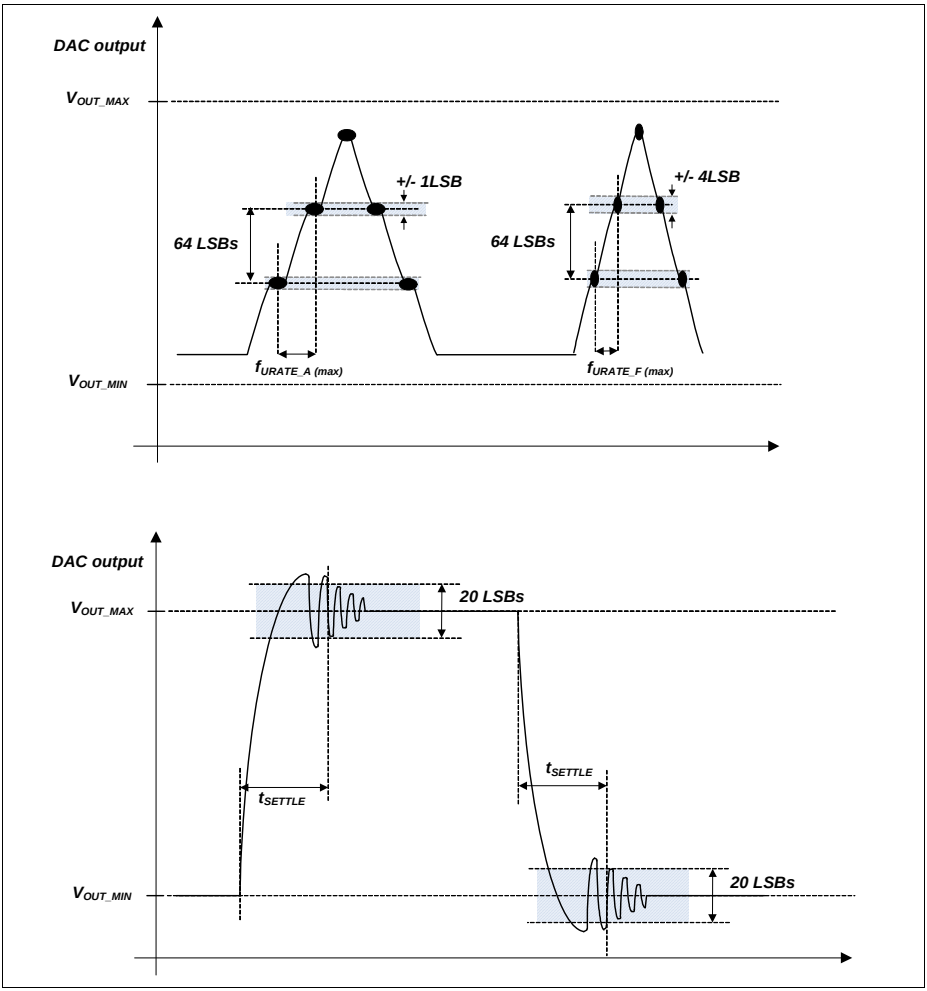

Figure 15 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	55	–	450	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	$V_{AIN} \geq V_{AREF} + 200$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	D_{CSG} CC	–	–	1	clk	
Bias startup time	t_{start} CC	–	–	98	us	
Bias supply current	I_{DDbias} CC	–	–	400	µA	
CSGy startup time	t_{CSGS} CC	–	–	2	µs	
Input operation current[1]	I_{DDCIN} CC	-10	–	33	µA	See **Figure 19**
High Speed Mode						
DAC output voltage range	V_{DOUT} CC	V_{SS}	–	V_{DDP}	V	
DAC propagation delay - Full scale	t_{FShs} CC	–	–	80	ns	See **Figure 20**
Input Selector propagation delay - Full scale	t_{Dhs} CC	–	–	100	ns	See **Figure 20**
Comparator bandwidth	t_{Dhs} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDhs} CC	–	–	940	µA	
Low Speed Mode						
DAC output voltage range	V_{DOUT} CC	$0.1 \times V_{DDP}$[2]	–	V_{DDP}	V	
DAC propagation delay - Full Scale	t_{FSls} CC	–	–	160	ns	See **Figure 20**
Input Selector propagation delay - Full Scale	t_{Dls} CC	–	–	200	ns	See **Figure 20**
Comparator bandwidth	t_{Dls} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDls} CC	–	–	300	µA	

1) Typical input resistance R_{CIN} = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

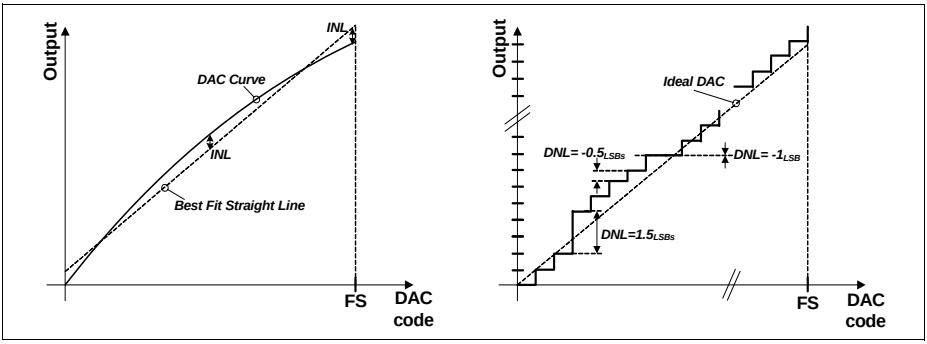

Figure 18 CSG DAC INL and DNL example

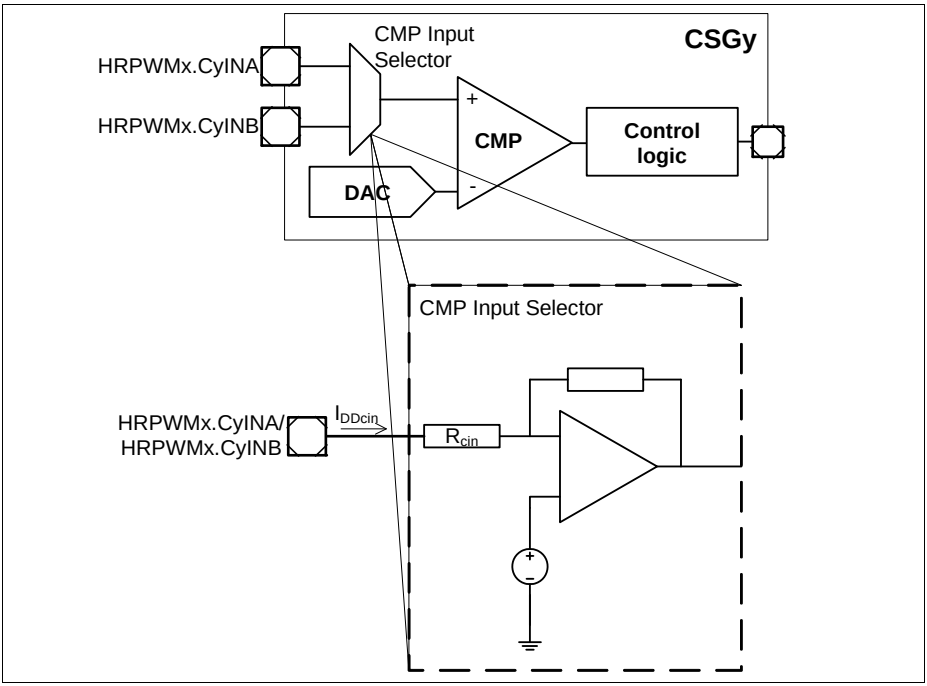

Figure 19 Input operation current

Peripheral Idle Currents

Test conditions:

- f_{sys} and derived clocks at 120 MHz
- V_{DDP} = 3.3 V, T_a =25 °C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity
- the given values are a result of differential measurements with asserted and deasserted peripheral reset and enabled clock of the peripheral under test

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

Table 40 Peripheral Idle Currents

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORTS ETH USB FCE WDT POSIFx	I_{PER} CC	–	≤ 0.3	–	mA	
MultiCAN ERU LEDTSCU0 CCU4x CCU8x		–	≤ 1.0	–		
DAC (digital)[1)]		–	1.3	–		
USICx		–	3.0	–		
DSD VADC (digital)[1)]		–	4.5	–		
DMAx		–	6.0	–		

1) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

Table 41 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time[5)]

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH × (1 / f_{CPU}) ≥ t_a.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C.

5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 45 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	25	–	–	ns	
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	13	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.9 Peripheral Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 50 DSD Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MCLK period in master mode	t_1	CC	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in master mode	t_2	CC	9	–	–	ns	$t_2 > t_{PERIPH}$ [1]
MCLK low time in master mode	t_3	CC	9	–	–	ns	$t_3 > t_{PERIPH}$ [1]
MCLK period in slave mode	t_1	SR	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in slave mode	t_2	SR	t_{PERIPH}	–	–	ns	[1]
MCLK low time in slave mode	t_3	SR	t_{PERIPH}	–	–	ns	[1]
DIN input setup time to the active clock edge	t_4	SR	t_{PERIPH} + 4	–	–	ns	[1]
DIN input hold time from the active clock edge	t_5	SR	t_{PERIPH} + 3	–	–	ns	[1]

1) $t_{PERIPH} = 1 / f_{PERIPH}$

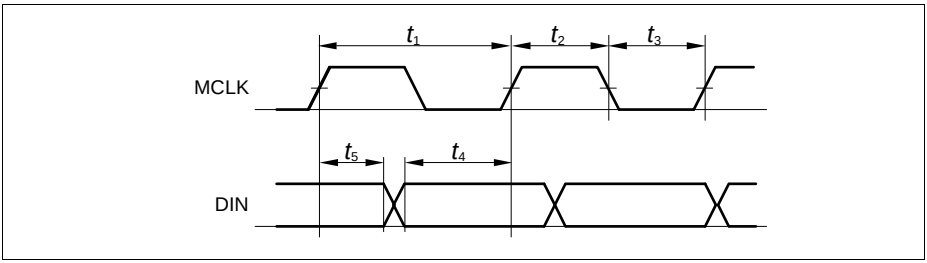

Figure 33 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 51 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

Table 52 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

4 Package and Reliability

The XMC4400 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 60 provides the thermal characteristics of the packages used in XMC4400.

Table 60 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions (including U-Groove where applicable)	Ex × Ey CC	-	7.0 × 7.0	mm	PG-LQFP-100-11
		-	7.0 × 7.0	mm	PG-LQFP-100-25
		-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
Exposed Die Pad dimensions excluding U-Groove	Ax × Ay CC	-	6.2 × 6.2	mm	PG-LQFP-100-25
Thermal resistance Junction-Ambient $T_J \leq 150$ °C	$R_{\Theta JA}$ CC	-	20.5	K/W	PG-LQFP-100-11[1)]
		-	20.0	K/W	PG-LQFP-100-25[1)]
		-	30.0	K/W	PG-LQFP-64-19[1)]
		-	22.5	K/W	PG-TQFP-64-19[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.