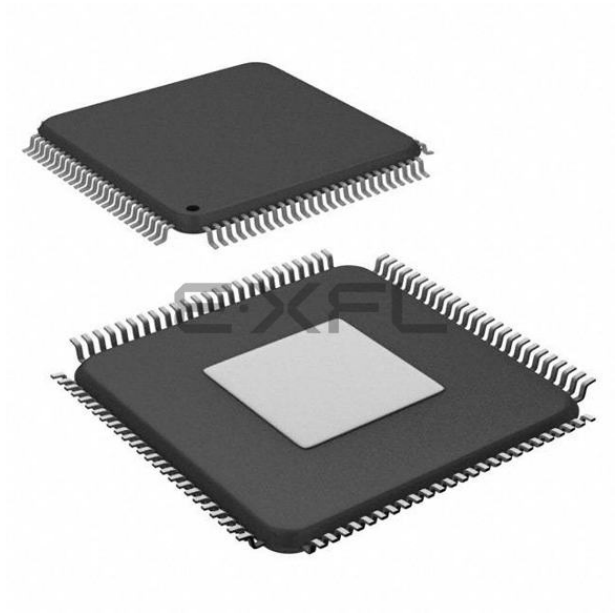
# Infineon Technologies - XMC4400F64F256BAXQMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SPI, UART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 14x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-25 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f64f256baxqma1 |

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# 1 Summary of Features

The XMC4400 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

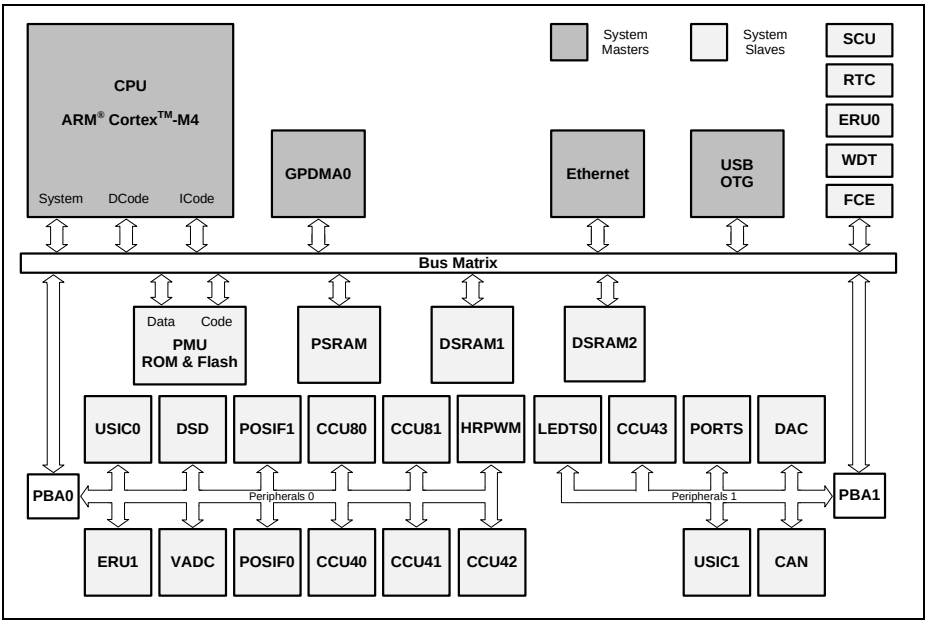


**Figure 1 System Block Diagram**

### CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

### 2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

**Table 11 Port I/O Function Description**

| Function | Outputs | | | Inputs | | |
|---|---|---|---|---|---|---|
| | ALT1 | ALTn | HWO0 | HWI0 | Input | Input |
| P0.0 | | MODA.OUT | MODB.OUT | MODB.INA | MODC.INA | |
| Pn.y | MODA.OUT | | | | MODA.INA | MODC.INB |

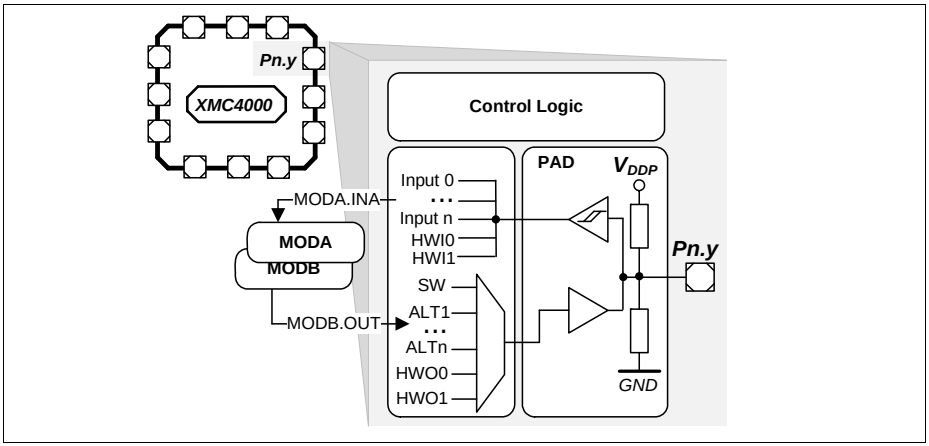


**Figure 6 Simplified Port Structure**

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

The XMC4400 has a common ground concept, all $V_{SS}$, $V_{SSA}$ and $V_{SSO}$ pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

$V_{AGND}$ is the low potential to the analog reference $V_{AREF}$. Depending on the application it can share the common ground or have a different potential. In devices with shared $V_{DDA}/V_{AREF}$ and $V_{SSA}/V_{AGND}$ pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When $V_{DDP}$ is supplied, $V_{BAT}$ must be supplied as well. If no other supply source (e.g. battery) is connected to $V_{BAT}$, the $V_{BAT}$ pin can also be connected directly to $V_{DDP}$.

**Table 23 Standard Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Input Leakage current | $I_{OZA2}$ CC | -6 | | 6 | µA | 0 V ≤ $V_{IN}$ < 0.5*$V_{DDP}$ - 1 V; 0.5*$V_{DDP}$ + 1 V <$V_{IN}$ ≤ $V_{DDP}$ |
| | | -3 | | 3 | µA | 0.5*$V_{DDP}$ - 1 V < $V_{IN}$ < 0.5*$V_{DDP}$ + 1 V |
| Input high voltage | $V_{IHA2}$ SR | 0.6 × $V_{DDP}$ | | $V_{DDP}$ + 0.3 | V | max. 3.6 V |
| Input low voltage | $V_{ILA2}$ SR | -0.3 | | 0.36 × $V_{DDP}$ | V | |
| Output high voltage, POD = weak | $V_{OHA2}$ CC | $V_{DDP}$ - 0.4 | | – | V | $I_{OH}$ ≥ -400 µA |
| | | 2.4 | | – | V | $I_{OH}$ ≥ -500 µA |
| Output high voltage, POD = medium | | $V_{DDP}$ - 0.4 | | – | V | $I_{OH}$ ≥ -1.4 mA |
| | | 2.4 | | – | V | $I_{OH}$ ≥ -2 mA |
| Output high voltage, POD = strong | | $V_{DDP}$ - 0.4 | | – | V | $I_{OH}$ ≥ -1.4 mA |
| | | 2.4 | | – | V | $I_{OH}$ ≥ -2 mA |
| Output low voltage, POD = weak | $V_{OLA2}$ CC | – | | 0.4 | V | $I_{OL}$ ≤ 500 µA |
| Output low voltage, POD = medium | | – | | 0.4 | V | $I_{OL}$ ≤ 2 mA |
| Output low voltage, POD = strong | | – | | 0.4 | V | $I_{OL}$ ≤ 2 mA |

4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of $t_c$ = 550 ns results in a typical average current of $I_{AREF}$ = 54.5 µA.

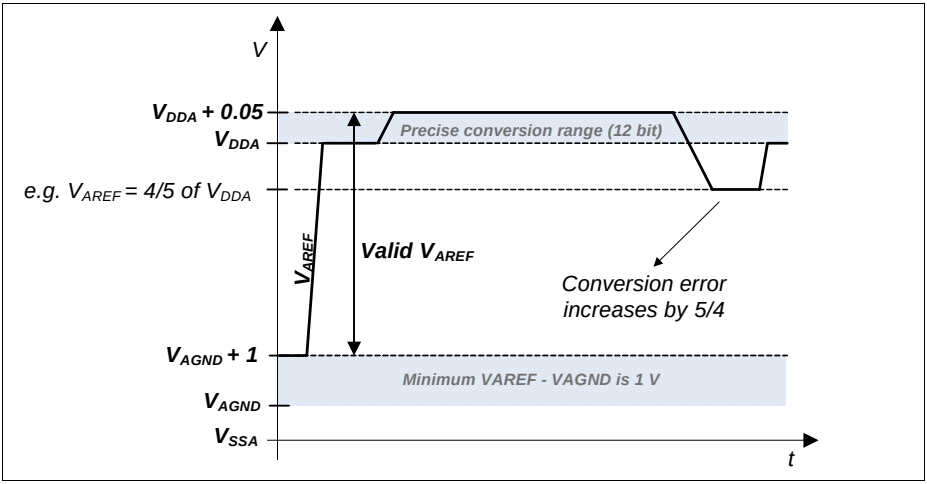


**Figure 12 VADC Reference Voltage Range**

The power-up calibration of the ADC requires a maximum number of 4 352 $f_{ADCI}$ cycles.

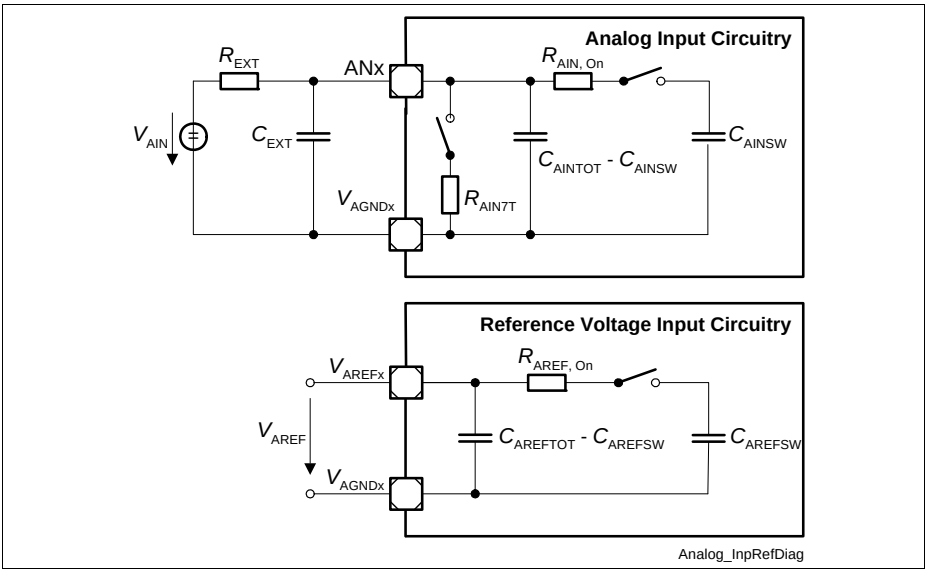


**Figure 13 ADCx Input Circuits**

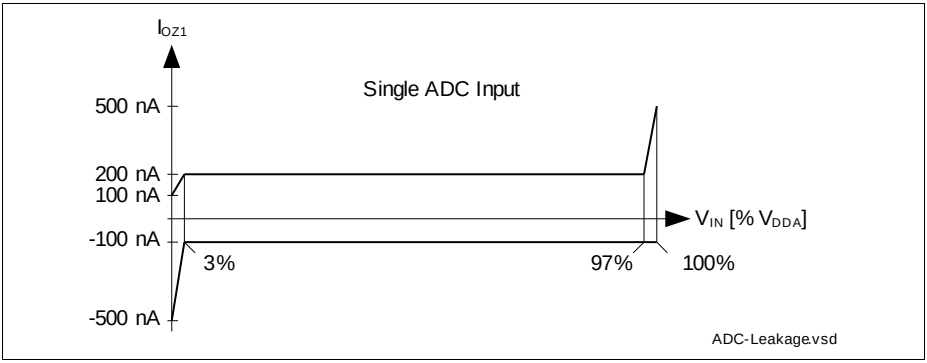


**Figure 14 ADCx Analog Input Leakage Current**

### 3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock, $f_{hrpwm}$.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.2.5.1 HRC characteristics

**Table 29** summarizes the characteristics of the HRC units.

**Table 29 HRC characteristics** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| High resolution step size[1)2)] | $t_{HRS}$ CC | – | 150 | – | ps | |
| Startup time (after reset release) | $t_{start}$ CC | – | – | 2 | µs | |

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

#### 3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

**Table 30 CMP and 10-bit DAC characteristics** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAC Resolution | *RES* CC | | 10 | | bits | |
| DAC differential nonlinearity | *DNL CC* | -1 | – | 1.5 | LSB | Monotonic behavior, See **Figure 18** |
| DAC integral nonlinearity | *INL* CC | -3 | – | 3 | LSB | See **Figure 18** |

### 3.2.9 Oscillator Pins

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

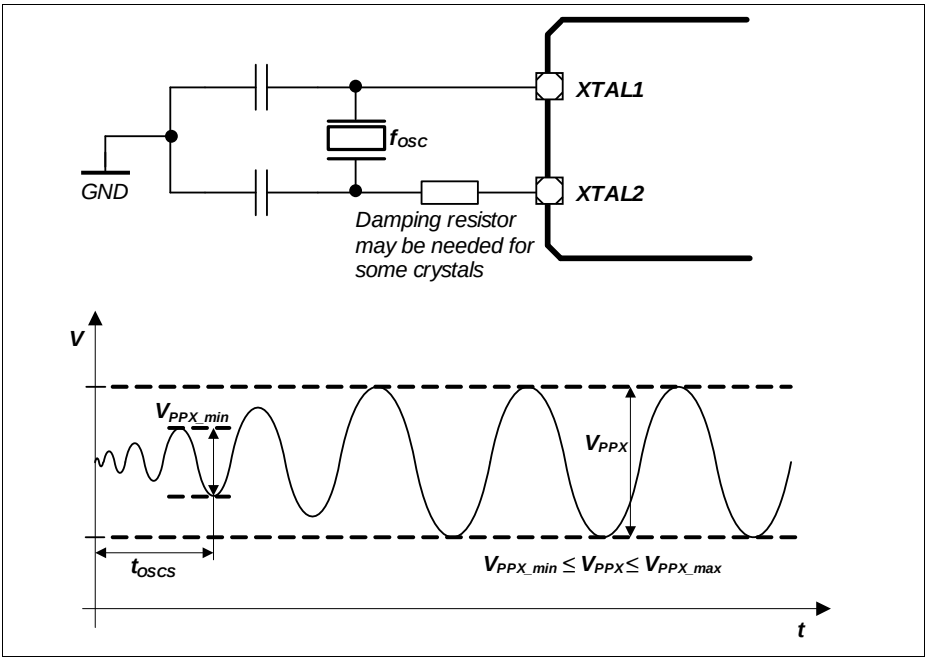


**Figure 21 Oscillator in Crystal Mode**

**Table 39 Power Supply Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Dissipation | $P_{DISS}$ | CC | – | – | 1 | W | $V_{DDP}$ = 3.6 V, $T_J$ = 150 °C |
| Wake-up time from Sleep to Active mode | $t_{SSA}$ | CC | – | 6 | – | cycles | |
| Wake-up time from Deep Sleep to Active mode | | | – | – | – | ms | Defined by the wake-up of the Flash module, see **Section 3.2.11** |
| Wake-up time from Hibernate mode | | | – | – | – | ms | Wake-up via power-on reset event, see **Section 3.3.2** |

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. Ethernet, USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: $f_{SYS}$ = 120 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
   The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) $I_{DDP}$ decreases typically by 5 mA when $f_{SYS}$ decreases by 10 MHz, at constant $T_J$
11) Sum of currents of all active converters (ADC and DAC)

### Peripheral Idle Currents

Test conditions:

- $f_{sys}$ and derived clocks at 120 MHz
- $V_{DDP}$ = 3.3 V, $T_a$ =25 °C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity
- the given values are a result of differential measurements with asserted and deasserted peripheral reset and enabled clock of the peripheral under test

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

**Table 40 Peripheral Idle Currents**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| PORTS<br>ETH<br>USB<br>FCE<br>WDT<br>POSIFx | $I_{PER}$ CC | – | ≤ 0.3 | – | mA | |
| MultiCAN<br>ERU<br>LEDTSCU0<br>CCU4x<br>CCU8x | | – | ≤ 1.0 | – | | |
| DAC (digital)[1)] | | – | 1.3 | – | | |
| USICx | | – | 3.0 | – | | |
| DSD<br>VADC (digital)[1)] | | – | 4.5 | – | | |
| DMAx | | – | 6.0 | – | | |

1) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

### 3.2.11 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 41 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per 256 Kbyte Sector | $t_{ERP}$ CC | – | 5 | 5.5 | s | |
| Erase Time per 64 Kbyte Sector | $t_{ERP}$ CC | – | 1.2 | 1.4 | s | |
| Erase Time per 16 Kbyte Logical Sector | $t_{ERP}$ CC | – | 0.3 | 0.4 | s | |
| Program time per page[1)] | $t_{PRP}$ CC | – | 5.5 | 11 | ms | |
| Erase suspend delay | $t_{FL\_ErSusp}$ CC | – | – | 15 | ms | |
| Wait time after margin change | $t_{FL\_MarginDel}$ CC | 10 | – | – | µs | |
| Wake-up time | $t_{WU}$ CC | – | – | 270 | µs | |
| Read access time | $t_a$ CC | 20 | – | – | ns | For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2)] |
| Data Retention Time, Physical Sector[3)4)] | $t_{RET}$ CC | 20 | – | – | years | Max. 1000 erase/program cycles |
| Data Retention Time, Logical Sector[3)4)] | $t_{RETL}$ CC | 20 | – | – | years | Max. 100 erase/program cycles |

### 3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when $V_{DDP}$ and/or $V_{DDC}$ violate the respective thresholds.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

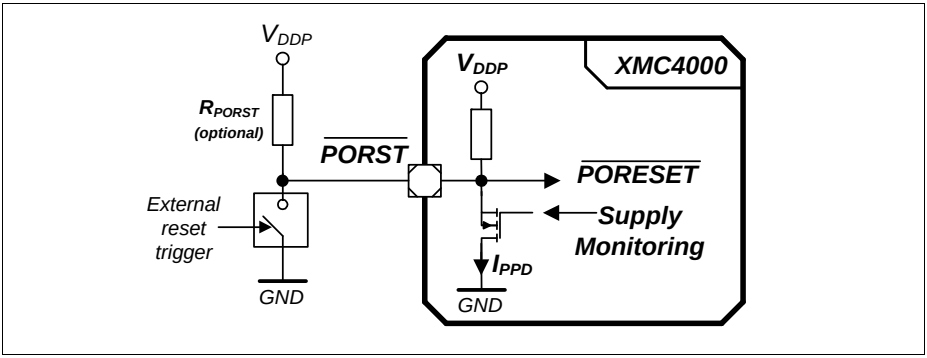


**Figure 26 $\overline{\text{PORST}}$ Circuit**

**Table 42 Supply Monitoring Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage reset threshold | $V_{POR}$ CC | 2.79[1] | – | 3.05[2] | V | [3] |
| Core supply voltage reset threshold | $V_{PV}$ CC | – | – | 1.17 | V | |
| $V_{DDP}$ voltage to ensure defined pad states | $V_{DDPPA}$ CC | – | 1.0 | – | V | |
| $\overline{\text{PORST}}$ rise time | $t_{PR}$ SR | – | – | 2 | µs | |
| Startup time from power-on reset with code execution from Flash | $t_{SSW}$ CC | – | 2.5 | 3.5 | ms | Time to the first user code instruction |
| $V_{DDC}$ ramp up time | $t_{VCR}$ CC | – | 550 | – | µs | Ramp up after power-on or after a reset triggered by a violation of $V_{POR}$ or $V_{PV}$ |

1) Minimum threshold for reset assertion.

### 3.3.5 Internal Clock Source Characteristics

**Fast Internal Clock Source**

**Table 45 Fast Internal Clock Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{OFINC}$ CC | – | 36.5 | – | MHz | not calibrated |
| | | – | 24 | – | MHz | calibrated |
| Accuracy | $\Delta f_{OFI}$ CC | -0.5 | – | 0.5 | % | automatic calibration[1)2)] |
| | | -15 | – | 15 | % | factory calibration, $V_{DDP}$ = 3.3 V |
| | | -25 | – | 25 | % | no calibration, $V_{DDP}$ = 3.3 V |
| | | -7 | – | 7 | % | Variation over voltage range[3)] 3.13 V ≤ $V_{DDP}$ ≤ 3.63 V |
| Start-up time | $t_{OFIS}$ CC | – | 50 | – | µs | |

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the $V_{DDP}$ supply voltage.

3) Deviations from the nominal $V_{DDP}$ voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

### 3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

**Table 47 JTAG Interface Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ | SR | 25 | – | – | ns | |
| TCK high time | $t_2$ | SR | 10 | – | – | ns | |
| TCK low time | $t_3$ | SR | 10 | – | – | ns | |
| TCK clock rise time | $t_4$ | SR | – | – | 4 | ns | |
| TCK clock fall time | $t_5$ | SR | – | – | 4 | ns | |
| TDI/TMS setup to TCK rising edge | $t_6$ | SR | 6 | – | – | ns | |
| TDI/TMS hold after TCK rising edge | $t_7$ | SR | 6 | – | – | ns | |
| TDO valid after TCK falling edge[1] (propagation delay) | $t_8$ | CC | – | – | 13 | ns | $C_L$ = 50 pF |
| | | | 3 | – | – | ns | $C_L$ = 20 pF |
| TDO hold after TCK falling edge[1] | $t_{18}$ | CC | 2 | – | – | ns | |
| TDO high imped. to valid from TCK falling edge[1)2)] | $t_9$ | CC | – | – | 14 | ns | $C_L$ = 50 pF |
| TDO valid to high imped. from TCK falling edge[1] | $t_{10}$ | CC | – | – | 13.5 | ns | $C_L$ = 50 pF |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

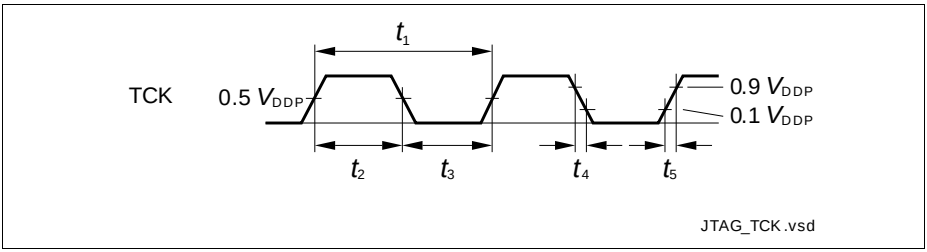


**Figure 28 Test Clock Timing (TCK)**

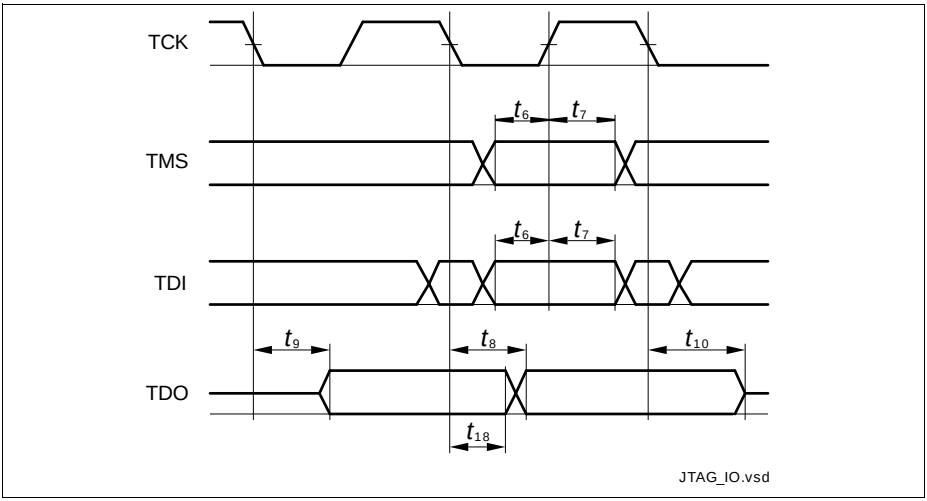


**Figure 29 JTAG Timing**

### 3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

*Note: Operating Conditions apply.*

**Table 53 USIC IIC Standard Mode Timing[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ CC/SR | - | - | 300 | ns | |
| Rise time of both SDA and SCL | $t_2$ CC/SR | - | - | 1000 | ns | |
| Data hold time | $t_3$ CC/SR | 0 | - | - | µs | |
| Data set-up time | $t_4$ CC/SR | 250 | - | - | ns | |
| LOW period of SCL clock | $t_5$ CC/SR | 4.7 | - | - | µs | |
| HIGH period of SCL clock | $t_6$ CC/SR | 4.0 | - | - | µs | |
| Hold time for (repeated) START condition | $t_7$ CC/SR | 4.0 | - | - | µs | |
| Set-up time for repeated START condition | $t_8$ CC/SR | 4.7 | - | - | µs | |
| Set-up time for STOP condition | $t_9$ CC/SR | 4.0 | - | - | µs | |
| Bus free time between a STOP and START condition | $t_{10}$ CC/SR | 4.7 | - | - | µs | |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

### 3.3.11 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.11.1 ETH Measurement Reference Points

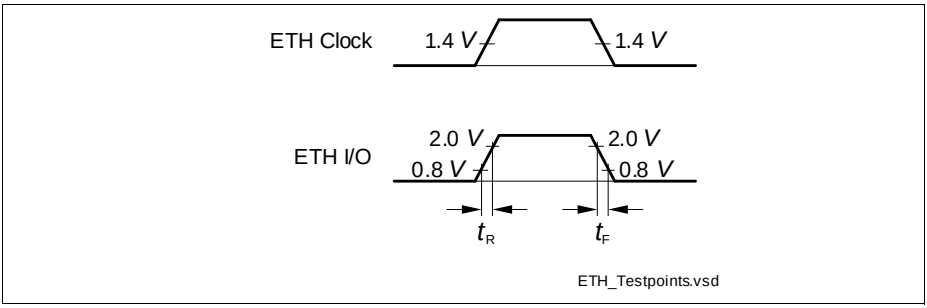


**Figure 39 ETH Measurement Reference Points**

### 3.3.11.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

**Table 59 ETH RMII Signal Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| ETH_RMII_REF_CL clock period | $t_{13}$ | SR | 20 | – | – | ns | $C_L$ = 25 pF; 50 ppm |
| ETH_RMII_REF_CL clock high time | $t_{14}$ | SR | 7 | – | 13 | ns | $C_L$ = 25 pF |
| ETH_RMII_REF_CL clock low time | $t_{15}$ | SR | 7 | – | 13 | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time | $t_{16}$ | SR | 4 | – | – | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time | $t_{17}$ | SR | 2 | – | – | ns | |
| ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid | $t_{18}$ | CC | 4 | – | 15 | ns | |

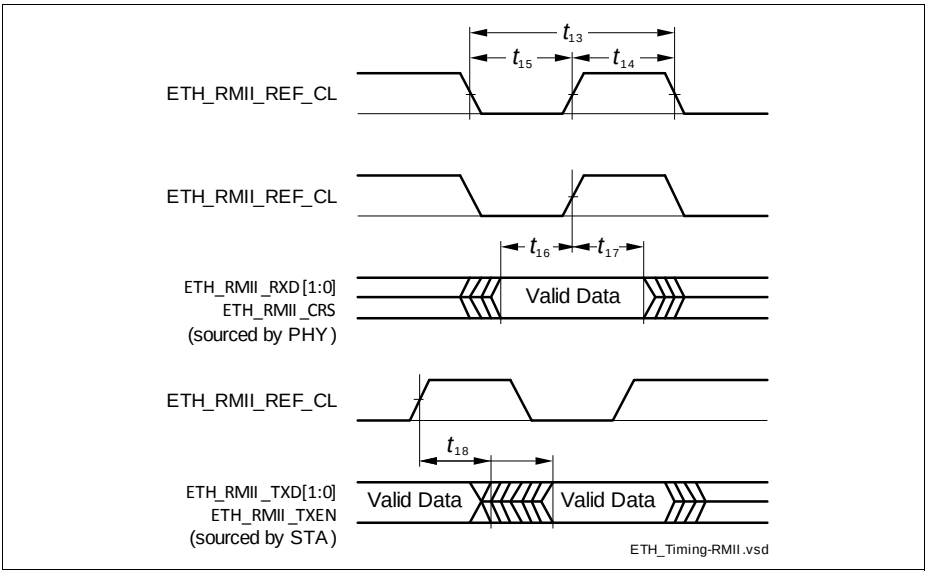


**Figure 41 ETH RMII Signal Timing**