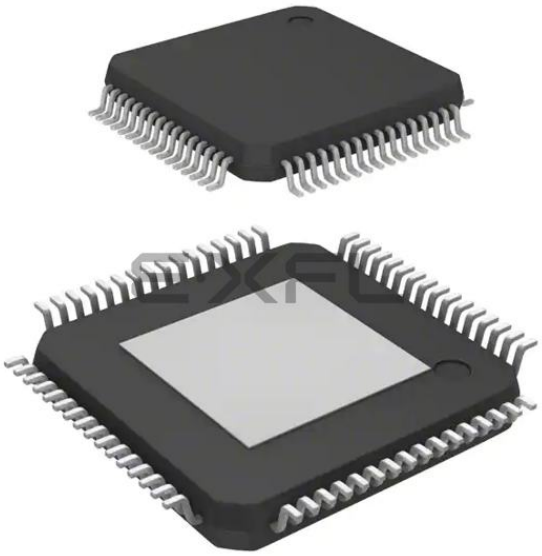
Infineon Technologies - XMC4400F64K256ABXQSA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f64k256abxqsa1

Table of Contents

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4400 series devices.

The document describes the characteristics of a superset of the XMC4400 series devices. For simplicity, the various device types are referred to by the collective term XMC4400 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4400 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4400** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4400 Device Types

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4400-F100x512	PG-LQFP-100	512	80
XMC4400-F64x512	PG-yQFP-64[2)]	512	80
XMC4400-F100x256	PG-LQFP-100	256	80
XMC4400-F64x256	PG-yQFP-64[2)]	256	80
XMC4402-F100x256	PG-LQFP-100	256	80
XMC4402-F64x256	PG-yQFP-64[2)]	256	80

1) x is a placeholder for the supported temperature range.

2) y is a placeholder for the QFP package variant, LQFP or TQFP depending on the stepping, see **Section 1.3**.

Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3
PG-LQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6	CH0, CH1	CH2, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4400 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	$0004\ 4001_H$	EES-AA, ES-AA
SCU_IDCHIP	$0004\ 4002_H$	ES-AB, AB
SCU_IDCHIP	$0004\ 4003_H$	BA
JTAG IDCODE	$101D\ C083_H$	EES-AA, ES-AA
JTAG IDCODE	$201D\ C083_H$	ES-AB, AB
JTAG IDCODE	$301D\ C083_H$	BA

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P3.0	7	-	A2	
P3.1	6	-	A2	
P3.2	5	-	A2	
P3.3	93	-	A1+	
P3.4	92	-	A1+	
P3.5	91	-	A2	
P3.6	90	-	A2	
P4.0	85	-	A2	
P4.1	84	-	A2	
P5.0	58	-	A1+	
P5.1	57	-	A1+	
P5.2	56	-	A1+	
P5.7	55	-	A1+	
P14.0	31	20	AN/DIG_IN	
P14.1	30	-	AN/DIG_IN	
P14.2	29	-	AN/DIG_IN	
P14.3	28	19	AN/DIG_IN	
P14.4	27	18	AN/DIG_IN	
P14.5	26	17	AN/DIG_IN	
P14.6	25	16	AN/DIG_IN	
P14.7	24	15	AN/DIG_IN	
P14.8	37	24	AN/DAC/DIG_IN	
P14.9	36	23	AN/DAC/DIG_IN	
P14.12	23	-	AN/DIG_IN	
P14.13	22	-	AN/DIG_IN	
P14.14	21	14	AN/DIG_IN	
P14.15	20	-	AN/DIG_IN	
P15.2	19	-	AN/DIG_IN	
P15.3	18	-	AN/DIG_IN	
P15.8	39	-	AN/DIG_IN	
P15.9	38	-	AN/DIG_IN	

2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

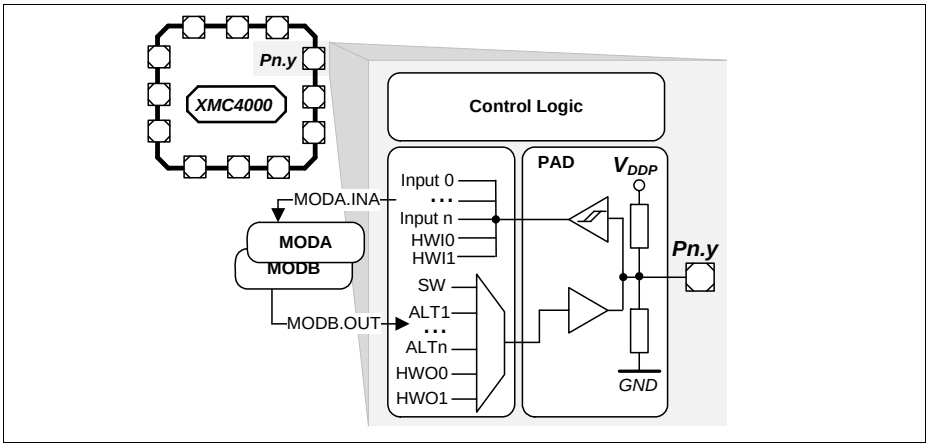

Figure 6 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 12 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P3.0		U0C1. SCLKOUT	CCU42. OUT0				U0C1. DX1B				CCU80. IN2C	CCU81. IN0C		
P3.1		U0C1. SELO0					U0C1. DX2B		ERU0. 0B1		CCU80. IN1C			
P3.2	USB. DRIVEVBUS	CAN. N0_TXD		LEDTS0. COLA					ERU0. 0A1		CCU80. IN0C			
P3.3		U1C1. SELO1	CCU42. OUT3					DSD. DIN3B			CCU42. IN3A	CCU80. IN3B		
P3.4		U1C1. SELO2	CCU42. OUT2	DSD. MCLK3				DSD. MCLK3B			CCU42. IN2A	CCU80. IN0B		
P3.5		U1C1. SELO3	CCU42. OUT1	U0C1. DOUT0					ERU0. 3B1		CCU42. IN1A			
P3.6		U1C1. SELO4	CCU42. OUT0	U0C1. SCLKOUT	DB. ETM_TRACEDATA0				ERU0. 3A1		CCU42. IN0A			
P4.0			DSD. MCLK1		DB. ETM_TRACEDATA1		U1C1. DX1C	DSD. MCLK1B	U0C1. DX0E					
P4.1		U1C1. MCLKOUT	DSD. MCLK0	U0C1. SELO0	DB. ETM_TRACEDATA2			DSD. MCLK0B			DSD. MCLK1D			
P5.0		DSD. CGPWMN	CCU81. OUT33					ETH0. RXD0D	U0C0. DX0D		CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. CGPWMP	CCU81. OUT32					ETH0. RXD1D			CCU81. IN0B			
P5.2			CCU81. OUT23					ETH0. CRS_DVD			CCU81. IN1B			ETH0. RXDVD
P5.7			CCU81. OUT02	LEDTS0. COLA										
P14.0							VADC. G0CH0							
P14.1							VADC. G0CH1							
P14.2							VADC. G0CH2	VADC. G1CH2						
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4							VADC. G0CH4		VADC. G2CH0					
P14.5							VADC. G0CH5		VADC. G2CH1		POSIF0. IN2B			
P14.6							VADC. G0CH6				POSIF0. IN1B		G0ORC6	
P14.7							VADC. G0CH7				POSIF0. IN0B		G0ORC7	
P14.8					DAC. OUT_0			VADC. G1CH0		VADC. G3CH2	ETH0. RXD0C			

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4400 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4400 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4400 is designed in.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ CC	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ SR	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Offset error	ED_{OFF}	CC		±20		mV	
Gain error	ED_{G_IN}	CC	-5	0	5	%	
Startup time	$t_{STARTUP}$	CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1}	CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE}	CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK}	CC	–	0.6	–	mA	
Output resistance	R_{OUT}	CC	–	50	–	Ohm	
Load resistance	R_L	SR	5	–	–	kOhm	
Load capacitance	C_L	SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR*	CC	–	56	–	dB	to V_{DDA} verified by design

1) According to best straight line method.

Conversion Calculation

Unsigned:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})
Signed:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	D_{CSG} CC	–	–	1	clk	
Bias startup time	t_{start} CC	–	–	98	us	
Bias supply current	I_{DDbias} CC	–	–	400	µA	
CSGy startup time	t_{CSGS} CC	–	–	2	µs	
Input operation current[1]	I_{DDCIN} CC	-10	–	33	µA	See **Figure 19**
High Speed Mode						
DAC output voltage range	V_{DOUT} CC	V_{SS}	–	V_{DDP}	V	
DAC propagation delay - Full scale	t_{FShs} CC	–	–	80	ns	See **Figure 20**
Input Selector propagation delay - Full scale	t_{Dhs} CC	–	–	100	ns	See **Figure 20**
Comparator bandwidth	t_{Dhs} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDhs} CC	–	–	940	µA	
Low Speed Mode						
DAC output voltage range	V_{DOUT} CC	$0.1 \times V_{DDP}$[2]	–	V_{DDP}	V	
DAC propagation delay - Full Scale	t_{FSls} CC	–	–	160	ns	See **Figure 20**
Input Selector propagation delay - Full Scale	t_{Dls} CC	–	–	200	ns	See **Figure 20**
Comparator bandwidth	t_{Dls} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDls} CC	–	–	300	µA	

1) Typical input resistance R_{CIN} = 100kOhm.

Table 32 External clock operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{eclk}	SR	–	–	$f_{hrpwm}/4$	MHz	
ON time	t_{oneclk}	SR	$2T_{ccu}$ [1)2)]	–	–	ns	
OFF time	$t_{offeclk}$	SR	$2T_{ccu}$ [1)2)]	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing V_{BAT} or another external sensor voltage V_{LPS} with a pre-programmed threshold voltage.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Low Power Analog Comparator Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
V_{BAT} supply voltage range for LPAC operation	V_{BAT}	SR	2.1	–	3.6	V	
Sensor voltage range	V_{LPCS}	CC	0	–	1.2	V	
Threshold step size	V_{th}	CC	–	18.75	–	mV	
Threshold trigger accuracy	ΔV_{th}	CC	–	–	±10	%	for V_{th} > 0.4 V
Conversion time	t_{LPCC}	CC	–	–	250	µs	
Average current consumption over time	I_{LPCAC}	CC	–	–	15	µA	conversion interval 10 ms[1)]
Current consumption during conversion	I_{LPCC}	CC	–	150	–	µA	[1)]

1) Single channel conversion, measuring V_{BAT} = 3.3 V, 8 cycles settling time

Table 36 USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DM pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \le V_{IN} \le V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

Table 39 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	104	–	mA	120 / 120 / 120
		–	93	–		120 / 60 / 60
		–	78	–		60 / 60 / 120
		–	57	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	72	–	mA	120 / 120 / 120
		–	71	–		120 / 60 / 60
		–	61	–		60 / 60 / 120
		–	52	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	8	–	mA	24 / 24 / 24
		–	5	–		4 / 4 / 4
		–	4	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	12.8	–	µA	V_{BAT} = 3.3 V
		–	9.0	–		V_{BAT} = 2.4 V
		–	7.7	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	12.0	–	µA	V_{BAT} = 3.3 V
		–	8.4	–		V_{BAT} = 2.4 V
		–	7.0	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA} CC	–	–	170 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	30	mA	V_{DDP} = 3.6 V, T_J = 150 °C

3.3.4 Phase Locked Loop (PLL) Characteristics

Main and USB PLL

Table 44 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 120 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	25	–	–	ns	
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	13	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 53 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 54 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

Table 62 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30.0 K/W	22.5 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.07}_{-0.04}$ mm
Exposed Die Pad outer dimensions	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	4.9 mm × 4.9 mm

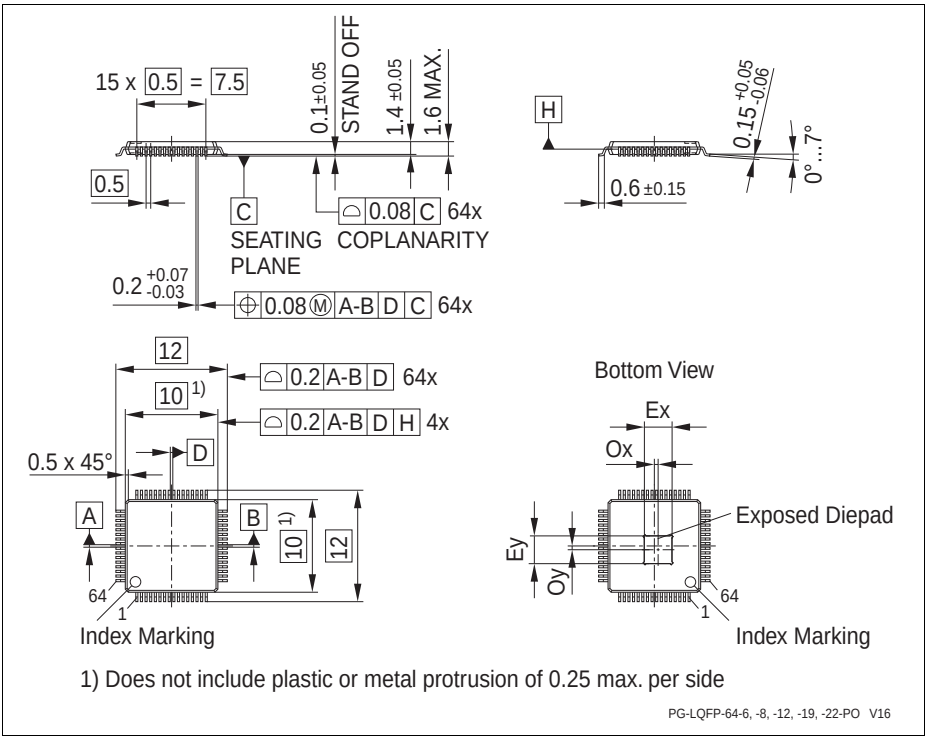

Figure 44 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)

5 Quality Declarations

The qualification of the XMC4400 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 63 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D