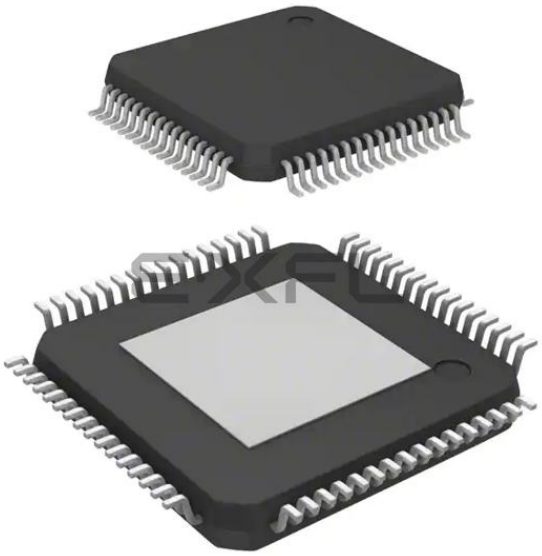
Infineon Technologies - XMC4400F64K512ABXQSA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	31
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f64k512abxqsa1

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On-Chip Memories

- 16 KB on-chip boot ROM
- 16 KB on-chip high-speed program memory
- 32 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication memory
- 512 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Four High Resoultion PWM (HRPWM) channels
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

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Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3
PG-LQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6	CH0, CH1	CH2, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4400 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	$0004\ 4001_H$	EES-AA, ES-AA
SCU_IDCHIP	$0004\ 4002_H$	ES-AB, AB
SCU_IDCHIP	$0004\ 4003_H$	BA
JTAG IDCODE	$101D\ C083_H$	EES-AA, ES-AA
JTAG IDCODE	$201D\ C083_H$	ES-AB, AB
JTAG IDCODE	$301D\ C083_H$	BA

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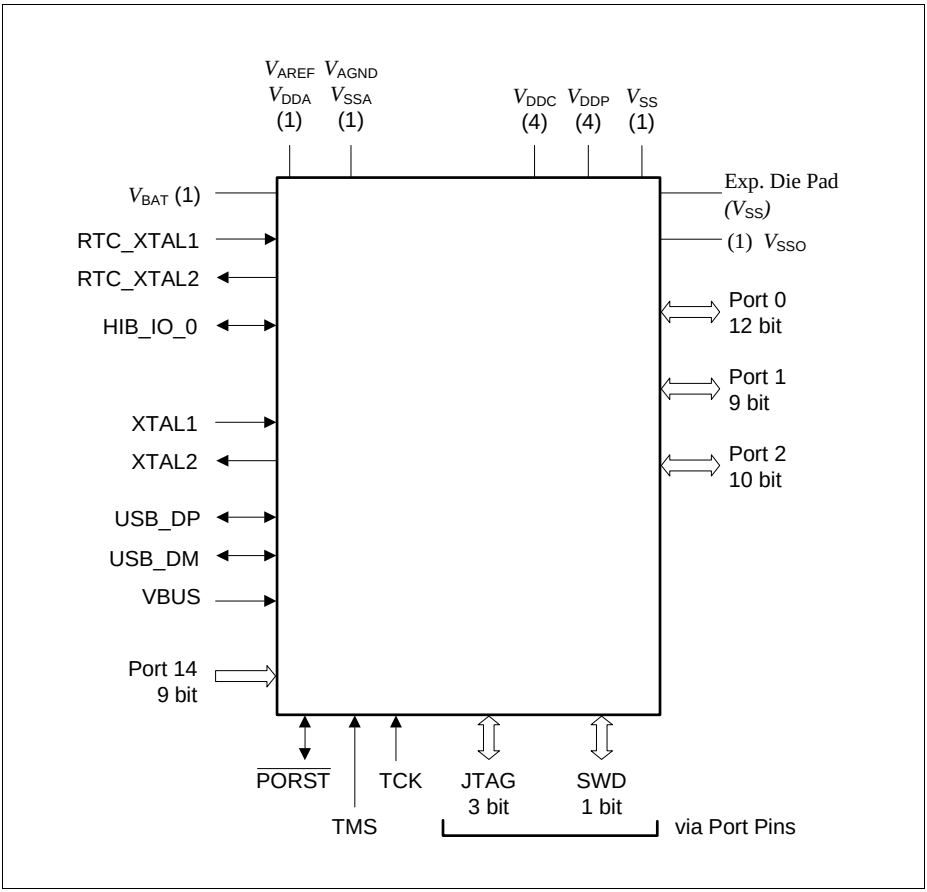

Figure 3 XMC4400 Logic Symbol PG-LQFP-64 and PG-TQFP-64

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Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
VDDA/VAREF	-	22	AN_Power/AN_Ref	Shared analog supply and reference voltage pin.
VSSA	34	-	AN_Power	
VSSA/VAGND	-	21	AN_Power/AN_Ref	Shared analog supply and reference ground pin.
VDDC	12	9	Power	
VDDC	42	25	Power	
VDDC	64	42	Power	
VDDC	86	55	Power	
VDDP	11	8	Power	
VDDP	43	26	Power	
VDDP	60	38	Power	
VDDP	87	56	Power	
VSS	59	37	Power	
VSSO	63	41	Power	
VSS	Exp. Pad	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

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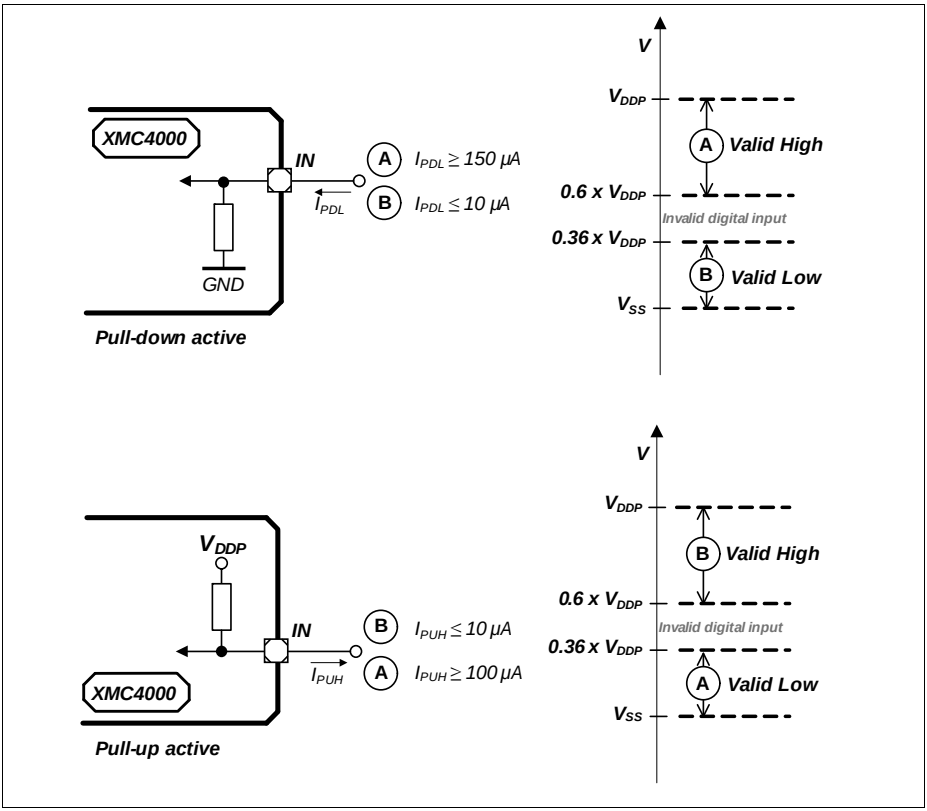

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 52 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6			ns	
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	3			ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	4			ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1)]	t_{12}	SR	6			ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1)]	t_{13}	SR	4			ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0		24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

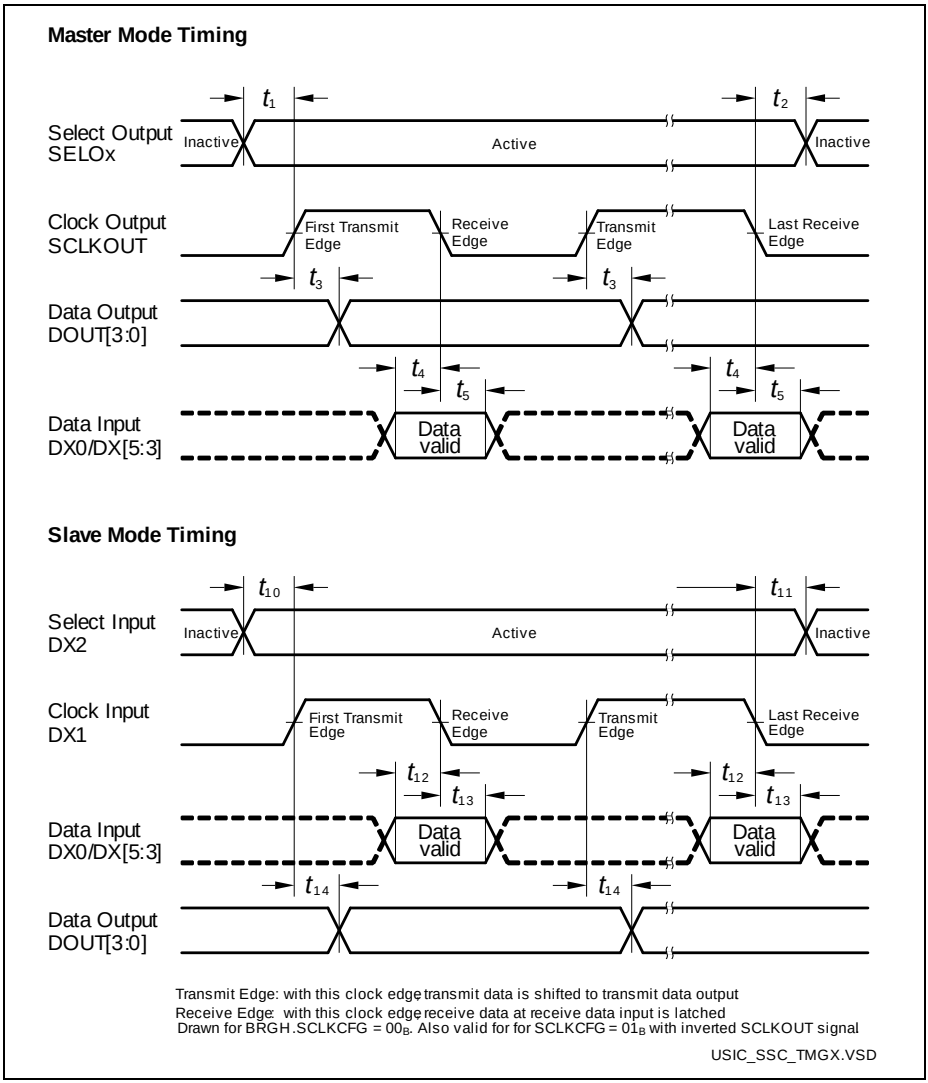

Figure 34 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

Table 62 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient (R_{4JA})	30.0 K/W	22.5 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.07}_{-0.04}$ mm
Exposed Die Pad outer dimensions	5.8 mm u5.8 mm	5.7 mm u5.7 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	4.9 mm u4.9 mm

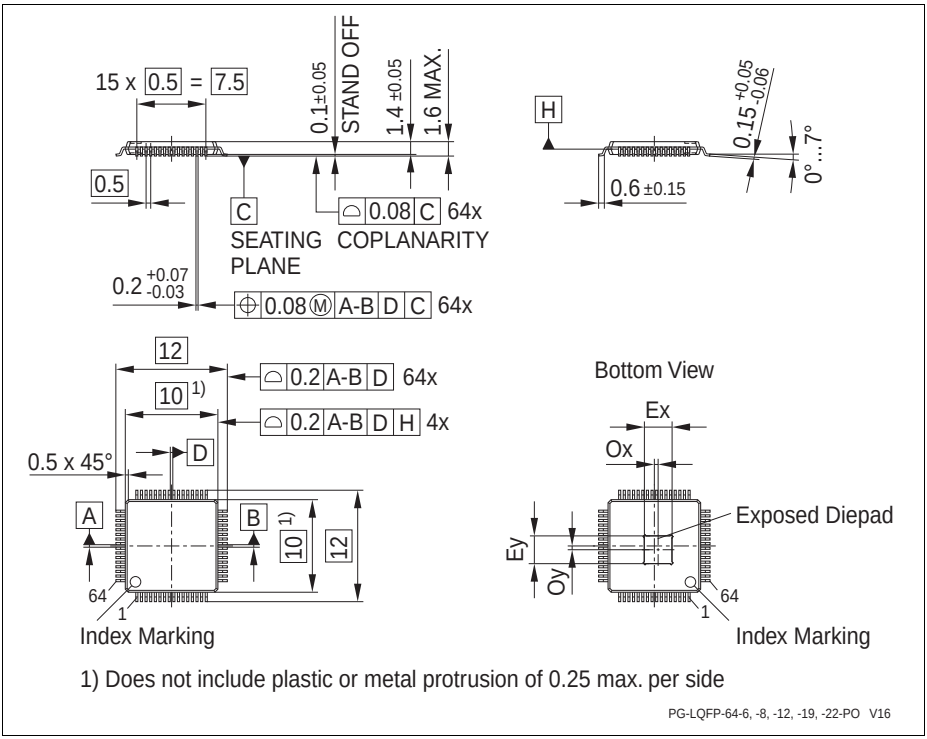

Figure 44 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)