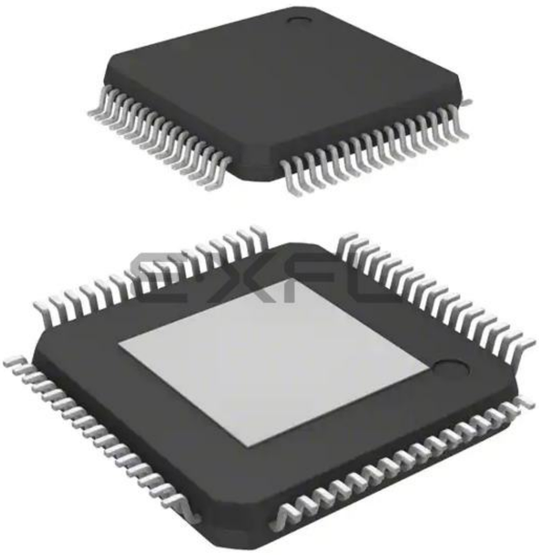

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**Applications of "Embedded - Microcontrollers"**

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SPI, UART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 14x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-64-19 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4400f64k512baxqma1 |

**XMC4400 Data Sheet**

**Revision History: V1.2 2015-12**

Previous Versions:
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

| Page | Subjects |
|---|---|
| 12 | Added a section listing the packages of the different markings. |
| 14 | Added BA marking variant. |
| 37 | Added footnote explaining minimum $V_{BAT}$ requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL. |
| 38 | Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver. |
| 38 | Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins. |
| 45 | Updated $C_{AINSW}$, $C_{AINTOT}$ and $R_{AIN}$ parameters with improved values. |
| 59 | Added footnote on test configuration for LPAC measurement. |
| 61 | Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP) |
| 66 | Relaxed RTC_XTAL $V_{PPX}$ parameter value and changed it to a system requirement. |
| 70 | Added footnote on current consumption by enabling of $f_{CCU}$. |
| 71 | Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 $N_{EPS4}$ for devices with BA marking. |
| many | Added PG-TQFP-64-19 and PG-LQFP-100-25 package information. |
| 97, 100 | Added tables describing the differences between PG-LQFP-100-11 to PG-LQFP-100-25 as well as PG-LQFP-64-19 to PG-TQFP-64-19 packages. |
| 102 | Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard. |

**Trademarks**

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### On-Chip Memories

- 16 KB on-chip boot ROM
- 16 KB on-chip high-speed program memory
- 32 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication memory
- 512 KB on-chip Flash Memory with 4 KB instruction cache

### Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

### Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

### Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Four High Resoultion PWM (HRPWM) channels
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for  system configuration and control

### Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

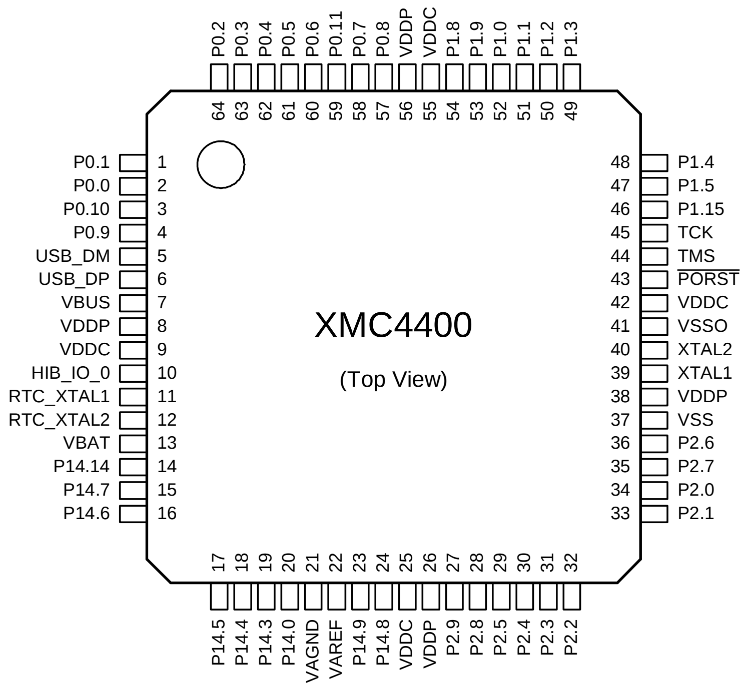


**Figure 5 XMC4400 PG-LQFP-64 and PG-TQFP-64 Pin Configuration** (top view)

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 13 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Con dition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Storage temperature | $T_{ST}$ | SR | -65 | – | 150 | °C | – |
| Junction temperature | $T_J$ | SR | -40 | – | 150 | °C | – |
| Voltage at 3.3 V power supply pins with respect to $V_{SS}$ | $V_{DDP}$ | SR | – | – | 4.3 | V | – |
| Voltage on any Class A and dedicated input pin with respect to $V_{SS}$ | $V_{IN}$ | SR | -1.0 | – | $V_{DDP}$ + 1.0 or max. 4.3 | V | whichever is lower |
| Voltage on any analog input pin with respect to $V_{AGND}$ | $V_{AIN}$ $V_{AREF}$ | SR | -1.0 | – | $V_{DDP}$ + 1.0 or max. 4.3 | V | whichever is lower |
| Input current on any pin during overload condition | $I_{IN}$ | SR | -10 | – | +10 | mA | |
| Absolute maximum sum of all input circuit currents for one port group during overload condition[1)] | $\Sigma I_{IN}$ | SR | -25 | – | +25 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | $\Sigma I_{IN}$ | SR | -100 | – | +100 | mA | |

1) The port groups are defined in **Table 17**.

**Figure 8** explains the input voltage ranges of $V_{IN}$ and $V_{AIN}$ and its dependency to the supply level of $V_{DDP}$.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above $V_{DDP}$. For the range up to $V_{DDP}$ + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

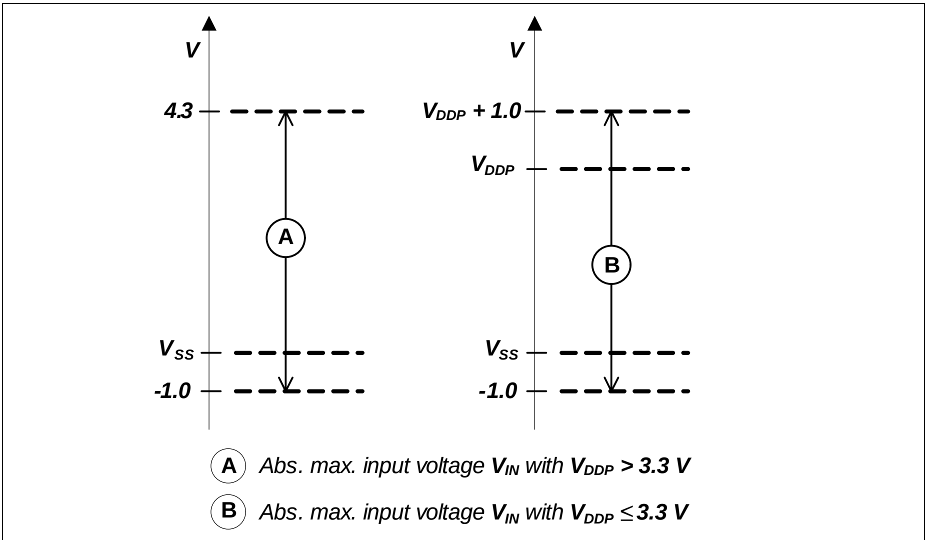


**Figure 8 Absolute Maximum Input Voltage Ranges**

## 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 14** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ($V_{DDP}$ or $V_{DDA}$)
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

**Table 22 Standard Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Output high voltage, POD[1] = weak | $V_{OHA1+}$ CC | $V_{DDP}$ - 0.4 | | – | V | $I_{OH} \geq$ -400 µA |
| | | 2.4 | | – | V | $I_{OH} \geq$ -500 µA |
| Output high voltage, POD[1] = medium | | $V_{DDP}$ - 0.4 | | – | V | $I_{OH} \geq$ -1.4 mA |
| | | 2.4 | | – | V | $I_{OH} \geq$ -2 mA |
| Output high voltage, POD[1] = strong | | $V_{DDP}$ - 0.4 | | – | V | $I_{OH} \geq$ -1.4 mA |
| | | 2.4 | | – | V | $I_{OH} \geq$ -2 mA |
| Output low voltage | $V_{OLA1+}$ CC | – | | 0.4 | V | $I_{OL} \leq$ 500 µA; POD[1] = weak |
| | | – | | 0.4 | V | $I_{OL} \leq$ 2 mA; POD[1] = medium |
| | | – | | 0.4 | V | $I_{OL} \leq$ 2 mA; POD[1] = strong |
| Fall time | $t_{FA1+}$ CC | – | | 150 | ns | $C_L$ = 20 pF; POD[1] = weak |
| | | – | | 50 | ns | $C_L$ = 50 pF; POD[1] = medium |
| | | – | | 28 | ns | $C_L$ = 50 pF; POD[1] = strong; edge = slow |
| | | – | | 16 | ns | $C_L$ = 50 pF; POD[1] = strong; edge = soft; |
| Rise time | $t_{RA1+}$ CC | – | | 150 | ns | $C_L$ = 20 pF; POD[1] = weak |
| | | – | | 50 | ns | $C_L$ = 50 pF; POD[1] = medium |
| | | – | | 28 | ns | $C_L$ = 50 pF; POD[1] = strong; edge = slow |
| | | – | | 16 | ns | $C_L$ = 50 pF; POD[1] = strong; edge = soft |

1) POD = Pin Out Driver

### 3.2.3 Digital to Analog Converters (DACx)

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 27 DAC Parameters** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| RMS supply current | $I_{DD}$ | CC | – | 2.5 | 4 | mA | per active DAC channel, without load currents of DAC outputs |
| Resolution | $RES$ | CC | – | 12 | – | Bit | |
| Update rate | $f_{URATE\_A}$ | CC | – | | 2 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy |
| Update rate | $f_{URATE\_F}$ | CC | – | | 5 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy |
| Settling time | $t_{SETTLE}$ | CC | – | 1 | 2 | µs | at full scale jump, output voltage reaches target value ± 20 LSB |
| Slew rate | $SR$ | CC | 2 | 5 | – | V/µs | |
| Minimum output voltage | $V_{OUT\_MIN}$ | CC | – | 0.3 | – | V | code value unsigned: $000_H$; signed: $800_H$ |
| Maximum output voltage | $V_{OUT\_MAX}$ | CC | – | 2.5 | – | V | code value unsigned: $FFF_H$; signed: $7FF_H$ |
| Integral non-linearity[1)] | $INL$ | CC | -5.5 | ±2.5 | 5.5 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |
| Differential non-linearity | $DNL$ | CC | -2 | ±1 | 2 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |

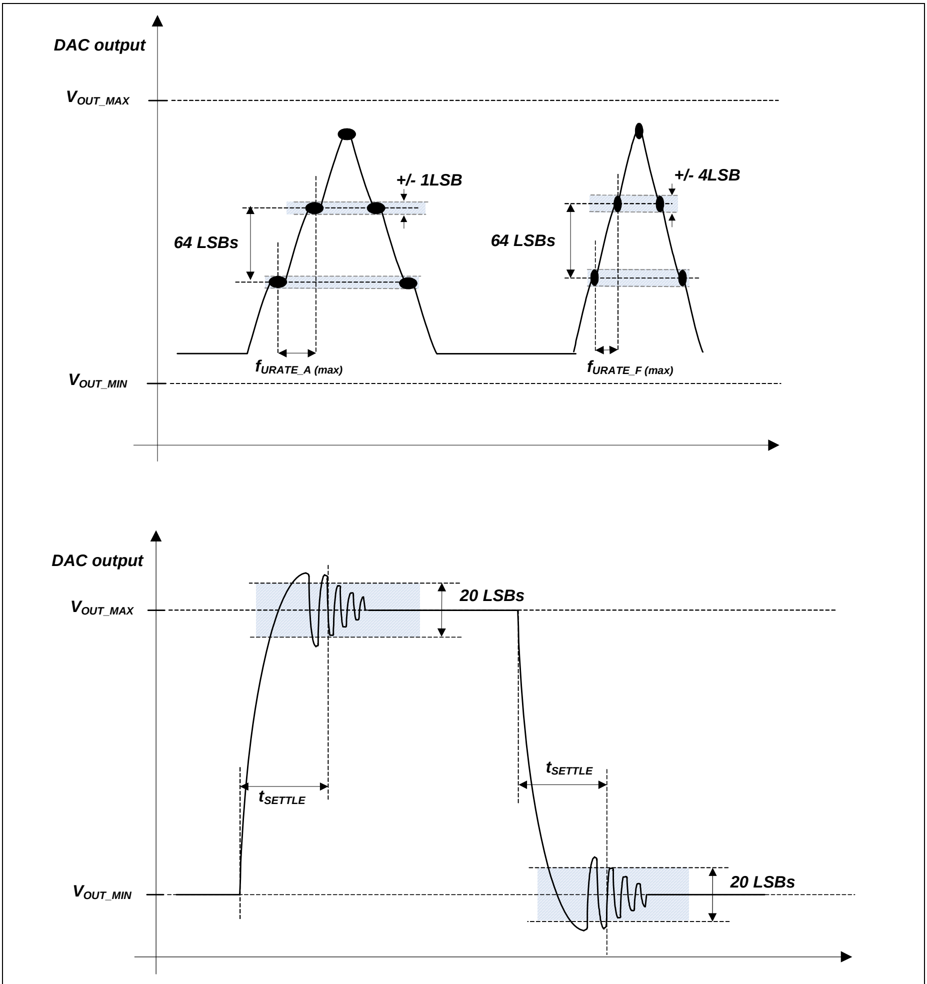


**Figure 15 DAC Conversion Examples**

### 3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages ($V_{AIN}$) above the analog reference[1)] ($V_{AREF}$) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA}$ + 50 mV.

**Table 28 ORC Parameters** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{ODC}$ | CC | 100 | 125 | 200 | mV | $V_{AIN} \geq V_{AREF} + V_{ODC}$ |
| Hysteresis | $V_{OHYS}$ | CC | 50 | – | $V_{ODC}$ | mV | |
| Detection Delay of a persistent Overvoltage | $t_{ODD}$ | CC | 55 | – | 450 | ns | $V_{AIN} \geq V_{AREF}$ + 200 mV |
| | | | 45 | – | 105 | ns | $V_{AIN} \geq V_{AREF}$ + 400 mV |
| Always detected Overvoltage Pulse | $t_{OPDD}$ | CC | 440 | – | – | ns | $V_{AIN} \geq V_{AREF}$ + 200 mV |
| | | | 90 | – | – | ns | $V_{AIN} \geq V_{AREF}$ + 400 mV |
| Never detected Overvoltage Pulse | $t_{OPDN}$ | CC | – | – | 49 | ns | $V_{AIN} \geq V_{AREF}$ + 200 mV |
| | | | – | – | 30 | ns | $V_{AIN} \geq V_{AREF}$ + 400 mV |
| Release Delay | $t_{ORD}$ | CC | 65 | – | 105 | ns | $V_{AIN} \leq V_{AREF}$ |
| Enable Delay | $t_{OED}$ | CC | – | 100 | 200 | ns | |

1) Always the standard VADC reference, alternate references do not apply to the ORC.

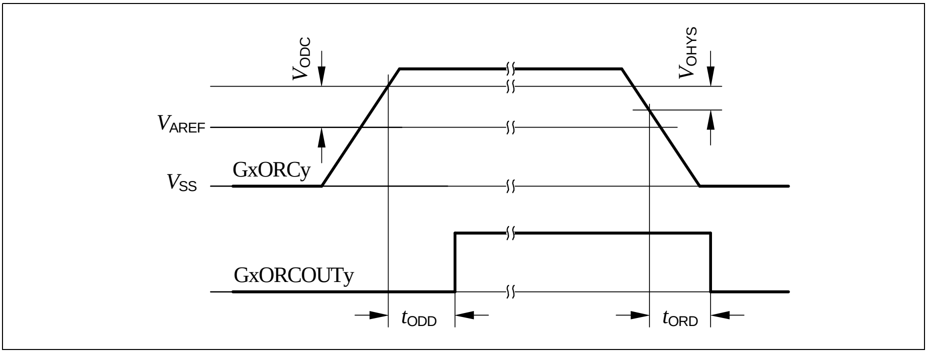


**Figure 16 GxORCOUTy Trigger Generation**

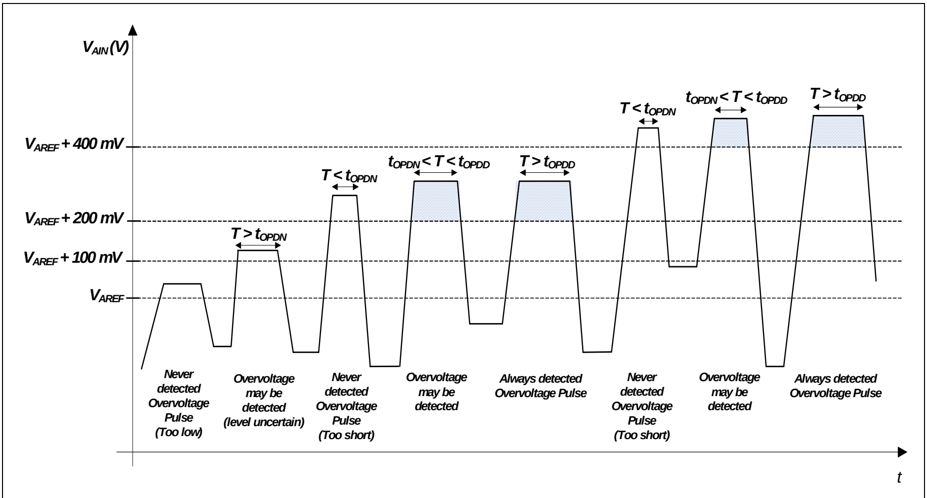


**Figure 17 ORC Detection Ranges**

**Table 30 CMP and 10-bit DAC characteristics** (Operating Conditions apply) (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| CSG Output Jitter | $D_{CSG}$ CC | – | – | 1 | clk | |
| Bias startup time | $t_{start}$ CC | – | – | 98 | us | |
| Bias supply current | $I_{DDbias}$ CC | – | – | 400 | µA | |
| CSGy startup time | $t_{CSGS}$ CC | – | – | 2 | µs | |
| Input operation current[1] | $I_{DDCIN}$ CC | -10 | – | 33 | µA | See **Figure 19** |
| High Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | $V_{SS}$ | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full scale | $t_{FShs}$ CC | – | – | 80 | ns | See **Figure 20** |
| Input Selector propagation delay - Full scale | $t_{Dhs}$ CC | – | – | 100 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dhs}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDhs}$ CC | – | – | 940 | µA | |
| Low Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | $0.1 \times V_{DDP}$[2] | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full Scale | $t_{FSls}$ CC | – | – | 160 | ns | See **Figure 20** |
| Input Selector propagation delay - Full Scale | $t_{Dls}$ CC | – | – | 200 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dls}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDls}$ CC | – | – | 300 | µA | |

1) Typical input resistance $R_{CIN}$ = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

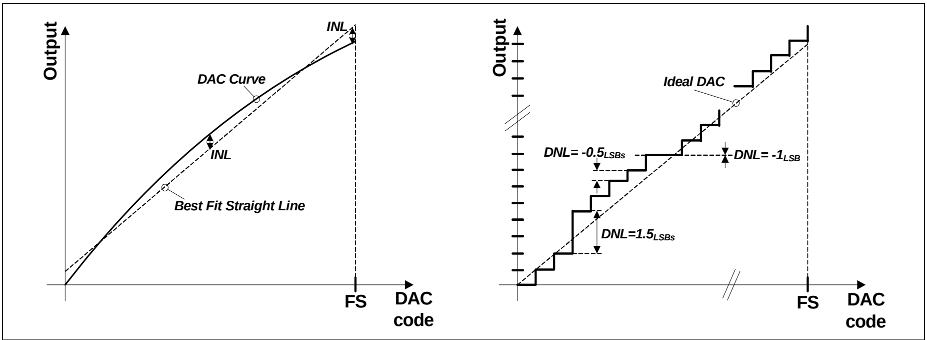


**Figure 18 CSG DAC INL and DNL example**

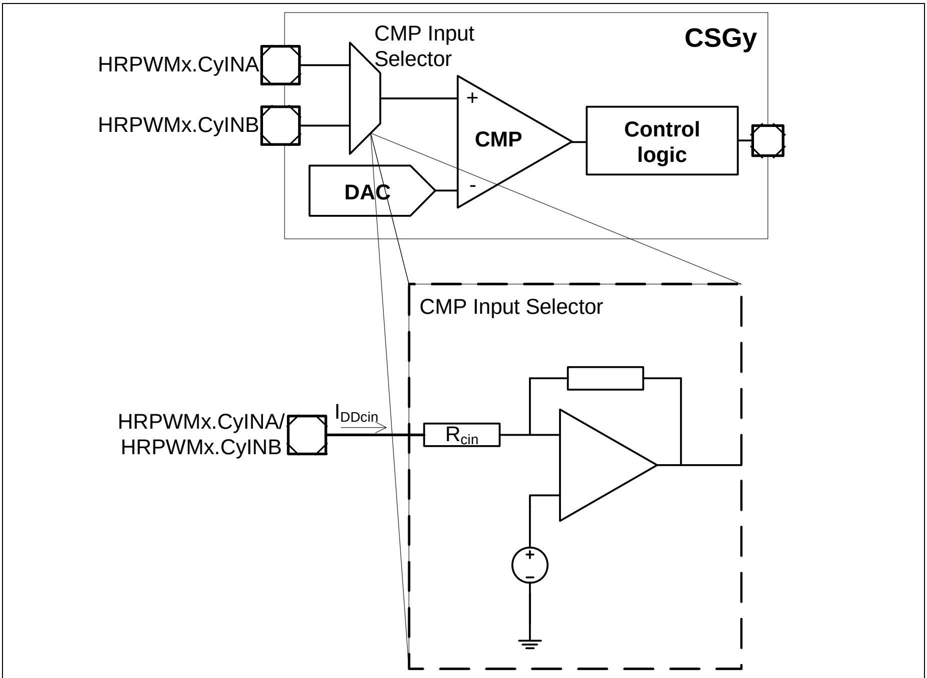


**Figure 19 Input operation current**

**Table 32 External clock operating conditions**

| Parameter | Symbol | | Values | | | Unit | Note / Test Con dition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Frequency | $f_{eclk}$ | SR | – | – | $f_{hrpwm}/4$ | MHz | |
| ON time | $t_{oneclk}$ | SR | $2T_{ccu}$ [1)2)] | – | – | ns | |
| OFF time | $t_{offeclk}$ | SR | $2T_{ccu}$ [1)2)] | – | – | ns | Only the rising edge is used |

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

### 3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing $V_{BAT}$ or another external sensor voltage $V_{LPS}$ with a pre-programmed threshold voltage.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 33 Low Power Analog Comparator Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| $V_{BAT}$ supply voltage range for LPAC operation | $V_{BAT}$ | SR | 2.1 | – | 3.6 | V | |
| Sensor voltage range | $V_{LPCS}$ | CC | 0 | – | 1.2 | V | |
| Threshold step size | $V_{th}$ | CC | – | 18.75 | – | mV | |
| Threshold trigger accuracy | $\Delta V_{th}$ | CC | – | – | ±10 | % | for $V_{th}$ > 0.4 V |
| Conversion time | $t_{LPCC}$ | CC | – | – | 250 | µs | |
| Average current consumption over time | $I_{LPCAC}$ | CC | – | – | 15 | µA | conversion interval 10 ms[1)] |
| Current consumption during conversion | $I_{LPCC}$ | CC | – | 150 | – | µA | [1)] |

1) Single channel conversion, measuring $V_{BAT}$ = 3.3 V, 8 cycles settling time

**Table 38 RTC_XTAL Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input frequency | $f_{OSC}$ SR | – | 32.768 | – | kHz | |
| Oscillator start-up time[1)2)3)] | $t_{OSCS}$ CC | – | – | 5 | s | |
| Input voltage at RTC_XTAL1 | $V_{IX}$ SR | -0.3 | – | $V_{BAT}$ + 0.3 | V | |
| Input amplitude (peak-to-peak) at RTC_XTAL1[2)4)] | $V_{PPX}$ SR | 0.4 | – | – | V | |
| Input high voltage at RTC_XTAL1[5)] | $V_{IHBX}$ SR | 0.6 × $V_{BAT}$ | – | $V_{BAT}$ + 0.3 | V | |
| Input low voltage at RTC_XTAL1[5)] | $V_{ILBX}$ SR | -0.3 | – | 0.36 × $V_{BAT}$ | V | |
| Input Hysteresis for RTC_XTAL1[5)6)] | $V_{HYSX}$ CC | 0.1 × $V_{BAT}$ | | – | V | 3.0 V ≤ $V_{BAT}$ < 3.6 V |
| | | 0.03 × $V_{BAT}$ | | – | V | $V_{BAT}$ < 3.0 V |
| Input leakage current at RTC_XTAL1 | $I_{ILX1}$ CC | -100 | – | 100 | nA | Oscillator power down 0 V ≤ $V_{IX}$ ≤ $V_{BAT}$ |

1) $t_{OSCS}$ is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0$ V. A running oscillation is maintained across the full $V_{BAT}$ voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

### 3.3.5 Internal Clock Source Characteristics

#### Fast Internal Clock Source

**Table 45 Fast Internal Clock Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{OFINC}$ CC | – | 36.5 | – | MHz | not calibrated |
| | | – | 24 | – | MHz | calibrated |
| Accuracy | $\Delta f_{OFI}$ CC | -0.5 | – | 0.5 | % | automatic calibration[1)2)] |
| | | -15 | – | 15 | % | factory calibration, $V_{DDP}$ = 3.3 V |
| | | -25 | – | 25 | % | no calibration, $V_{DDP}$ = 3.3 V |
| | | -7 | – | 7 | % | Variation over voltage range[3)] 3.13 V ≤ $V_{DDP}$ ≤ 3.63 V |
| Start-up time | $t_{OFIS}$ CC | – | 50 | – | µs | |

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the $V_{DDP}$ supply voltage.

3) Deviations from the nominal $V_{DDP}$ voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

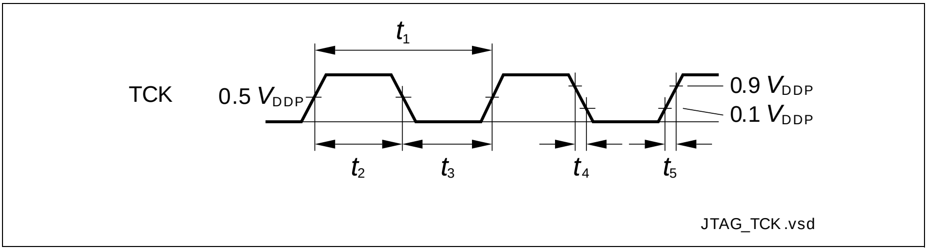


**Figure 28 Test Clock Timing (TCK)**

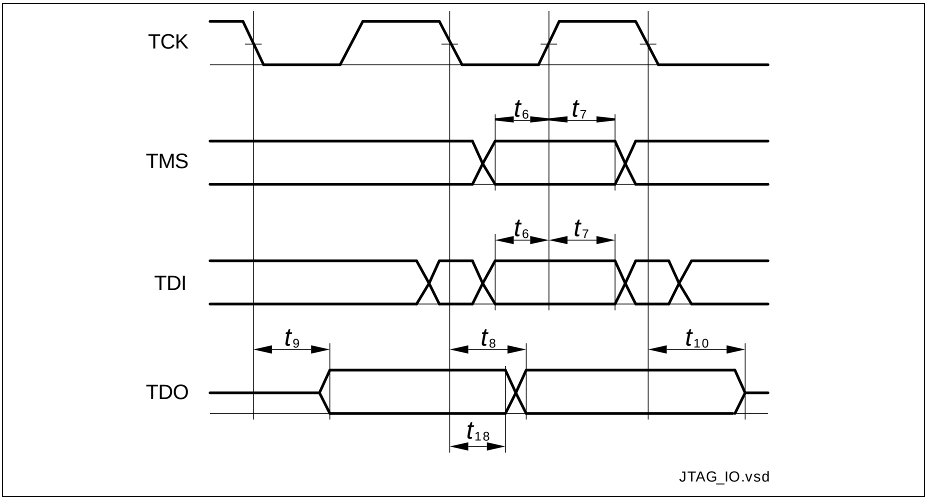


**Figure 29 JTAG Timing**

### 3.3.9 Peripheral Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

#### 3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 50 DSD Interface Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| MCLK period in master mode | $t_1$ | CC | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{PERIPH}$ [1)] |
| MCLK high time in master mode | $t_2$ | CC | 9 | – | – | ns | $t_2 > t_{PERIPH}$ [1)] |
| MCLK low time in master mode | $t_3$ | CC | 9 | – | – | ns | $t_3 > t_{PERIPH}$ [1)] |
| MCLK period in slave mode | $t_1$ | SR | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{PERIPH}$ [1)] |
| MCLK high time in slave mode | $t_2$ | SR | $t_{PERIPH}$ | – | – | ns | [1)] |
| MCLK low time in slave mode | $t_3$ | SR | $t_{PERIPH}$ | – | – | ns | [1)] |
| DIN input setup time to the active clock edge | $t_4$ | SR | $t_{PERIPH} + 4$ | – | – | ns | [1)] |
| DIN input hold time from the active clock edge | $t_5$ | SR | $t_{PERIPH} + 3$ | – | – | ns | [1)] |

1) $t_{PERIPH} = 1 / f_{PERIPH}$

### 3.3.11.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

**Table 59 ETH RMII Signal Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| ETH_RMII_REF_CL clock period | $t_{13}$ | SR | 20 | – | – | ns | $C_L$ = 25 pF; 50 ppm |
| ETH_RMII_REF_CL clock high time | $t_{14}$ | SR | 7 | – | 13 | ns | $C_L$ = 25 pF |
| ETH_RMII_REF_CL clock low time | $t_{15}$ | SR | 7 | – | 13 | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time | $t_{16}$ | SR | 4 | – | – | ns | |
| ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time | $t_{17}$ | SR | 2 | – | – | ns | |
| ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid | $t_{18}$ | CC | 4 | – | 15 | ns | |

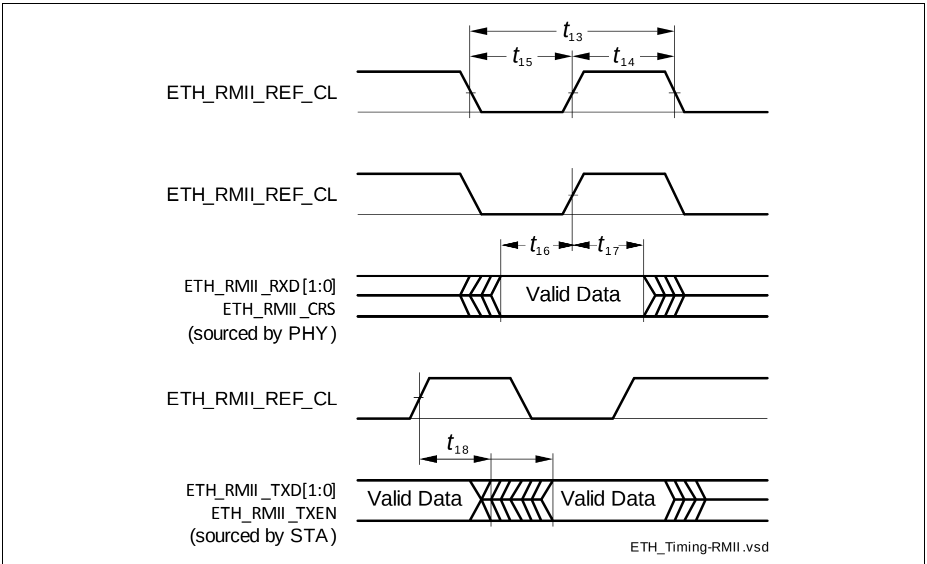


**Figure 41 ETH RMII Signal Timing**

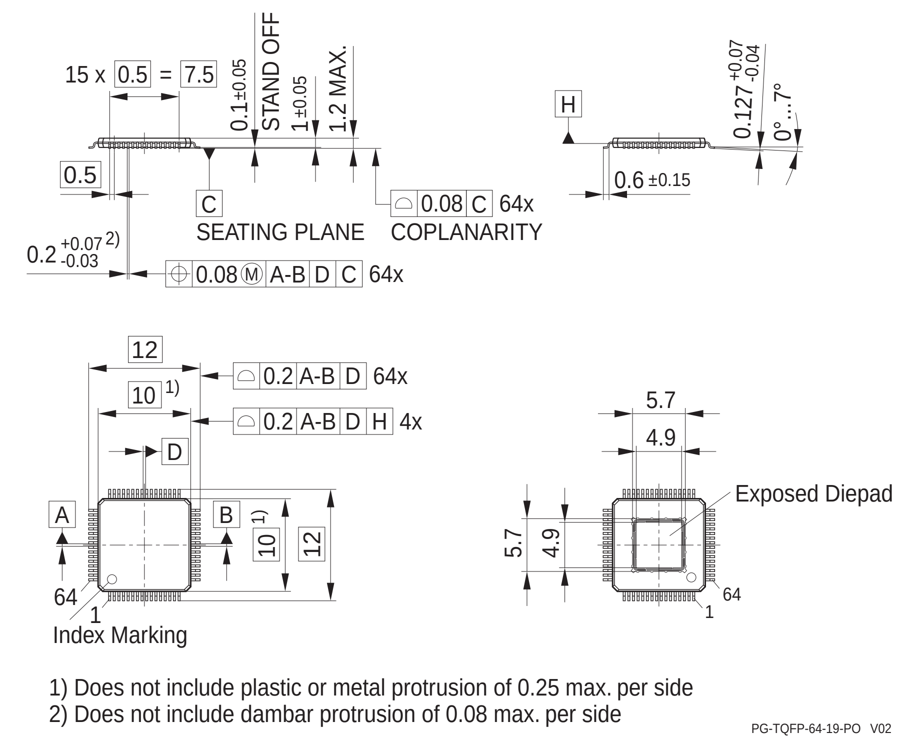


**Figure 45 PG-TQFP-64-19** (Plastic Green Low Profile Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**