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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I <sup>2</sup> S, LED, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/xmc4402f64k256abxqsa1">https://www.e-xfl.com/product-detail/infineon-technologies/xmc4402f64k256abxqsa1</a>

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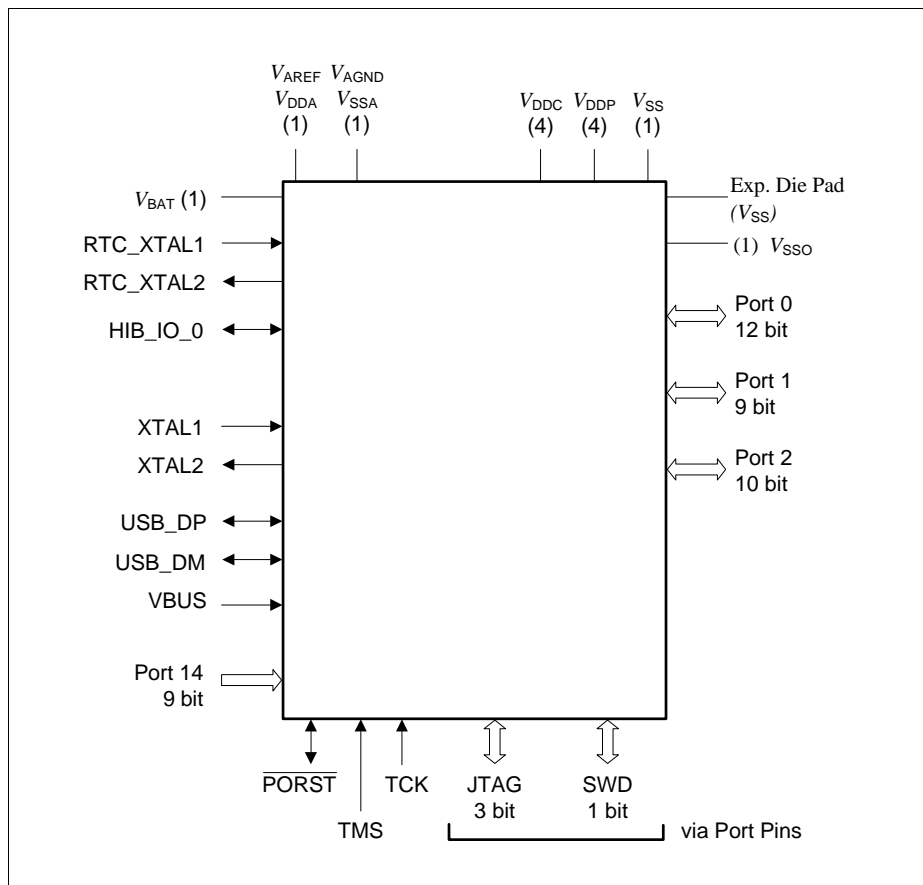
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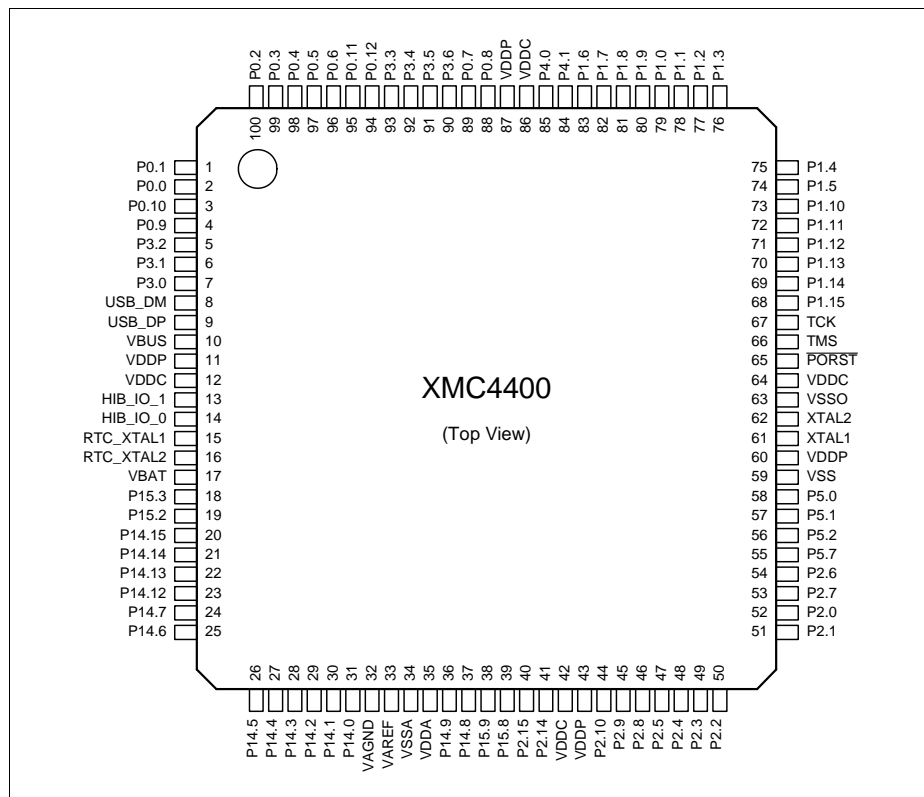
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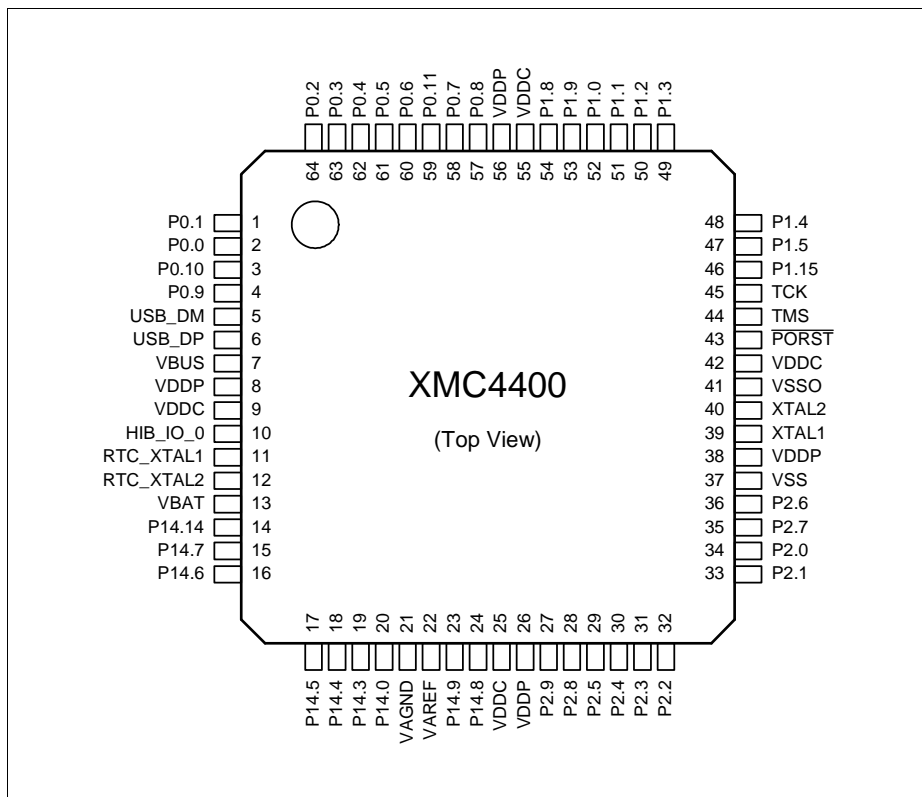
**Figure 3 XMC4400 Logic Symbol PG-LQFP-64 and PG-TQFP-64**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.



**Figure 4 XMC4400 PG-LQFP-100 Pin Configuration (top view)**



**Figure 5 XMC4400 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)**

## 2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

**Table 9 Package Pin Mapping Description**

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG\_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

**Table 10 Package Pin Mapping**

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	100	64	A2	
P0.3	99	63	A2	
P0.4	98	62	A2	
P0.5	97	61	A2	
P0.6	96	60	A2	
P0.7	89	58	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	88	57	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	4	A2	
P0.10	3	3	A1+	

**Table 12 Port I/O Functions (cont'd)**

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P14.9					DAC. OUT_1			VADC. G1CH1		VADC. G3CH3	ETH0. RXD1C			
P14.12								VADC. G1CH4						
P14.13								VADC. G1CH5						
P14.14								VADC. G1CH6					G1ORC6	
P14.15								VADC. G1CH7					G1ORC7	
P15.2									VADC. G2CH2					
P15.3									VADC. G2CH3					
P15.8										VADC. G3CH0	ETH0. CLK_RMII			ETH0. CLK_RXC
P15.9										VADC. G3CH1	ETH0. CRS_DVC			ETH0. RXDVC
USB_DP														
USB_DM														
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT					WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT					WAKEUPB							
TCK						DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO									
PORST														
XTAL1							U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F				
XTAL2														
RTC_XTAL1									ERU0. 1B1					
RTC_XTAL2														

The XMC4400 has a common ground concept, all  $V_{SS}$ ,  $V_{SSA}$  and  $V_{SSO}$  pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

$V_{AGND}$  is the low potential to the analog reference  $V_{AREF}$ . Depending on the application it can share the common ground or have a different potential. In devices with shared  $V_{DDA}/V_{AREF}$  and  $V_{SSA}/V_{AGND}$  pins the reference is tied to the supply. Some analog channels can optionally serve as "Alternate Reference"; further details on this operating mode are described in the Reference Manual.

When  $V_{DDP}$  is supplied,  $V_{BAT}$  must be supplied as well. If no other supply source (e.g. battery) is connected to  $V_{BAT}$ , the  $V_{BAT}$  pin can also be connected directly to  $V_{DDP}$ .



**Table 21 Standard Pads Class\_A1**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1}$ CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	$V_{IHA1}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1}$ SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD <sup>1)</sup> = weak	$V_{OHA1}$ CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\text{ }\mu\text{A}$
$V_{DDP} - 0.4$		–	V	$I_{OH} \geq -1.4\text{ mA}$	
2.4		–	V	$I_{OH} \geq -2\text{ mA}$	
Output low voltage	$V_{OLA1}$ CC	–	0.4	V	$I_{OL} \leq 500\text{ }\mu\text{A}$ ; POD <sup>1)</sup> = weak
		–	0.4	V	$I_{OL} \leq 2\text{ mA}$ ; POD <sup>1)</sup> = medium
Fall time	$t_{FA1}$ CC	–	150	ns	$C_L = 20\text{ pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\text{ pF}$ ; POD <sup>1)</sup> = medium
Rise time	$t_{RA1}$ CC	–	150	ns	$C_L = 20\text{ pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\text{ pF}$ ; POD <sup>1)</sup> = medium

1) POD = Pin Out Driver

**Table 22 Standard Pads Class\_A1+**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1+}$ CC	-1	1	$\mu\text{A}$	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	$V_{IHA1+}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1+}$ SR	-0.3	$0.36 \times V_{DDP}$	V	

**Table 24 HIB\_IO Class\_A1 special Pads**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZHIB}$ CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{BAT}$
Input high voltage	$V_{IHIB}$ SR	$0.6 \times V_{BAT}$	$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILHIB}$ SR	-0.3	$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins <sup>1)</sup>	$HYSHIB$ CC	$0.1 \times V_{BAT}$	–	V	$V_{BAT} \geq 3.13\text{ V}$
		$0.06 \times V_{BAT}$	–	V	$V_{BAT} < 3.13\text{ V}$
Output high voltage, POD <sup>1)</sup> = medium	$V_{OHIB}$ CC	$V_{BAT} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
Output low voltage	$V_{OLHIB}$ CC	–	0.4	V	$I_{OL} \leq 2\text{ mA}$
Fall time	$t_{FHIB}$ CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$
Rise time	$t_{RHIB}$ CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

### 3.2.2 Analog to Digital Converters (ADCx)

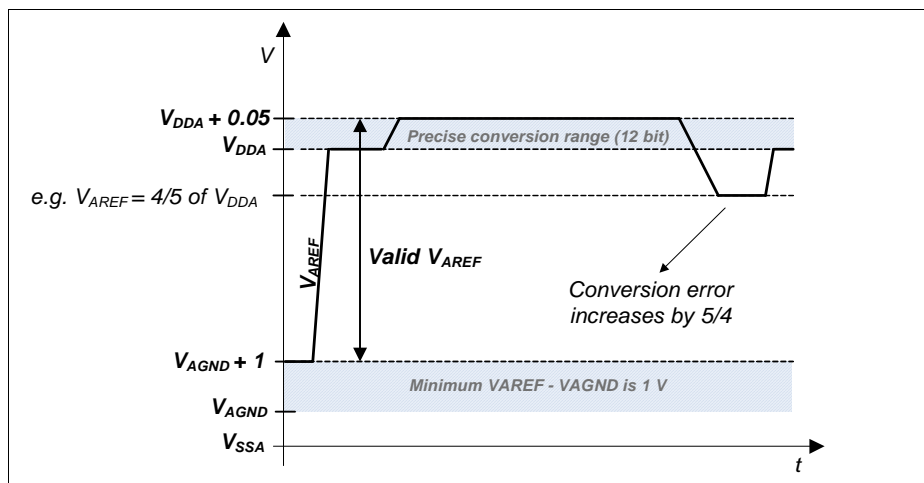
*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 25 ADC Parameters** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage <sup>5)</sup>	$V_{AREF}$ SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05^{1)}$	V	
Analog reference ground <sup>5)</sup>	$V_{AGND}$ SR	$V_{SSM} - 0.05$	–	$V_{AREF} - 1$	V	
Analog reference voltage range <sup>2)5)</sup>	$V_{AREF} - V_{AGND}$ SR	1	–	$V_{DDA} + 0.1$	V	
Analog input voltage	$V_{AIN}$ SR	$V_{AGND}$	–	$V_{DDA}$	V	
Input leakage at analog inputs <sup>3)</sup>	$I_{OZ1}$ CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DD}$ A
		-500	–	100	nA	$0 V \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Input leakage current at VAREF	$I_{OZ2}$ CC	-1	–	1	μA	$0 V \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	$I_{OZ3}$ CC	-1	–	1	μA	$0 V \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	$f_{ADCI}$ CC	2	–	30	MHz	$V_{DDA} = 3.3 V$
Switched capacitance at the analog voltage inputs <sup>4)</sup>	$C_{AINSW}$ CC	–	4	6.5	pF	
Total capacitance of an analog input	$C_{AINTOT}$ CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input <sup>5)6)</sup>	$C_{AREFSW}$ CC	–	15	30	pF	
Total capacitance of the voltage reference inputs <sup>5)</sup>	$C_{AREFTOT}$ CC	–	20	40	pF	

## Electrical Parameters

- 4) The sampling capacity of the conversion C-network is pre-charged to  $V_{AREF}/2$  before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from  $V_{AREF}/2$ .
- 5) Applies to AINx, when used as alternate reference input.
- 6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
- 7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than  $\pm 1$  LSB.
- 8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
- 9) The resulting current for a conversion can be calculated with  $I_{AREF} = Q_{CONV} / t_c$ .  
The fastest 12-bit post-calibrated conversion of  $t_c = 550$  ns results in a typical average current of  $I_{AREF} = 54.5$   $\mu$ A.



**Figure 12 VADC Reference Voltage Range**

**Table 32 External clock operating conditions**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency	$f_{\text{eclk}}$ SR	–	–	$f_{\text{hrpwm}}/4$	MHz	
ON time	$t_{\text{oneclk}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	
OFF time	$t_{\text{offeclk}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

### 3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing  $V_{\text{BAT}}$  or another external sensor voltage  $V_{\text{LPS}}$  with a pre-programmed threshold voltage.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 33 Low Power Analog Comparator Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{\text{BAT}}$ supply voltage range for LPAC operation	$V_{\text{BAT}}$ SR	2.1	–	3.6	V	
Sensor voltage range	$V_{\text{LPCS}}$ CC	0	–	1.2	V	
Threshold step size	$V_{\text{th}}$ CC	–	18.75	–	mV	
Threshold trigger accuracy	$\Delta V_{\text{th}}$ CC	–	–	$\pm 10$	%	for $V_{\text{th}} > 0.4 \text{ V}$
Conversion time	$t_{\text{LPCC}}$ CC	–	–	250	$\mu\text{s}$	
Average current consumption over time	$I_{\text{LPCAC}}$ CC	–	–	15	$\mu\text{A}$	conversion interval 10 ms <sup>1)</sup>
Current consumption during conversion	$I_{\text{LPCC}}$ CC	–	150	–	$\mu\text{A}$	<sup>1)</sup>

1) Single channel conversion, measuring  $V_{\text{BAT}} = 3.3 \text{ V}$ , 8 cycles settling time

### 3.2.8 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 35 USB OTG VBUS and ID Parameters** (Operating Conditions apply)

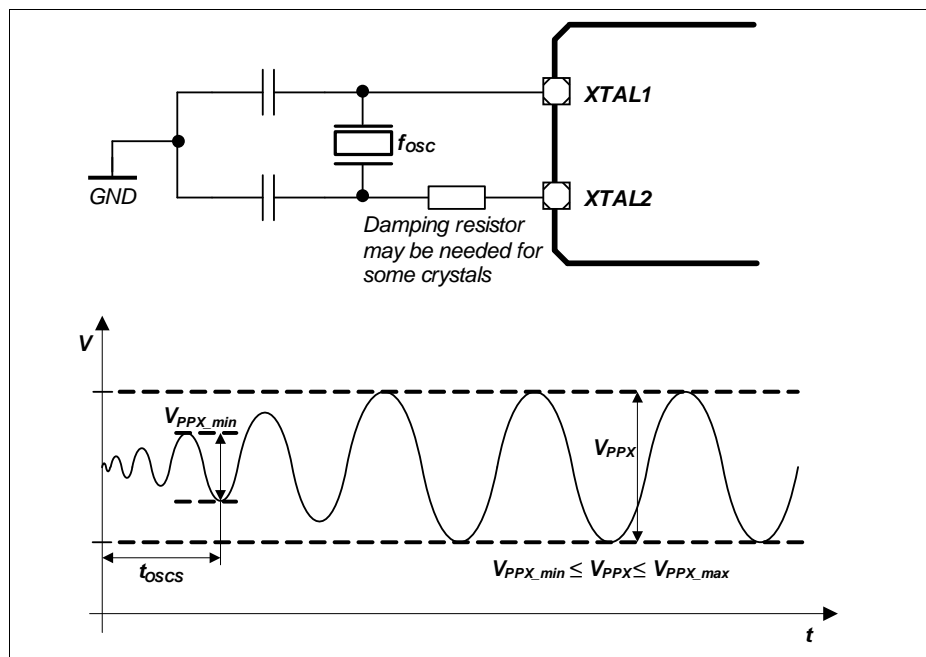
Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
VBUS input voltage range	$V_{IN}$	CC	0.0	—	5.25	V	
A-device VBUS valid threshold	$V_{B1}$	CC	4.4	—	—	V	
A-device session valid threshold	$V_{B2}$	CC	0.8	—	2.0	V	
B-device session valid threshold	$V_{B3}$	CC	0.8	—	4.0	V	
B-device session end threshold	$V_{B4}$	CC	0.2	—	0.8	V	
VBUS input resistance to ground	$R_{VBUS\_IN}$	CC	40	—	100	kOhm	
B-device VBUS pull-up resistor	$R_{VBUS\_PU}$	CC	281	—	—	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	$R_{VBUS\_PD}$	CC	656	—	—	Ohm	
USB.ID pull-up resistor	$R_{UID\_PU}$	CC	14	—	25	kOhm	
VBUS input current	$I_{VBUS\_IN}$	CC	—	—	150	μA	$0\text{ V} \leq V_{IN} \leq 5.25\text{ V}$ : $T_{AVG} = 1\text{ ms}$

### 3.2.9 Oscillator Pins

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal (see [Figure 21](#)) or in direct input mode (see [Figure 22](#)).



**Figure 21 Oscillator in Crystal Mode**

**Table 37 OSC\_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{\text{OSC}}$ SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time <sup>1)2)</sup>	$t_{\text{OSCS}}$ CC	–	–	10	ms	
Input voltage at XTAL1	$V_{\text{IX}}$ SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	
Input amplitude (peak-to-peak) at XTAL1 <sup>2)3)</sup>	$V_{\text{PPX}}$ SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	
Input high voltage at XTAL1 <sup>4)</sup>	$V_{\text{IHBX}}$ SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	
Input low voltage at XTAL1 <sup>4)</sup>	$V_{\text{ILBX}}$ SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	$I_{\text{ILX1}}$ CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

1)  $t_{\text{OSCS}}$  is defined from the moment the oscillator is enabled with SCU\_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of  $0.4 \times V_{\text{DDP}}$ .

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.



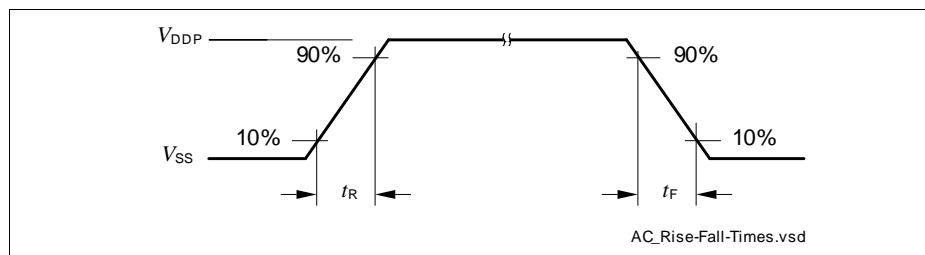
**Table 41 Flash Memory Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB) <sup>3)4)</sup>	$t_{RTU}$ CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	$N_{EPS4}$ CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time <sup>5)</sup>

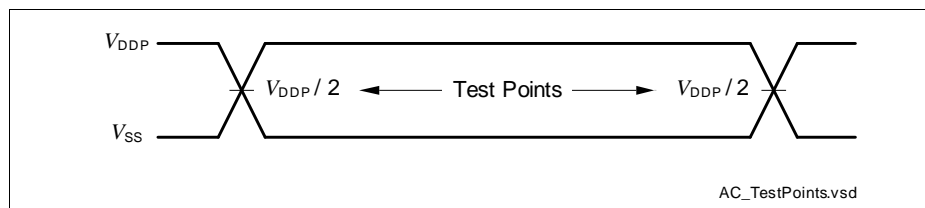
- 1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
- 2) The following formula applies to the wait state configuration:  $FCON.WSPFLASH \times (1 / f_{CPU}) \geq t_a$ .
- 3) Storage and inactive time included.
- 4) Values given are valid for an average weighted junction temperature of  $T_j = 110^\circ\text{C}$ .
- 5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

### 3.3 AC Parameters

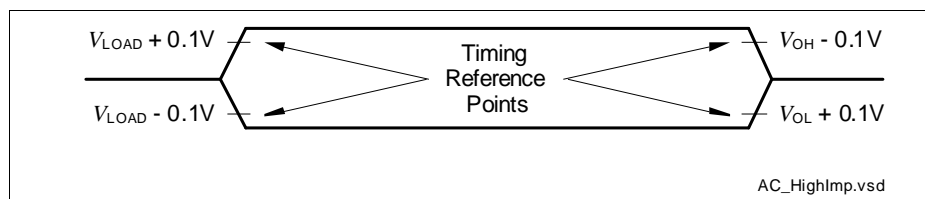
#### 3.3.1 Testing Waveforms



**Figure 23 Rise/Fall Time Parameters**



**Figure 24 Testing Waveform, Output Delay**



**Figure 25 Testing Waveform, Output High Impedance**

### 3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

**Table 47 JTAG Interface Timing Parameters**

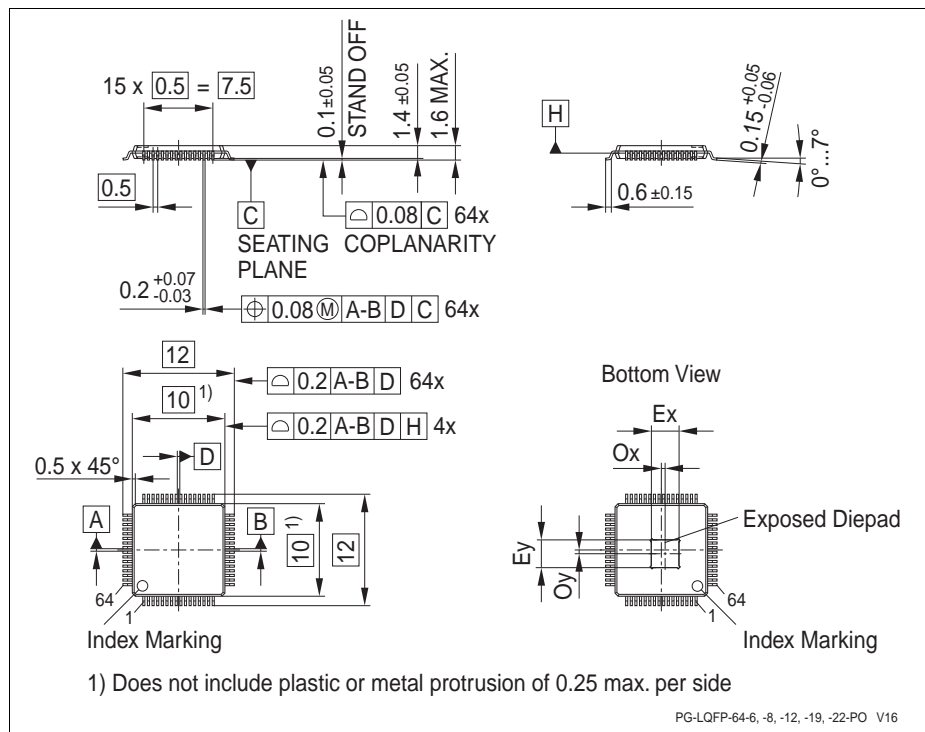
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	$t_1$ SR	25	—	—	ns	
TCK high time	$t_2$ SR	10	—	—	ns	
TCK low time	$t_3$ SR	10	—	—	ns	
TCK clock rise time	$t_4$ SR	—	—	4	ns	
TCK clock fall time	$t_5$ SR	—	—	4	ns	
TDI/TMS setup to TCK rising edge	$t_6$ SR	6	—	—	ns	
TDI/TMS hold after TCK rising edge	$t_7$ SR	6	—	—	ns	
TDO valid after TCK falling edge <sup>1)</sup> (propagation delay)	$t_8$ CC	—	—	13	ns	$C_L = 50$ pF
		3	—	—	ns	$C_L = 20$ pF
TDO hold after TCK falling edge <sup>1)</sup>	$t_{18}$ CC	2	—	—	ns	
TDO high imped. to valid from TCK falling edge <sup>1)2)</sup>	$t_9$ CC	—	—	14	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge <sup>1)</sup>	$t_{10}$ CC	—	—	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

**Table 62 Differences PG-LQFP-64-19 to PG-TQFP-64-19**

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ( $R_{\theta JA}$ )	30.0 K/W	22.5 K/W
Package thickness	1.4 $\pm$ 0.05 mm	1.0 $\pm$ 0.05 mm
	1.6 mm MAX	1.2 mm MAX
Lead Width	0.22 $\pm$ 0.05 mm	0.2 $\pm$ 0.07 $_{-0.03}$ mm
Lead Thickness	0.15 $\pm$ 0.05 $_{-0.06}$ mm	0.127 $\pm$ 0.07 $_{-0.04}$ mm
Exposed Die Pad outer dimensions	5.8 mm $\times$ 5.8 mm	5.7 mm $\times$ 5.7 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	4.9 mm $\times$ 4.9 mm



**Figure 44 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)**

## 5 Quality Declarations

The qualification of the XMC4400 is executed according to the JEDEC standard JESD47H.

*Note: For automotive applications refer to the Infineon automotive microcontrollers.*

**Table 63 Quality Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	$t_{OP}$ CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$ , device permanent on
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM}$ SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM}$ SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	$MSL$ CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	$T_{SDR}$ SR	–	–	260	$^\circ\text{C}$	Profile according to JEDEC J-STD-020D