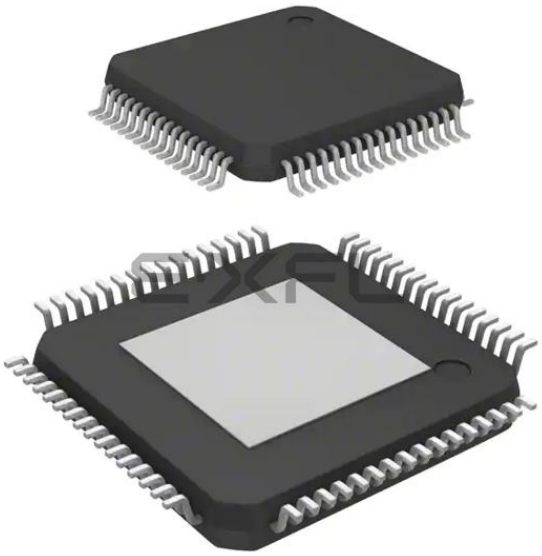
Infineon Technologies - XMC4402F64K256BAXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4402f64k256baxqma1

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2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

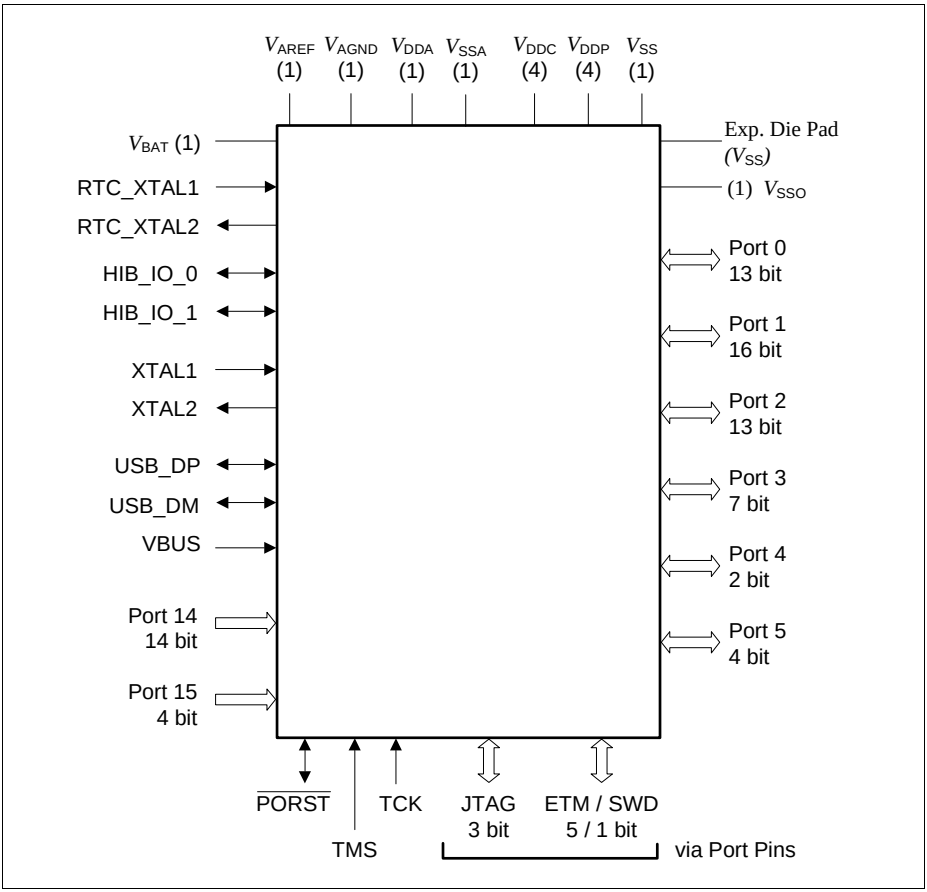

Figure 2 XMC4400 Logic Symbol PG-LQFP-100

Table 10 Package Pin Mapping (cont'd)

Function	LQFP-100	LQFP-64 TQFP-64	Pad Type	Notes
USB_DP	9	6	special	
USB_DM	8	5	special	
HIB_IO_0	14	10	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	13	-	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	67	45	A1	Weak pull-down active.
TMS	66	44	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	65	43	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	61	39	clock_IN	
XTAL2	62	40	clock_O	
RTC_XTAL1	15	11	clock_IN	
RTC_XTAL2	16	12	clock_O	
VBAT	17	13	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	10	7	special	
VAREF	33	-	AN_Ref	
VAGND	32	-	AN_Ref	
VDDA	35	-	AN_Power	

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2			U1C1. DX0D	ETH0. CLK_RMIIB	ERU0. 0B0			HRPWM0. C1INB		ETH0. CLKRXB
P0.1	USB. DRIVEVBUS	U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3				ETH0. CRS_DVB	ERU0. 0A0			HRPWM0. C2INB		ETH0. RXDVB
P0.2		U1C1. SELO1	CCU80. OUT01	HRPWM0. HROUT01	U1C0. DOUT3	U1C0. HWIN3	ETH0. RXD0B		ERU0. 3B3					
P0.3			CCU80. OUT20	HRPWM0. HROUT20	U1C0. DOUT2	U1C0. HWIN2	ETH0. RXD1B			ERU1. 3B0				
P0.4	ETH0. TX_EN		CCU80. OUT10	HRPWM0. HROUT21	U1C0. DOUT1	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3					
P0.5	ETH0. TXD0	U1C0. DOUT0	CCU80. OUT00	HRPWM0. HROUT00	U1C0. DOUT0	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0				
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30	HRPWM0. HROUT30				U1C0. DX2A	ERU0. 3B2		CCU80. IN2B			
P0.7	WWDT. SERVICE_OUT	U0C0. SELO0		HRPWM0. HROUT11		DB. TDI	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT		HRPWM0. HROUT10		$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1		CCU80. IN1B			
P0.9	HRPWM0. HROUT31	U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0	ETH0. MDO	ETH0. MDIA	U1C1. DX2A	USB. ID	ERU0. 1B0					
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1			U1C1. DX1A		ERU0. 1A0					
P0.11		U1C0. SCLKOUT	CCU80. OUT31				ETH0. RXERB	U1C0. DX1A	ERU0. 3A2					
P0.12		U1C1. SELO0	CCU40. OUT3					U1C1. DX2B	ERU0. 2B2					
P1.0	DSD. CGPWMN	U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3			U0C0. DX2A		ERU0. 3B0		CCU40. IN3A	HRPWM0. C0INA		
P1.1	DSD. CGPWMP	U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2			U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0		CCU40. IN2A	HRPWM0. C1INA		
P1.2			CCU40. OUT1	ERU1. PDOUT1	U0C0. DOUT3	U0C0. HWIN3		POSIF0. IN1A		ERU1. 2B0	CCU40. IN1A	HRPWM0. C2INA		
P1.3		U0C0. MCLKOUT	CCU40. OUT0	ERU1. PDOUT0	U0C0. DOUT2	U0C0. HWIN2		POSIF0. IN0A		ERU1. 2A0	CCU40. IN0A	HRPWM0. C0INB		
P1.4	WWDT. SERVICE_OUT	CAN. N0_TXD	CCU80. OUT33	CCU81. OUT20	U0C0. DOUT1	U0C0. HWIN1	U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0		CCU41. IN0C	HRPWM0. BL0A		
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0	U0C0. HWIN0	U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		
P1.6		U0C0. SCLKOUT					DSD. DIN2A							

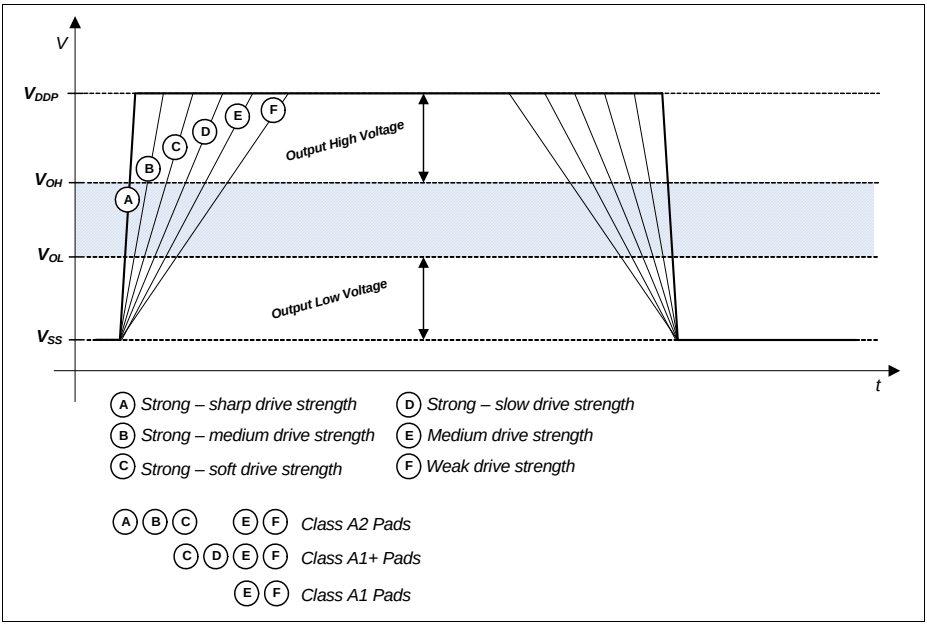

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ CC	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ SR	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (ADCx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \le V_{AREF} \le V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \le V_{AGND} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 550 ns results in a typical average current of I_{AREF} = 54.5 µA.

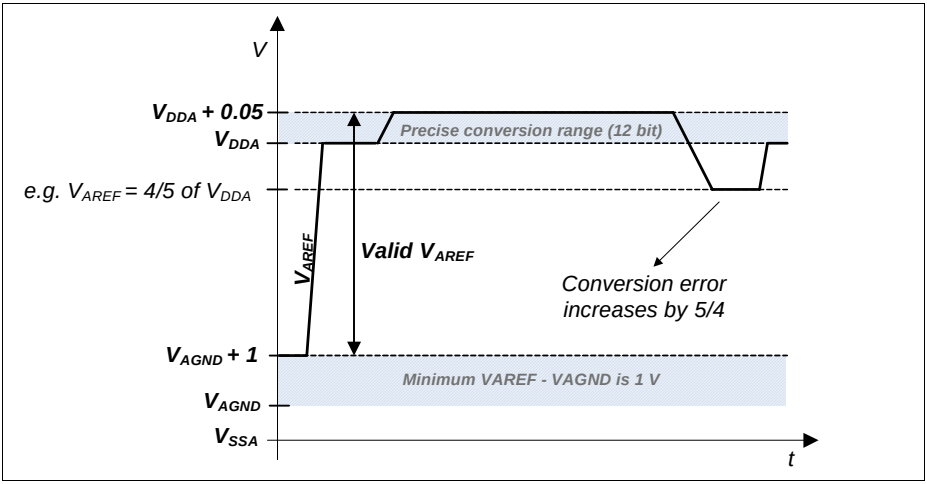

Figure 12 VADC Reference Voltage Range

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC}$ + (2 + N + STC + PC +DM) × T_{ADCI}	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 120 MHz i.e. t_{ADC} = 8.33 ns, DIVA = 3, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.3 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3$ ns $+ 2 \times 8.33$ ns = 550 ns

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3$ ns $+ 2 \times 8.33$ ns = 483 ns

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3$ ns $+ 2 \times 8.33$ ns = 417 ns

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3$ ns $+ 2 \times 8.33$ ns = 350 ns

2) The INL error increases for DAC output voltages below this limit.

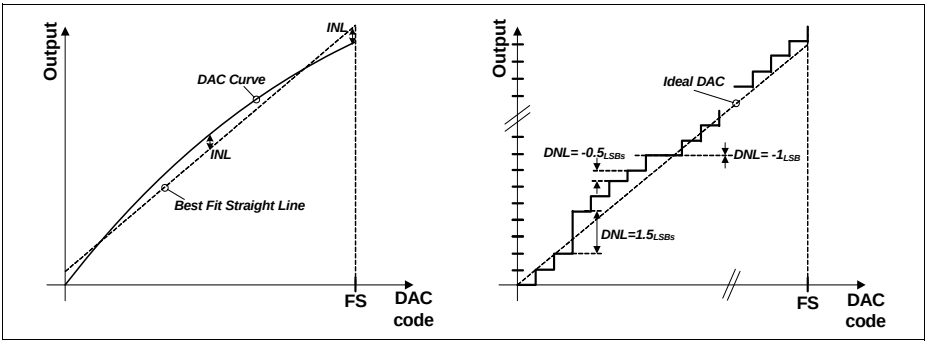

Figure 18 CSG DAC INL and DNL example

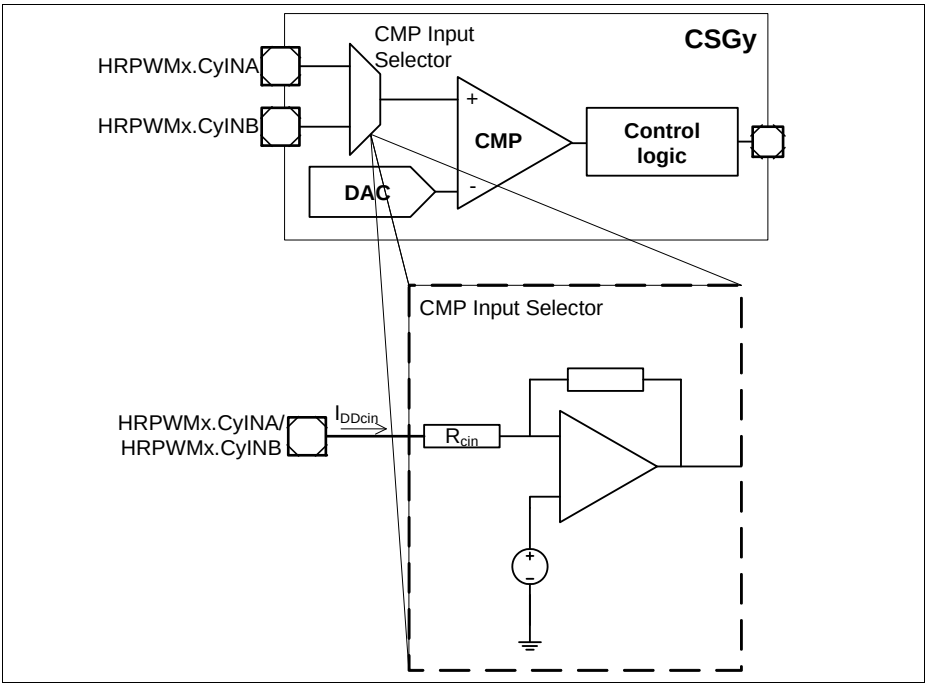

Figure 19 Input operation current

3.2.8 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

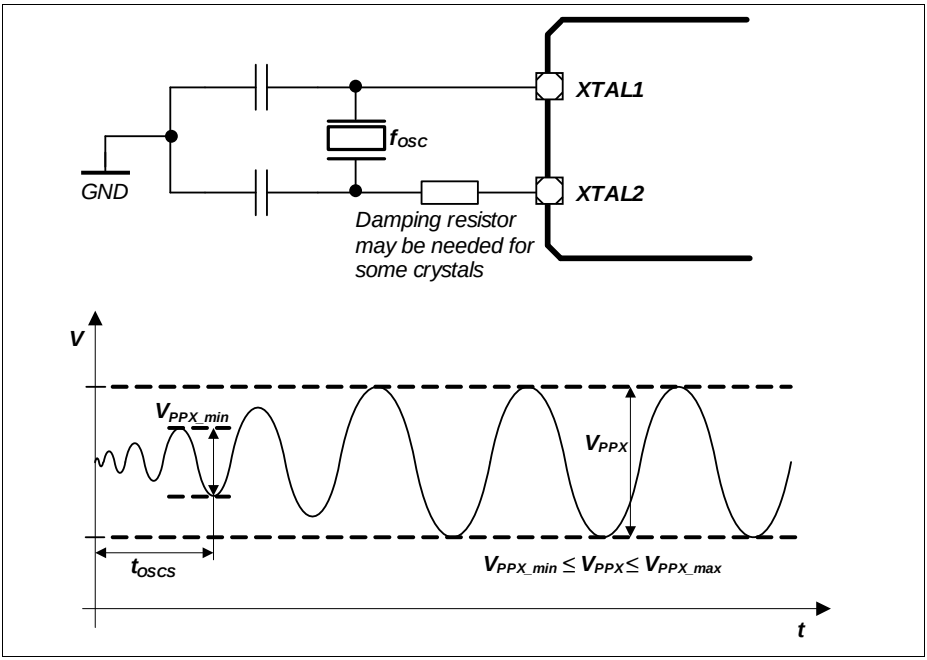

Figure 21 Oscillator in Crystal Mode

Table 37 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2)3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX}SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{DDP}

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Table 38 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)3)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	V_{BAT} + 0.3	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)4)]	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1[5)]	V_{IHBX}SR	0.6 × V_{BAT}	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1[5)]	V_{ILBX} SR	-0.3	–	0.36 × V_{BAT}	V	
Input Hysteresis for RTC_XTAL1[5)6)]	V_{HYSX} CC	0.1 × V_{BAT}		–	V	3.0 V ≤ V_{BAT} < 3.6 V
		0.03 × V_{BAT}		–	V	V_{BAT} < 3.0 V
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{BAT}

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0$ V. A running oscillation is maintained across the full V_{BAT} voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 39 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Dissipation	P_{DISS}	CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode			–	–	–	ms	Defined by the wake-up of the Flash module, see **Section 3.2.11**
Wake-up time from Hibernate mode			–	–	–	ms	Wake-up via power-on reset event, see **Section 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. Ethernet, USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: f_{SYS} = 120 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
   The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) I_{DDP} decreases typically by 5 mA when f_{SYS} decreases by 10 MHz, at constant T_J
11) Sum of currents of all active converters (ADC and DAC)

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.

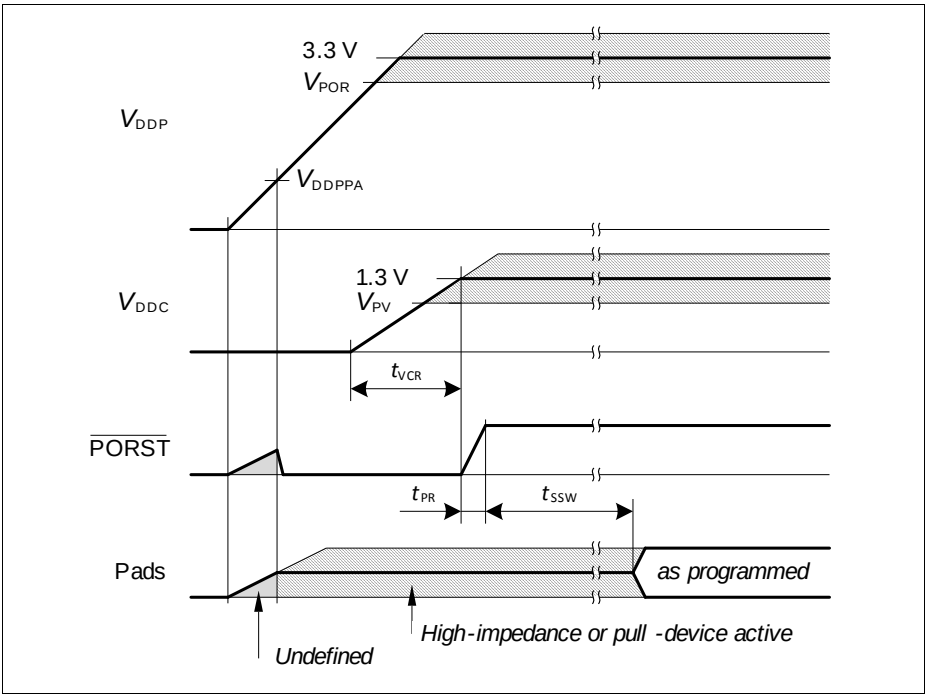

Figure 27 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Slow Internal Clock Source

Table 46 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	25	–	–	ns	
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	13	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.11.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 59 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

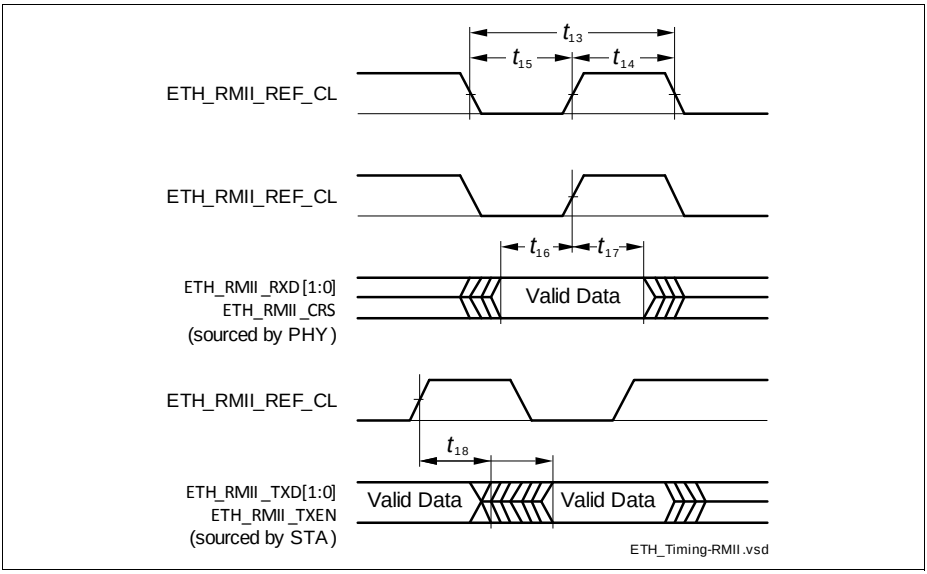

Figure 41 ETH RMII Signal Timing

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**, specific packages for different device markings are listed in **Table 2**.

The exposed die pad dimensions are listed in **Table 60**.

Table 61 Differences PG-LQFP-100-11 to PG-LQFP-100-24

Change	PG-LQFP-100-11	PG-LQFP-100-25
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	20.5 K/W	20.0 K/W
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.073}_{-0.037}$ mm
Exposed Die Pad outer dimensions	7.0 mm × 7.0 mm	7.0 mm × 7.0 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	6.2 mm × 6.2 mm