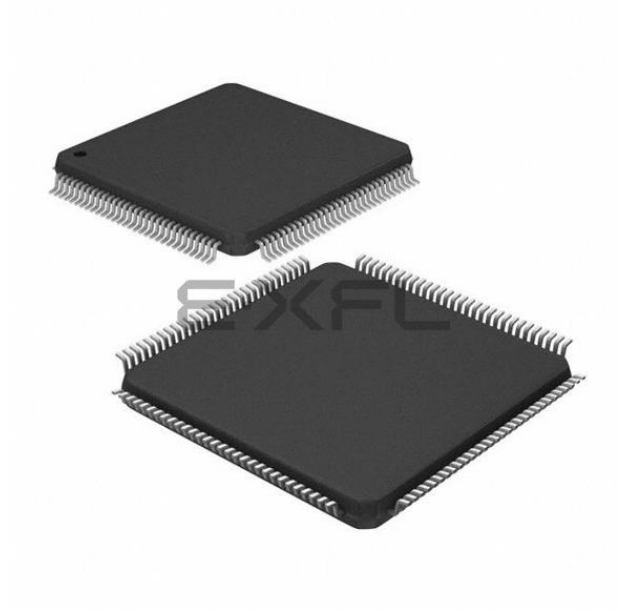

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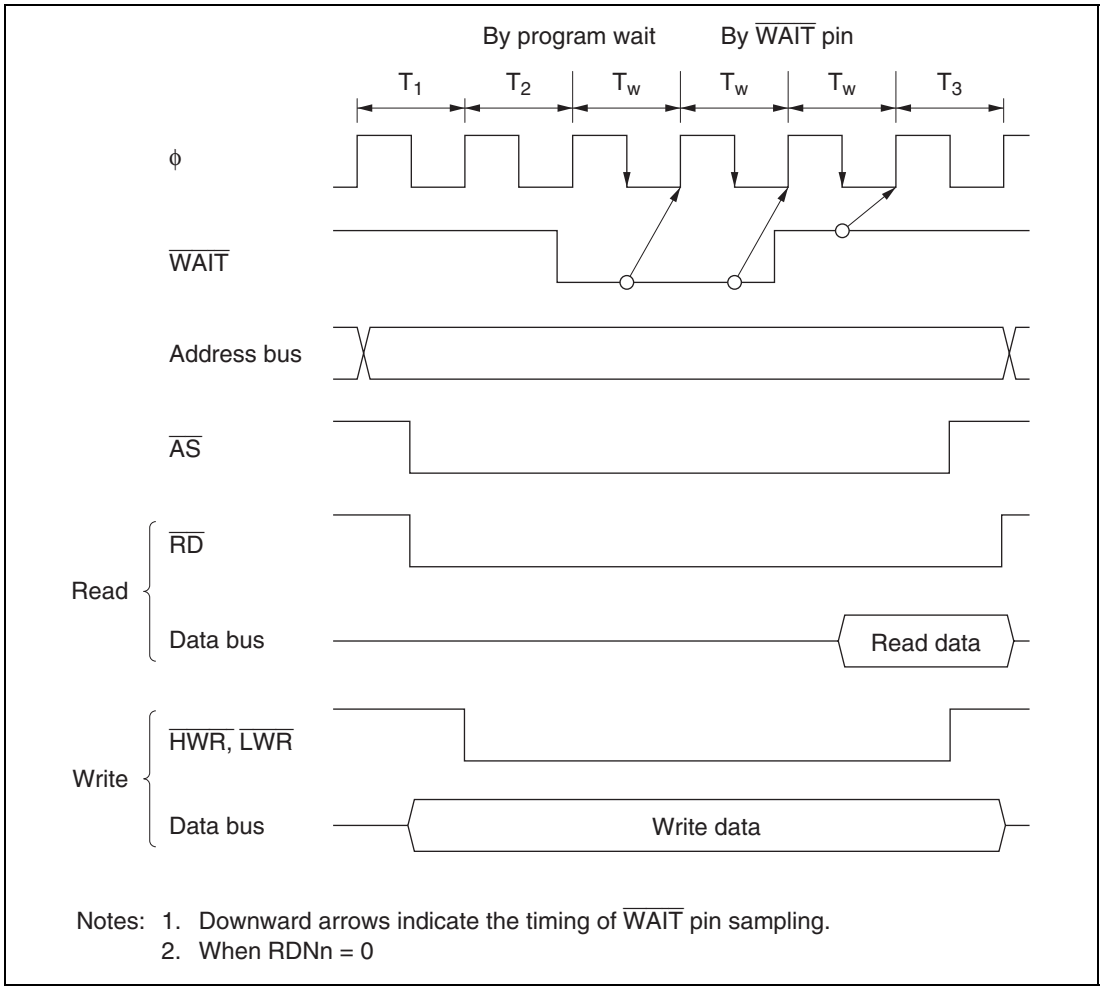


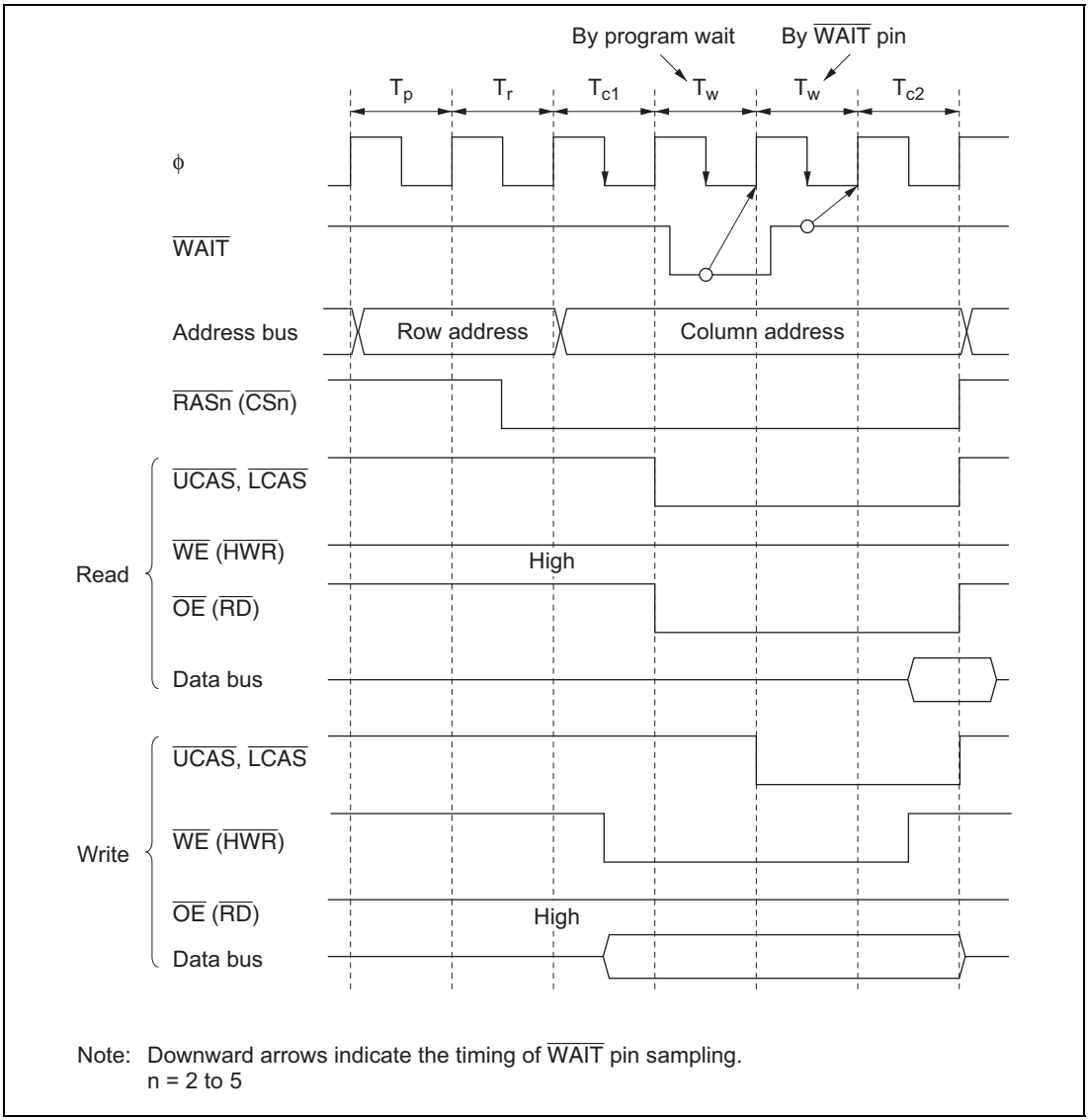
Notes: 1. Downward arrows indicate the timing of $\overline{WAIT}$ pin sampling.
2. When RDNn = 0

Figure 6.18 Example of Wait State Insertion Timing

6.5.5 Read Strobe ($\overline{RD}$) Timing

The read strobe ($\overline{RD}$) timing can be changed for individual areas by setting bits RDN7 to RDN0 to 1 in RDNCR. Figure 6.19 shows an example of the timing when the read strobe timing is changed in basic bus 3-state access space.

When the DMAC or EXDMAC is used in single address mode, note that if the $\overline{RD}$ timing is changed by setting RDNn to 1, the $\overline{RD}$ timing will change relative to the rise of $\overline{DACK}$ or $\overline{EDACK}$.



Note: Downward arrows indicate the timing of WAIT pin sampling.
n = 2 to 5

Figure 6.38 Example of Wait State Insertion Timing (2-State Column Address Output)

6.8.12 Burst Operation

With synchronous DRAM, in addition to full access (normal access) in which data is accessed by outputting a row address for each access, burst access is also provided which can be used when making consecutive accesses to the same row address. This access enables fast access of data by simply changing the column address after the row address has been output. Burst access can be selected by setting the BE bit to 1 in DRAMCR.

DQM has the 2-cycle latency when synchronous DRAM is read. Therefore, the DQM signal cannot be specified to the Tc2 cycle data output if the Tc1 cycle is executed for second or following column address when the CAS latency is set to 1 to issue the READ command. Do not set the BE bit to 1 when synchronous DRAM of CAS latency 1 is connected.

(1) Burst Access Operation Timing

Figure 6.64 shows the operation timing for burst access. When there are consecutive access cycles for continuous synchronous DRAM space, the column address output cycles continue as long as the row address is the same for consecutive access cycles. The row address used for the comparison is set with bits MXC2 to MXC0 in DRAMCR.

6.10.2 Pin States in Idle Cycle

Table 6.13 shows the pin states in an idle cycle.

Table 6.13 Pin States in Idle Cycle

Pins	Pin State
A23 to A0	Contents of following bus cycle
D15 to D0	High impedance
$\overline{CSn}$ (n = 7 to 0)	High*1 *2
$\overline{UCAS}$, $\overline{LCAS}$	High*2
$\overline{AS}$/$\overline{AH}$	High
$\overline{RD}$	High
$\overline{OE}$	High
$\overline{HWR}$, $\overline{LWR}$	High
$\overline{DACKn}$ (n = 1, 0)	High
$\overline{EDACKn}$ (n = 3 to 0)	High

Notes: 1. Remains low in DRAM space RAS down mode.
2. Remains low in a DRAM space refresh cycle.

6.15 Usage Notes

6.15.1 External Bus Release Function and All-Module-Clocks-Stopped Mode

In this LSI, if the ACSE bit is set to 1 in MSTPCR, and then a SLEEP instruction is executed with the setting for all peripheral module clocks to be stopped (MSTPCR = H'FFFF, EXMSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE, EXMSTPCR = H'FFFF), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered in which the clock is also stopped for the bus controller and I/O ports. In this state, the external bus release function is halted. To use the external bus release function in sleep mode, the ACSE bit in MSTPCR must be cleared to 0. Conversely, if a SLEEP instruction to place the chip in all-module-clocks-stopped mode is executed in the external bus released state, the transition to all-module-clocks-stopped mode is deferred and performed until after the bus is recovered.

6.15.2 External Bus Release Function and Software Standby

In this LSI, internal bus master operation does not stop even while the bus is released, as long as the program is running in on-chip ROM, etc., and no external access occurs. If a SLEEP instruction to place the chip in software standby mode is executed while the external bus is released, the transition to software standby mode is deferred and performed after the bus is recovered.

Also, since clock oscillation halts in software standby mode, if $\overline{\text{BREQ}}$ goes low in this mode, indicating an external bus release request, the request cannot be answered until the chip has recovered from the software standby state.

6.15.3 External Bus Release Function and CBR Refreshing/Auto Refreshing

CBR refreshing*[1]/auto refreshing*[2] cannot be executed while the external bus is released. Setting the BREQOE bit to 1 in BCR beforehand enables the $\overline{\text{BREQO}}$ signal to be output when a CBR refresh*[1]/auto refresh*[2] request is issued.

Notes: 1. The auto refresh control function is not supported by the H8S/2426 Group and H8S/2424 Group.
2. The CBR refreshing control is not supported by the 5-V version.

Bit	Bit Name	Initial Value	R/W	Description
7	DAT1	0	R/W	Destination Address Update Mode
6	DAT0	0	R/W	These bits specify incrementing/decrementing of the transfer destination address (EDDAR). When an external device with DACK is designated as the transfer destination in single address mode, the specification by these bits is ignored. 0x: Fixed 10: Incremented (+1 in byte transfer, +2 in word transfer) 11: Decremented (–1 in byte transfer, –2 in word transfer)
5	DARIE	0	R/W	Destination Address Repeat Interrupt Enable When this bit is set to 1, in the event of destination address repeat area overflow the IRF bit is set to 1 and the EDA bit cleared to 0 in EDMDR, and transfer is terminated. If the EDIE bit in EDMDR is 1 when the IRF bit in EDMDR is set to 1, an interrupt request is sent to the CPU. When used together with block transfer mode, a destination address repeat interrupt is requested at the end of a block-size transfer. If the EDA bit is set to 1 in EDMDR for the channel on which transfer is terminated by a destination address repeat interrupt, transfer can be resumed from the state in which it ended. If a destination address repeat area has not been designated, this bit is ignored. 0: Destination address repeat interrupt is not requested 1: When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

8.5 Interrupt Sources

EXDMAC interrupt sources are a transfer end indicated by the transfer counter, and repeat area overflow interrupts. Table 8.4 shows the interrupt sources and their priority order.

Table 8.4 Interrupt Sources and Priority Order

Interrupt	Interrupt source	Interrupt Priority
EXDMTEND2	Transfer end indicated by channel 2 transfer counter	High
	Channel 2 source address repeat area overflow	
	Channel 2 destination address repeat area overflow	
EXDMTEND3	Transfer end indicated by channel 3 transfer counter	
	Channel 3 source address repeat area overflow	
	Channel 3 destination address repeat area overflow	Low

Interrupt sources can be enabled or disabled by means of the EDIE bit in EDMDR for the relevant channel, and can be sent to the interrupt controller independently. The relative priority order of the channels is determined by the interrupt controller (see table 8.4).

Figure 8.45 shows the transfer end interrupt logic. A transfer end interrupt is generated whenever the EDIE bit is set to 1 while the IRF bit is set to 1 in EDMDR.

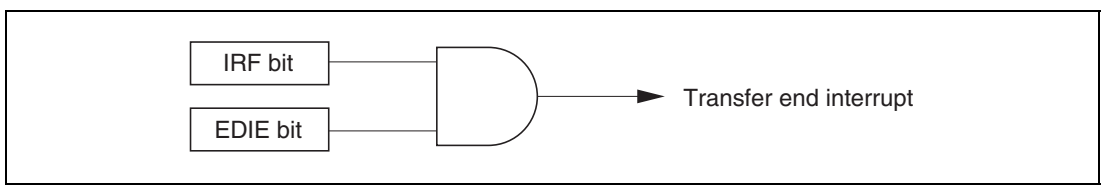


Figure 8.45 Transfer End Interrupt Logic

Interrupt source settings are made individually with the interrupt enable bits in the registers for the relevant channels. The transfer counter's transfer end interrupt is enabled or disabled by means of the TCEIE bit in EDMDR, the source address register repeat area overflow interrupt by means of the SARIE bit in EDACR, and the destination address register repeat area overflow interrupt by means of the DARIE bit in EDACR. When an interrupt source occurs while the corresponding interrupt enable bit is set to 1, the IRF bit in EDMDR is set to 1. The IRF bit is set by all interrupt sources indiscriminately.

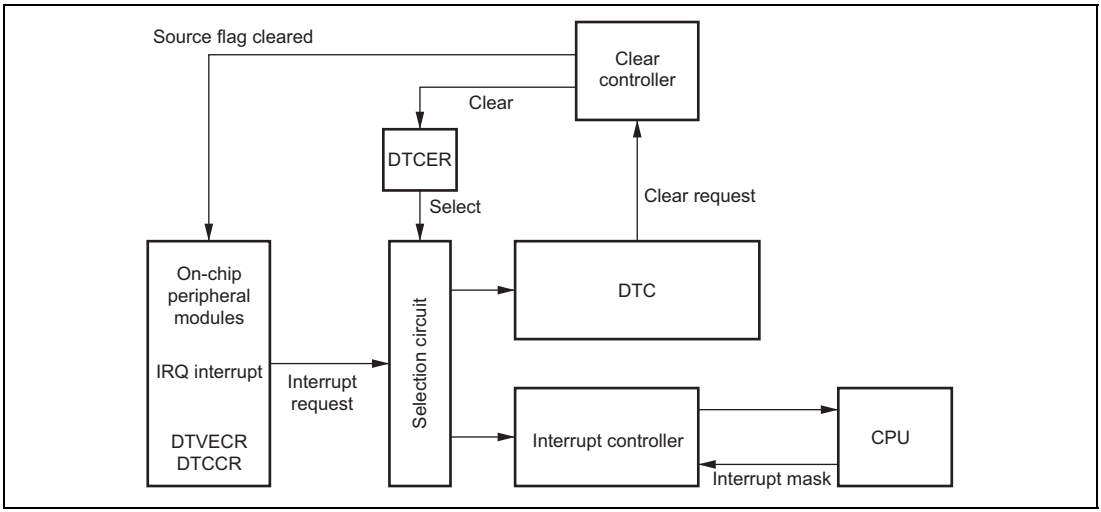


Figure 9.2 Block Diagram of DTC Activation Source Control

Port	Description	Mode 1	Mode 2	Mode 4	Mode 3, 7		Schmitt-triggered input Pin*3	Input Pull-up MOS Capability	Open Drain Output Capability	5-V Tolerance*2
					EXPE = 1	EXPE = 0				
Port F	General I/O port also functioning as interrupt inputs, bus control signal I/Os, SSU I/Os, and A/D converter inputs	PF7/φ				PF7/φ	—	—	—	—
		PF6/$\overline{AS}$/$\overline{AH}$				PF6			All output pin functions other than $\overline{AS}$ and $\overline{AH}$	
		$\overline{RD}$				PF5			All output pin functions other than $\overline{RD}$	
		$\overline{HWR}$				PF4			All output pin functions other than $\overline{HWR}$	
		PF3/$\overline{LWR}$/SSO0-C				PF3/SSO0-C			All output pin functions other than $\overline{LWR}$	
		PF2/$\overline{LCAS}$*2/DQML*1/$\overline{IRQ15\text{-}A}$/SSI0-C				PF2/$\overline{IRQ15\text{-}A}$/SSI0-C	$\overline{IRQ15\text{-}A}$		All output pin functions other than $\overline{LCAS}$*2 and DQML*1	
		PF1/$\overline{UCAS}$*2/DQMU*1/$\overline{IRQ14\text{-}A}$/SSCK0-C				PF1/$\overline{IRQ14\text{-}A}$/SSCK0-C	$\overline{IRQ14\text{-}A}$		All output pin functions other than $\overline{UCAS}$*2 and DQMU*1	
		PF0/$\overline{WAIT\text{-}A}$/$\overline{ADTRG0\text{-}B}$/$\overline{SCS0\text{-}C}$				PF0/$\overline{ADTRG0\text{-}B}$/$\overline{SCS0\text{-}C}$	—		All output pin functions	

10.1.5 Pin Functions

Port 1 pins also function as the pins for PPG outputs, TPU I/Os, EXDMAC I/Os (H8S/2426 Group, H8S/2426R Group), SSU I/Os, and DMAC I/Os (H8S/2424 Group). The correspondence between the register specification and the pin functions is shown below.

(1) Pin Functions of H8S/2426 Group and H8S/2426R Group

- P17/PO15/TIOCB2/TCLKD/$\overline{\text{EDRAK3}}$/$\overline{\text{SCS0-A}}$

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, TPU channel 2 settings (by bits MD3 to MD0 in TMDR_2, bits IOB3 to IOB0 in TIOR_2, and bits CCLR1 and CCLR0 in TCR_2), bits TPSC2 to TPSC0 in TCR_0 and TCR_5, bit NDER15 in NDERH of the PPG, bit EDRAKE in EDMDR_3 of the EXDMAC, bits MSS, CSS1, and CSS0 in SSCRH and bit SSUMS in SSCRL of the SSU, bits SCS0S1 and SCS0S0 in PFCR5, and bit P17DDR.

- Modes 1, 2, and 4 Modes 3 and 7 (EXPE = 1)

<table>
<tr><td>SSU settings</td><td colspan="5">(1) in table below</td><td>(2) in table below</td><td>(4) in table below</td><td>(3) in table below</td></tr>
<tr><td>EDRAKE</td><td colspan="4">0</td><td>1</td><td colspan="3">—</td></tr>
<tr><td>TPU channel 2 settings</td><td>(1) in table below</td><td colspan="3">(2) in table below</td><td>—</td><td colspan="3">—</td></tr>
<tr><td>P17DDR</td><td>—</td><td>0</td><td>1</td><td>1</td><td>—</td><td>0*6</td><td>0*6</td><td>—</td></tr>
<tr><td>NDER15</td><td>—</td><td>—</td><td>0</td><td>1</td><td>—</td><td colspan="3">—</td></tr>
<tr><td rowspan="3">Pin function</td><td rowspan="2">TIOCB2 output</td><td>P17 input</td><td>P17 output</td><td>PO15 output</td><td>$\overline{\text{EDRAK3}}$ output</td><td rowspan="3">$\overline{\text{SCS0-A}}$ input*3*7</td><td rowspan="3">$\overline{\text{SCS0-A}}$ I/O*5*7</td><td rowspan="3">$\overline{\text{SCS0-A}}$ output*4*7</td></tr>
<tr><td colspan="4">TIOCB2 input*1</td></tr>
<tr><td colspan="5">TCLKD input*2</td></tr>
</table>

- P14/PO12/TIOCA1/SSO0-A

  The pin function is switched as shown below according to the combination of the TPU channel 1 settings (by bits MD3 to MD0 in TMDR_1, bits IOA3 to IOA0 in TIOR_1, and bits CCLR1 and CCLR0 in TCR_1), bit NDER12 in NDERH of the PPG, bits MSS and BIDE in SSCRH, bit SSUMS in SSCRL, and bits TE and RE in SSER of the SSU, bits SSO0S1 and SSO0S0 in PFCR5, and bit P14DDR.

SSU settings	(1) in table below				(2) in table below	(3) in table below
TPU channel 1 settings	(1) in table below	(2) in table below			—	
P14DDR	—	0	1	1	0*5	—
NDER12	—	—	0	1	—	
Pin function	TIOCA1 output	P14 input	P14 output	PO12 output	SSO0-A input*3*6	SSO0-A output*4*6
		TIOCA1 input*1				

TPU channel 1 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

[Legend]

x: Don't care

Notes: 1. TIOCA1 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.
2. TIOCB1 output disabled.
3. When using as SSO0-A input, set SSO0S1 and SSO0S0 in PFCR5 to B'00 before other register setting.
4. When using as SSO0-A output, set SSO0S1 and SSO0S0 in PFCR5 to B'00 before other register setting.
5. P14DDR = 0 when the SSU pin is used as input.
6. Do not set up for SSU unless SSO0S1 and SSO0S0 = B'00 in PFCR5. Use as I/O port or TPU pin.

- P21/$\overline{\text{IRQ9-B}}$/PO1-A/TIOCB3-A

  The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR_3, bits IOB3 to IOB0 in TIORH_3, and bits CCLR2 to CCLR0 in TCR_3), bit NDER1 in NDERL of the PPG, bits PPGS and TPUS in PFCR3, bit P21DDR, and bit ITS9 in ITSR of the interrupt controller.

TPU channel 3 settings	(1) in table below	(2) in table below		
P21DDR	—	0	1	
NDER1	—	—	0	1
Pin function	TIOCB3-A output*4	P21 input	P21 output	PO1-A output*3
		TIOCB3-A input*1*4		
	$\overline{\text{IRQ9-B}}$ interrupt input*2			

Notes: 1. TIOCB3-A input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.
2. $\overline{\text{IRQ9-B}}$ input when the ITS9 bit in ITSR is 1.
3. When using as PO1-A output, set PPGS in PFCR3 to 0 before other register setting.
4. When using as TIOCB3-A input/output, set TPUS in PFCR3 to 0 before other register setting.

TPU channel 3 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]
x: Don't care

- PA3/A19/SCK4-B

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bit C/$\overline{A}$ in SMR_4 and bits CKE0 and CKE1 in SCR_4 of the SCI, bit A19E in PFCR1, bit SCK4S in PFCR4, and bit PA3DDR.

Operating mode	1, 2	4						
EXPE	—	—						
A19E	—	0					1	
CKE1	—	0				1	—	
C/$\overline{A}$	—	0			1	—	—	
CKE0	—	0		1	—	—	—	
PA3DDR	—	0	1	—	—	—	0	1
Pin function	A19 output	PA3 input	PA3 output	SCK4-B output*	SCK4-B output*	SCK4-B input*	PA3 input	A19 output

Operating mode	3, 7											
EXPE	0					1						
A19E	—					0					1	
CKE1	0				1	0				1	—	
C/$\overline{A}$	0			1	—	0			1	—	—	
CKE0	0		1	—	—	0		1	—	—	—	
PA3DDR	0	1	—	—	—	0	1	—	—	—	0	1
Pin function	PA3 input	PA3 output	SCK4-B output*	SCK4-B output*	SCK4-B input*	PA3 input	PA3 output	SCK4-B output*	SCK4-B output*	SCK4-B input*	PA3 input	A19 output

Note: * When using as SCK4-B input/output, set SCK4S in PFCR4 to 1 before other register setting.

d. Phase counting mode 4

Figure 11.29 shows an example of phase counting mode 4 operation, and table 11.36 summarizes the TCNT up/down-count conditions.

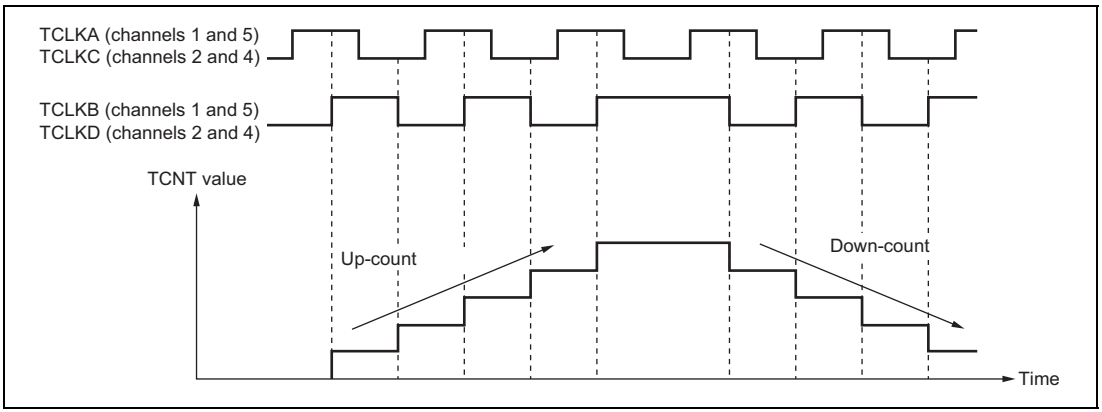


Figure 11.29 Example of Phase Counting Mode 4 Operation

Table 11.36 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4) TCLKE (Channels 7 and 11) TCLKG (Channels 8 and 10)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4) TCLKF (Channels 7 and 11) TCLKH (Channels 8 and 10)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	Don't care
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	Don't care
↓	Low level	

[Legend]
↑: Rising edge
↓: Falling edge

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode)

Bit Rate (bit/s)	Operating Frequency φ (MHz)													
	8		10		16		20		25		30		33	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110														
250	3	124	—	—	3	249								
500	2	249	—	—	3	124	—	—			3	233		
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—
1 M	0	1			0	3	0	4	—	—	—	—	—	—
2.5 M			0	0*			0	1	—	—	0	2	—	—
5 M							0	0*	—	—	—	—	—	—

[Legend]

Blank: Cannot be set.

—: Can be set, but there will be a degree of error.

*: Continuous transfer is not possible.

Table 15.7 Maximum Bit Rate with External Clock Input (Clocked Synchronous Mode)

φ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)	φ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
8	1.3333	1333333.3	18	3.0000	3000000.0
10	1.6667	1666666.7	20	3.3333	3333333.3
12	2.0000	2000000.0	25	4.1667	4166666.7
14	2.3333	2333333.3	30	5.0000	5000000.0
16	2.6667	2666666.7	33	5.5000	5500000.0

16.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. The reception procedure and operations in slave receive mode are described below.

1. Set the ICE bit in ICCRA to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to CKS0 bits in ICCRA to 1. (Initial setting) Set the MST and TRS bits in ICCRA to select slave receive mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise of the 9th clock pulse. At the same time, RDRF in ICSR is set to read ICDRR (dummy read) and RDRF is cleared. (Since the read data show the slave address and R/$\overline{W}$, it is not used.)
3. Clear RDRF after reading ICDRR every time RDRF is set. If 8th receive clock pulse falls while RDRF is 1, SCL is fixed low until ICDRR is read. The change of the acknowledge before reading ICDRR, to be returned to the master device, is reflected to the next transmit frame.
4. The last byte data is read by reading ICDRR.

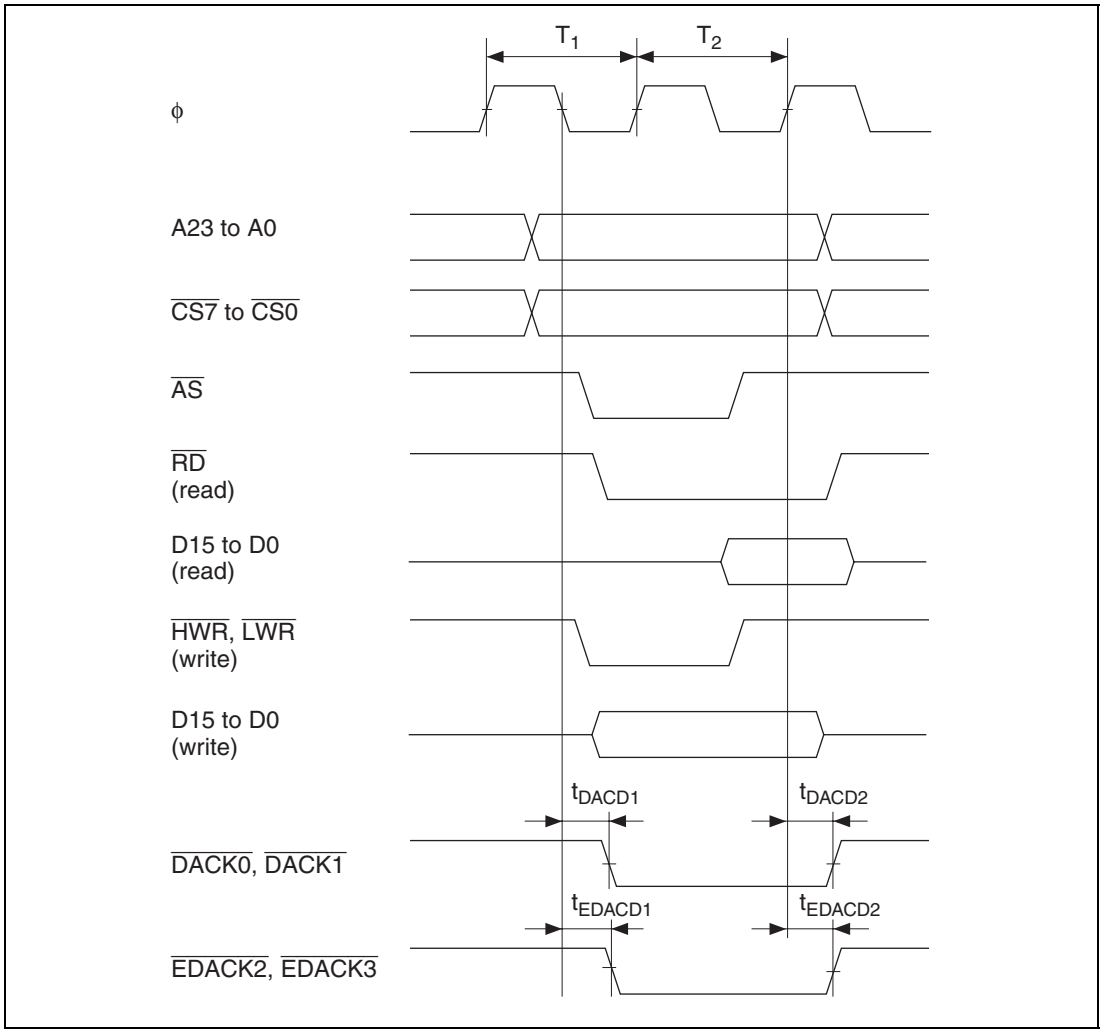


Figure 25.31 DMAC and EXDMAC Single Address Transfer Timing: Two-State Access

Item			Symbol	Min.	Max.	Unit	Test Conditions
SSU*	$\overline{SCS}$ hold time	Master	t_{LAG}	2.5	—	t_{cyc}	Figures 25.86 to 25.89
		Slave		2.5	—		
	Data output delay time	Master	t_{OD}	—	40	ns	
		Slave		—	40		
	Data output hold time	Master	t_{OH}	–5	—	ns	
		Slave		0	—		
	Continuous transmit delay time	Master	t_{TD}	2.5	—	t_{cyc}	
		Slave		2.5	—		
	Slave access time		t_{SA}	—	1	t_{cyc}	Figures 25.88 and 25.89
	Slave out release time		t_{REL}	—	1	t_{cyc}	

Note * SSU: Synchronous serial communication unit

25.5.4 A/D Conversion Characteristics

Table 25.48 A/D Conversion Characteristics

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz

Item	Min.	Typ.	Max.	Unit
Resolution	10	10	10	Bit
Conversion time	2.5*	—	—	µs
Analog input capacitance	—	—	15	pF
Permissible signal source impedance	—	—	5	kΩ
Nonlinearity error	—	—	±3.5	LSB
Offset error	—	—	±3.5	LSB
Full-scale error	—	—	±3.5	LSB
Quantization error	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	LSB

Note: * For 40 states at ADCLK = 16 MHz.