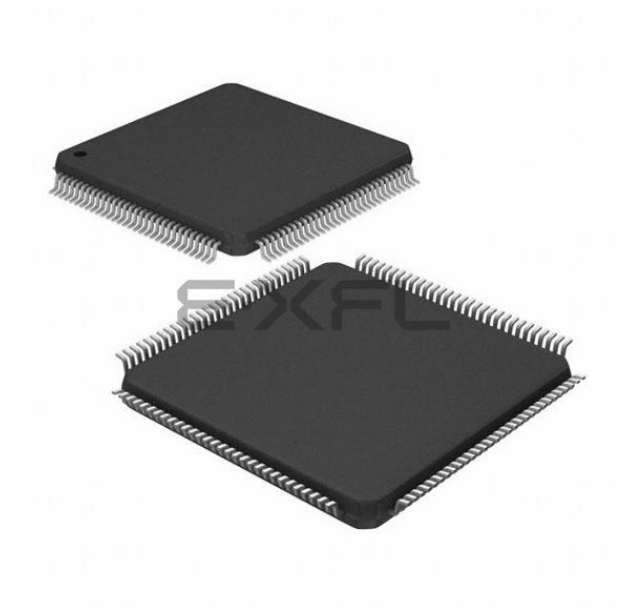
Renesas Electronics America Inc - R4F24249NVFPV Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24249nvfpv

(2) 16-Bit Access Space

Figure 6.9 illustrates data alignment control for the 16-bit access space. With the 16-bit access space, the upper data bus (D15 to D8) and lower data bus (D7 to D0) are used for accesses. The amount of data that can be accessed at one time is one byte or one word, and a longword access is executed as two word accesses.

In byte access, whether the upper or lower data bus is used is determined by whether the address is even or odd. The upper data bus is used for an even address, and the lower data bus for an odd address.

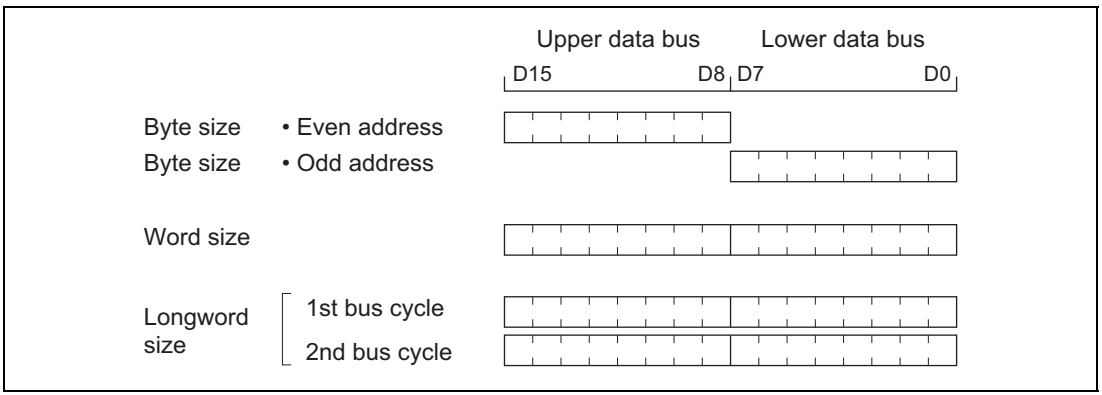


Figure 6.9 Access Sizes and Data Alignment Control (16-Bit Access Space)

(3) Read after Write

If an external read occurs after an external write while the ICIS2 bit is set to 1 in BCR, an idle cycle is inserted at the start of the read cycle.

Figure 6.79 shows an example of the operation in this case. In this example, bus cycle A is a CPU write cycle and bus cycle B is a read cycle from an external device. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the CPU write data and read data from an external device. In (b), an idle cycle is inserted, and a data collision is prevented.

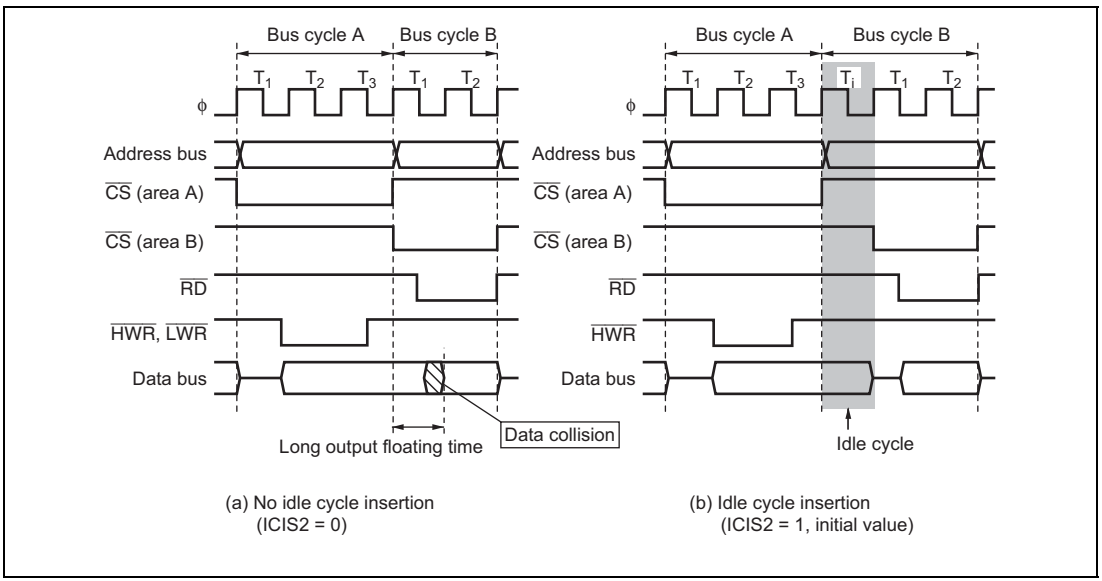
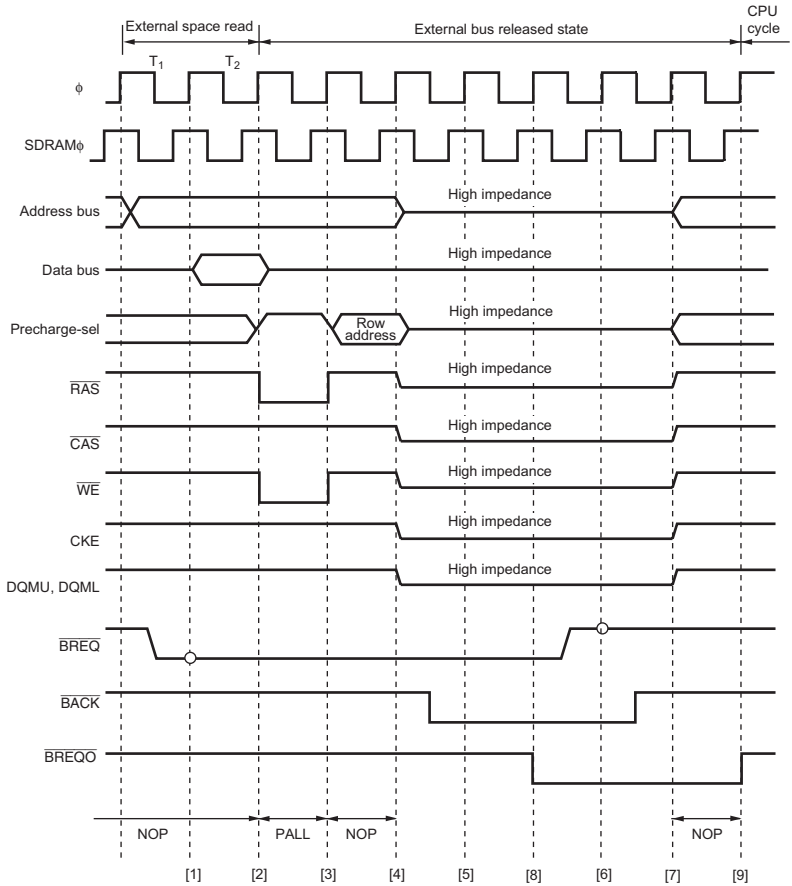


Figure 6.79 Example of Idle Cycle Operation (Read after Write)

Figure 6.97 shows the timing for transition to the bus released state with the synchronous DRAM interface.

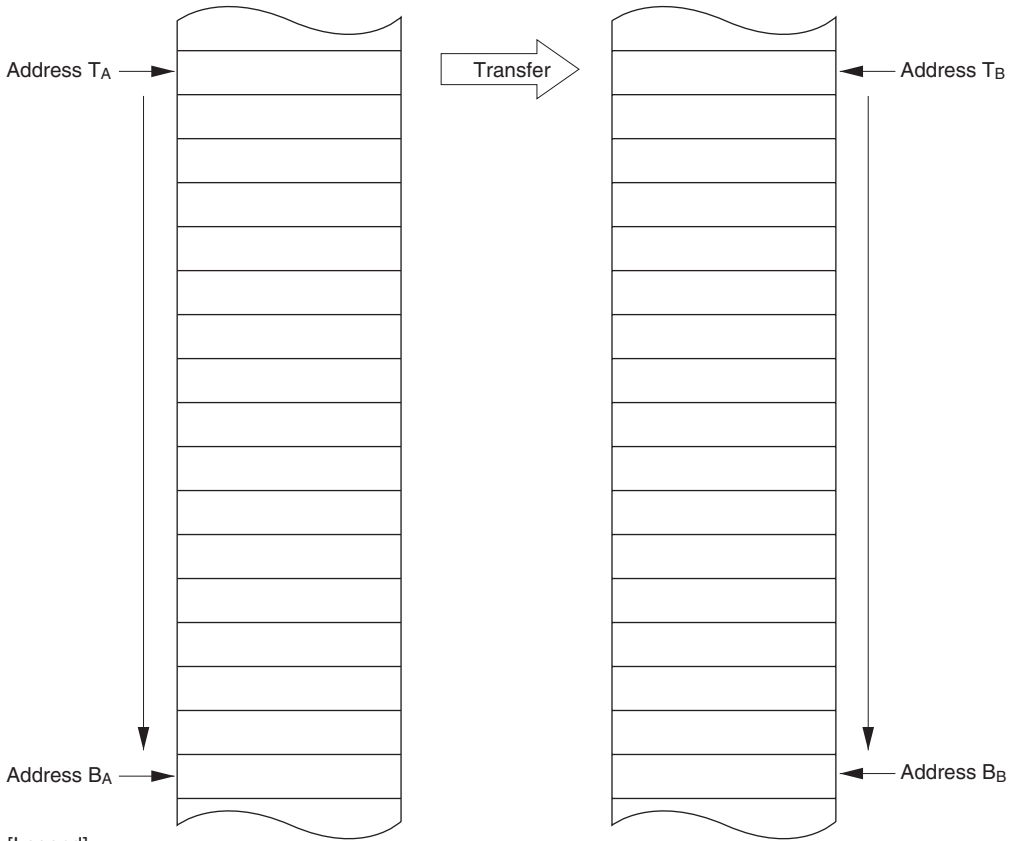


[1] Low level of $\overline{\text{BREQ}}$ signal is sampled at rise of φ.
[2] PALL command is issued.
[3] Bus control signal returns to be high at end of external space access cycle.
At least one state from sampling of $\overline{\text{BREQ}}$ signal.
[4] $\overline{\text{BACK}}$ signal is driven low, releasing bus to external bus master..
[5] $\overline{\text{BREQ}}$ signal state is also sampled in external bus released state.
[6] High level of $\overline{\text{BREQ}}$ signal is sampled.
[7] $\overline{\text{BACK}}$ signal is driven high, ending external bus release cycle.
[8] When there is external access or refresh request of internal bus master during external bus release while the $\overline{\text{BREQOE}}$ bit is set to 1, $\overline{\text{BREQO}}$ signal goes low.
[9] $\overline{\text{BREQO}}$ signal goes high 1.5 states after rising edge of $\overline{\text{BACK}}$ signal. If $\overline{\text{BREQO}}$ signal is asserted because of auto-refreshing request, it retains low until auto-refresh cycle starts up.

Figure 6.97 Bus Release State Transition Timing when Synchronous DRAM Interface

Note: The synchronous DRAM interface is not supported by the H8S/2426 Group and H8S/2424 Group.

Figure 7.11 illustrates operation in normal mode.



[Legend]
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \cdot (-1)^{SAID} \cdot (2^{DTSZ} \cdot (N - 1))$
Address $B_B = L_B + DAIDE \cdot (-1)^{DAID} \cdot (2^{DTSZ} \cdot (N - 1))$
Where: L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRA

Figure 7.11 Operation in Normal Mode

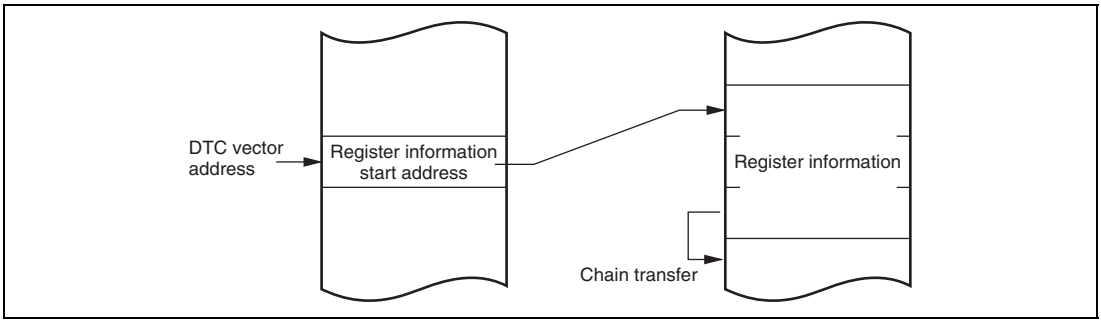


Figure 9.4 Correspondence between DTC Vector Address and Register Information

Table 9.2 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address	DTCE*[1]	Priority
Software	Write to DTVECR	DTVECR	H'0400 + (DTVECR[7:0] × 2)	—	High
External pin	IRQ0	16	H'0420	DTCEA7	
	IRQ1	17	H'0422	DTCEA6	
	IRQ2	18	H'0424	DTCEA5	
	IRQ3	19	H'0426	DTCEA4	
	IRQ4	20	H'0428	DTCEA3	
	IRQ5	21	H'042A	DTCEA2	
	IRQ6	22	H'042C	DTCEA1	
	IRQ7	23	H'042E	DTCEA0	
	IRQ8*[2]	24	H'0430	DTCEB7	
	IRQ9*[2]	25	H'0432	DTCEB6	
	IRQ10*[2]	26	H'0434	DTCEB5	
	IRQ11*[2]	17	H'0436	DTCEB4	
	IRQ12*[2]	18	H'0438	DTCEB3	
	IRQ13*[2]	19	H'043A	DTCEB2	
	IRQ14*[2]	30	H'043C	DTCEB1	
	IRQ15*[2]	31	H'043E	DTCEB0	
A/D_0	ADI0	38	H'044C	DTCEC6	Low

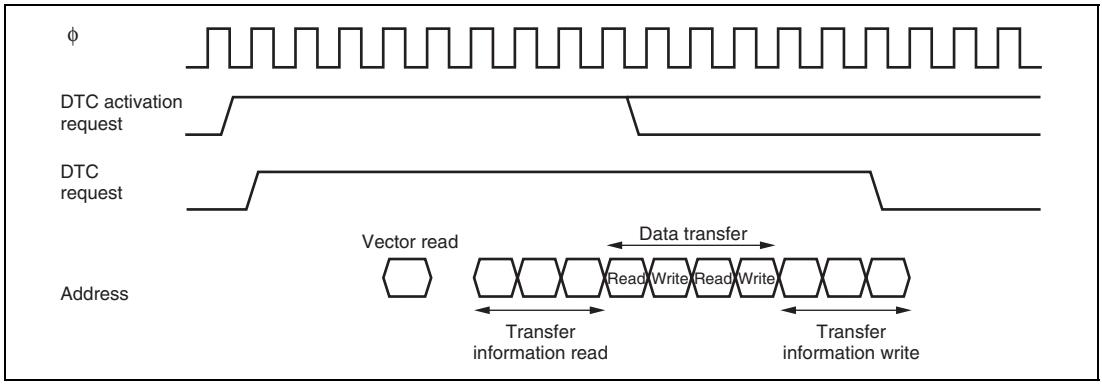


Figure 9.11 DTC Operation Timing (Example of Block Transfer Mode, with Block Size of 2)

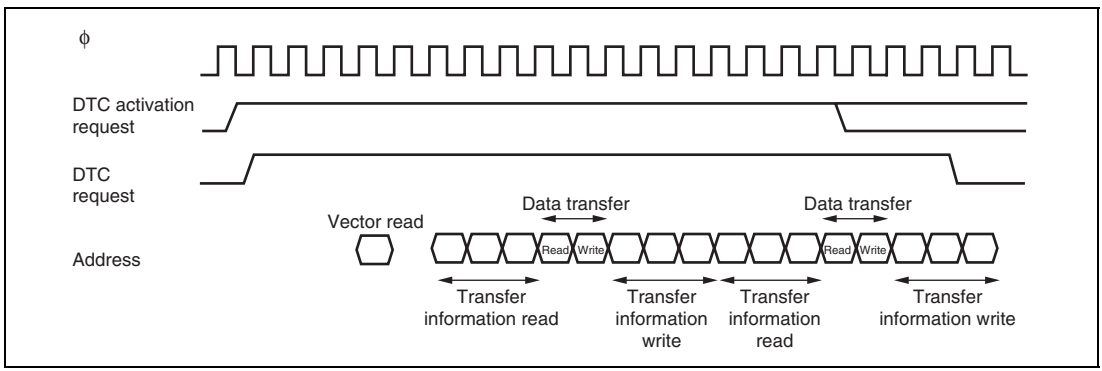


Figure 9.12 DTC Operation Timing (Example of Chain Transfer)

9.6 Procedures for Using DTC

9.6.1 Activation by Interrupt

The procedure for using the DTC with interrupt activation is as follows:

1. Set the MRA, MRB, SAR, DAR, CRA, and CRB register information in the on-chip RAM.
2. Set the start address of the register information in the DTC vector address.
3. Set the corresponding bit in DTCER to 1.
4. Set the enable bits for the interrupt sources to be used as the activation sources to 1. The DTC is activated when an interrupt used as an activation source is generated.
5. After the end of one data transfer, or after the specified number of data transfers have ended, the DTCE bit is cleared to 0 and a CPU interrupt is requested. If the DTC is to continue transferring data, set the DTCE bit to 1.

9.6.2 Activation by Software

The procedure for using the DTC with software activation is as follows:

1. Set the MRA, MRB, SAR, DAR, CRA, and CRB register information in the on-chip RAM.
2. Set the start address of the register information in the DTC vector address.
3. Check that the SWDTE bit is 0.
4. Write 1 to SWDTE bit and the vector number to DTVECR.
5. Check the vector number written to DTVECR.
6. After the end of one data transfer, if the DISEL bit is 0 and a CPU interrupt is not requested, the SWDTE bit is cleared to 0. If the DTC is to continue transferring data, set the SWDTE bit to 1. When the DISEL bit is 1, or after the specified number of data transfers have ended, the SWDTE bit is held at 1 and a CPU interrupt is requested.

Port	Description	Mode 1	Mode 2	Mode 4	Mode 3, 7		Schmitt-triggered input Pin*3	Input Pull-up MOS Capability	Open Drain Output Capability	5-V Tolerance*2
					EXPE = 1	EXPE = 0				
Port F	General I/O port also functioning as interrupt inputs, bus control signal I/Os, SSU I/Os, and A/D converter inputs	PF7/φ				PF7/φ	—	—	—	—
		PF6/$\overline{AS}$/$\overline{AH}$				PF6			All output pin functions other than $\overline{AS}$ and $\overline{AH}$	
		$\overline{RD}$				PF5			All output pin functions other than $\overline{RD}$	
		$\overline{HWR}$				PF4			All output pin functions other than $\overline{HWR}$	
		PF3/$\overline{LWR}$/SSO0-C				PF3/SSO0-C			All output pin functions other than $\overline{LWR}$	
		PF2/$\overline{LCAS}$*2/DQML*1/$\overline{IRQ15\text{-}A}$/SSI0-C				PF2/$\overline{IRQ15\text{-}A}$/SSI0-C	$\overline{IRQ15\text{-}A}$		All output pin functions other than $\overline{LCAS}$*2 and DQML*1	
		PF1/$\overline{UCAS}$*2/DQMU*1/$\overline{IRQ14\text{-}A}$/SSCK0-C				PF1/$\overline{IRQ14\text{-}A}$/SSCK0-C	$\overline{IRQ14\text{-}A}$		All output pin functions other than $\overline{UCAS}$*2 and DQMU*1	
		PF0/$\overline{WAIT\text{-}A}$/$\overline{ADTRG0\text{-}B}$/$\overline{SCS0\text{-}C}$				PF0/$\overline{ADTRG0\text{-}B}$/$\overline{SCS0\text{-}C}$	—		All output pin functions	

10.5 Port 5

Port 5 is a 4-bit I/O port. Port 5 has the following registers. For the port function control registers, refer to section 10.18, Port Function Control Registers.

- Port 5 data direction register (P5DDR)
- Port 5 data register (P5DR)
- Port 5 register (PORT5)
- Port 5 open drain control register (P5ODR)
- Port function control register 4 (PFCR4)

10.5.1 Port 5 Data Direction Register (P5DDR)

The individual bits of P5DDR specify input or output for the pins of port 5. P5DDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved
3	P53DDR	0	W	When a pin function is specified as a general purpose I/O, setting this bit to 1 makes the corresponding pin an output port, while clearing this bit to 0 makes the corresponding pin an input port.
2	P52DDR	0	W	
1	P51DDR	0	W	
0	P50DDR	0	W	

10.5.2 Port 5 Data Register (P5DR)

P5DR stores output data for the port 5 pins.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.
3	P53DR	0	R/W	Output data for a pin is stored when the pin function is specified as a general purpose I/O.
2	P52DR	0	R/W	
1	P51DR	0	R/W	
0	P50DR	0	R/W	

- PB1/A9/TIOCB6

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, TPU channel 6 settings (by bits MD3 to MD0 in TMDR_6, bits IOB3 to IOB0 in TIORH_6, and bits CCLR2 to CCLR0 in TCR_6), and bit PB1DDR.

Operating mode	1, 2	4 3, 7 (EXPE = 1)		3, 7 (EXPE = 0)		
TPU channel 6 settings	—	—		(1) in table below	(2) in table below	
PB1DDR	—	0	1	—	0	1
Pin function	A9 output	PB1 input	A9 output	TIOCB6 output	PB1 input	PB1 output
					TIOCB6 input*	

TPU channel 6 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

Note: * TIOCB6 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin. After a match between TCNT and TGR, the compare match signal is not generated until the (TIOC pin) TCNT input clock is generated.

Figure 11.33 shows output compare output timing.

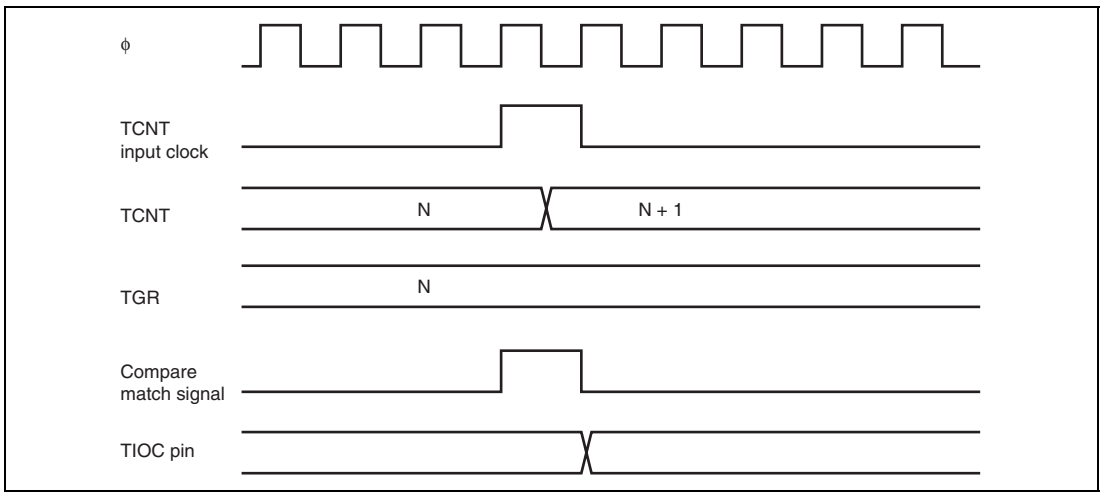


Figure 11.33 Output Compare Output Timing

12.4.6 Example of Non-Overlapping Pulse Output (Example of Four-Phase Complementary Non-Overlapping Output)

Figure 12.9 shows an example in which pulse output is used for four-phase complementary non-overlapping pulse output.

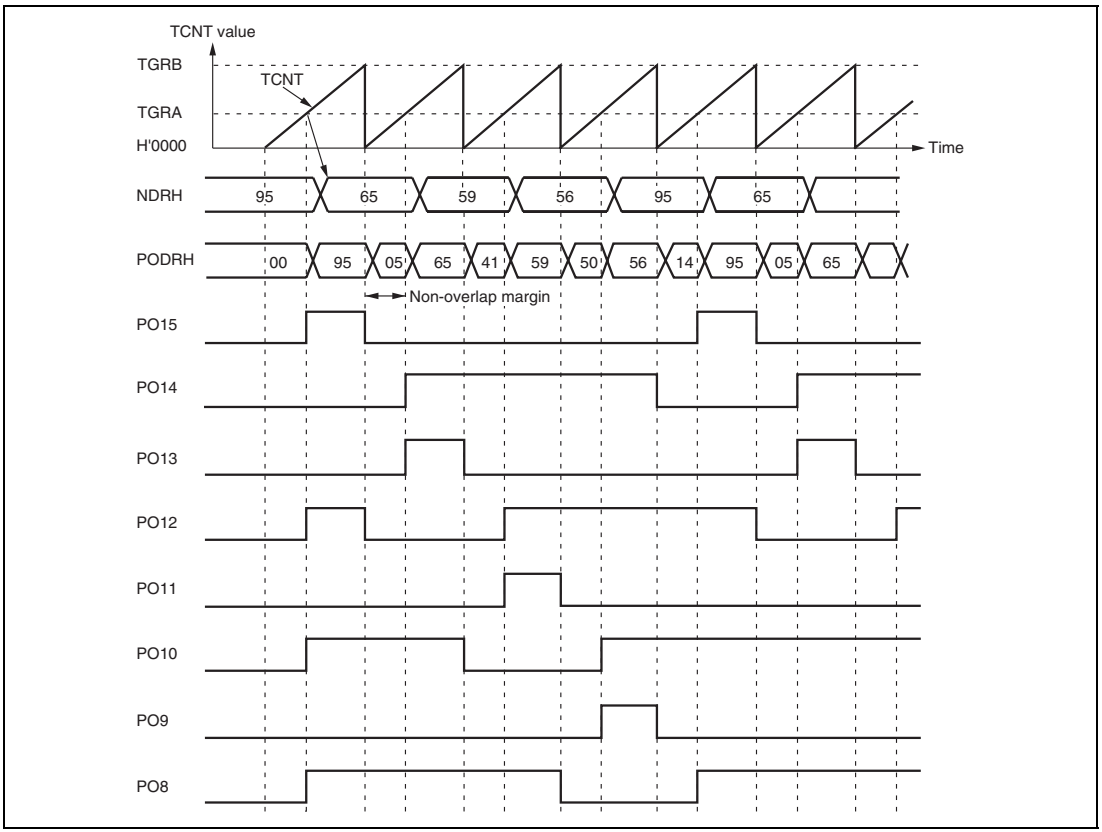


Figure 12.9 Non-Overlapping Pulse Output Example (Four-Phase Complementary)

Section 13 8-Bit Timers (TMR)

This LSI has an on-chip 8-bit timer module with two channels operating on the basis of an 8-bit counter. The 8-bit timer module can be used to count external events and be used as a multifunction timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with an arbitrary duty cycle using a compare-match signal with two registers.

13.1 Features

- Selection of seven clock sources

  The counters can be driven by one of six internal clock signals (ϕ/2, ϕ/8, ϕ/32, ϕ/64, ϕ/1024, or ϕ/8192) or an external clock input
- Selection of three ways to clear the counters

  The counters can be cleared on compare match A or B, or by an external reset signal (rising edge, rising and falling edges, falling edge, low level, or high level)
- Timer output control by a combination of two compare match signals

  The timer output signal in each channel is controlled by a combination of two independent compare match signals, enabling the timer to generate output waveforms with an arbitrary duty cycle or PWM output
- Provision for cascading of two channels (TMR_0 and TMR_1)

  Operation as a 16-bit timer is possible, using TMR_0 for the upper 8 bits and TMR_1 for the lower 8 bits (16-bit count mode)

  TMR_1 can be used to count TMR_0 compare matches (compare match count mode)
- Three independent interrupts

  Compare match A and B and overflow interrupts can be requested independently
- A/D converter conversion start trigger can be generated

- Receive shift register_3 (RSR_3)
- Transmit shift register_3 (TSR_3)
- Receive data register_3 (RDR_3)
- Transmit data register_3 (TDR_3)
- Serial mode register_3 (SMR_3)
- Serial control register_3 (SCR_3)
- Serial status register_3 (SSR_3)
- Smart card mode register_3 (SCMR_3)
- Bit rate register_3 (BRR_3)
- Receive shift register_4 (RSR_4)
- Transmit shift register_4 (TSR_4)
- Receive data register_4 (RDR_4)
- Transmit data register_4 (TDR_4)
- Serial mode register_4 (SMR_4)
- Serial control register_4 (SCR_4)
- Serial status register_4 (SSR_4)
- Smart card mode register_4 (SCMR_4)
- Bit rate register_4 (BRR_4)

15.3.1 Receive Shift Register (RSR)

RSR is a shift register used to receive serial data that is input to the RxD pin and convert it into parallel data. When one byte of data has been received, it is transferred to RDR automatically. RSR cannot be directly accessed by the CPU.

15.3.2 Receive Data Register (RDR)

RDR is an 8-bit register that stores receive data. When the SCI has received one byte of serial data, it transfers the received serial data from RSR to RDR where it is stored. After this, RSR is receive-enabled. Since RSR and RDR function as a double buffer in this way, enables continuous receive operations to be performed. After confirming that the RDRF bit in SSR is set to 1, read RDR for only once. RDR cannot be written to by the CPU.

17.7 Usage Notes

17.7.1 Module Stop Function Setting

Operation of the A/D converter can be disabled or enabled using the module stop control register. The initial setting is for operation of the A/D converter to be halted. Register access is enabled by clearing the module stop state. Set the CKS1 and CKS2 bits to 1 to set ADCLK to ϕ, and clear the ADST, TRGS1, TRGS0, and EXTRGS bits all to 0 to disable A/D conversion when entering module stop state after operation of the A/D converter. After that, set the module stop control register after executing a dummy read by one word. For details, see section 23, Power-Down Modes.

17.7.2 A/D Input Hold Function in Software Standby Mode

When this LSI enters software standby mode with A/D conversion enabled, the analog inputs are retained, and the analog power supply current is equal to as during A/D conversion. If the analog power supply current needs to be reduced in software standby mode, set the CKS1 and CKS2 bits to 1 to set ADCLK to ϕ, and clear the ADST, TRGS1, TRGS0, and EXTRGS bits all to 0 to disable A/D conversion. After that, enter software standby mode after executing a dummy read by one word.

17.7.3 Restarting the A/D Converter

When the ADST bit has been cleared to 0, A/D converter stops in synchronization with the ADCLK and then enters the standby sate. After the ADST bit has been cleared, the converter may not actually make the transition to the standby state for up to 10 cycles (ϕ), so do not change the channels of the ADCLK, motion mode, or analog input at this time.

When restarting the A/D converter right after the ADST bit has been cleared to 0, read the 16 bytes from ADDRA to ADDRH and then start the A/D converter by setting the ADST bit to 1. If the converter is in single mode or one-cycle scan mode, however, the ADST bit can be set to 1 by clearing the ADF bit to 0 after confirming that the ADF bit had been set to 1 on completion of the previous round of conversion.

19.4.6 $\overline{\text{SCS}}$ Pin Control and Conflict Error

When bits CSS1 and CSS0 in SSCRH are specified to B'10 and the SSUMS bit in SSCRL is cleared to 0, the $\overline{\text{SCS}}$ pin functions as an input (Hi-Z) to detect conflict error. The conflict detection period is from setting the MSS bit in SSCRH to 1 to starting serial transfer and after transfer ends. When a low level signal is input to the $\overline{\text{SCS}}$ pin within the period, a conflict error occurs. At this time, the CE bit in SSSR is set to 1 and the MSS bit is cleared to 0.

Note: While the CE bit is set to 1, transmission or reception is not resumed. Clear the CE bit to 0 before resuming the transmission or reception.

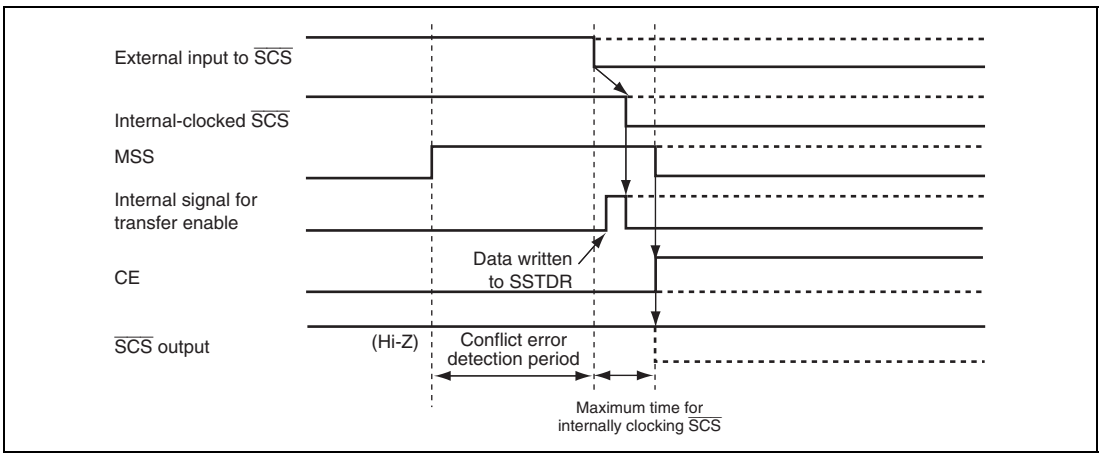


Figure 19.10 Conflict Error Detection Timing (Before Transfer)

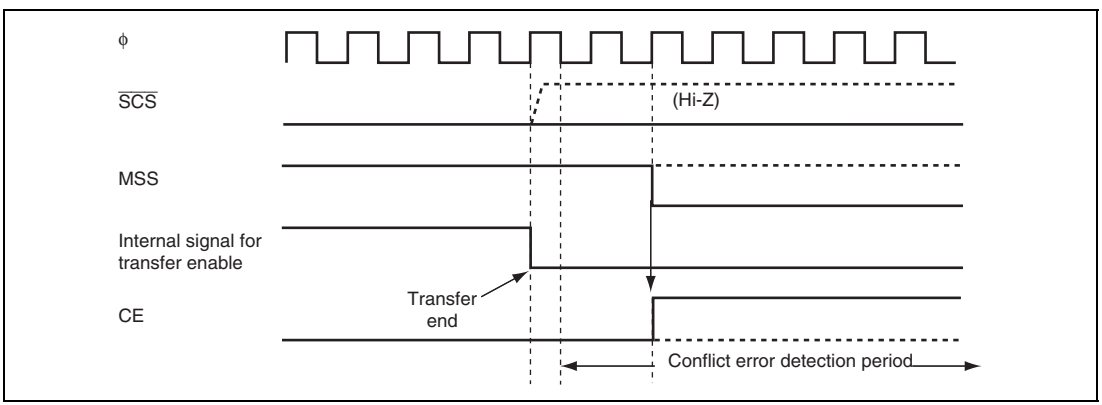
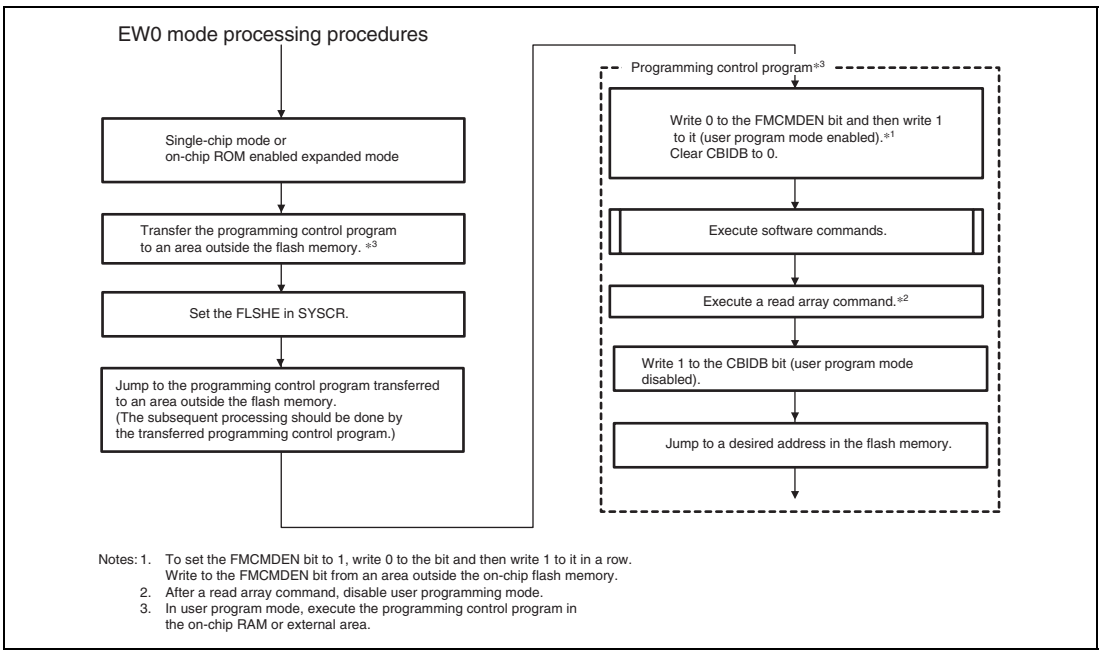


Figure 19.11 Conflict Error Detection Timing (After Transfer End)

21.3.2 EW0 Mode

Setting the FMCMDEN bit in FLMCR1 to 1 shifts the flash memory into the user programming mode, in which commands can be accepted. Figure 21.2 shows how to set and clear the EW0 mode.

Programming and erasure are controlled through software commands. The flash memory state after programming or erasure can be checked through FLMSTR or the status register.



Notes: 1. To set the FMCMDEN bit to 1, write 0 to the bit and then write 1 to it in a row. Write to the FMCMDEN bit from an area outside the on-chip flash memory.
2. After a read array command, disable user programming mode.
3. In user program mode, execute the programming control program in the on-chip RAM or external area.

Figure 21.2 Setting and Clearing EW0 Mode

21.5 Status Register

The status register indicates the state of flash memory operation and whether erasure or programming has ended successfully or with an error. The status register contents can be read through the FMRDY, FMPRSF, and FMERSF bits in FLMSTR.

Table 21.6 shows the status register.

In the EW0 mode, the status register can be read with the following timing.

- When a read status register command is issued and then an even address in the user ROM or data flash is read
- When a program command, a block erase command, or a block blank check command is issued and then an even address in the user ROM or data flash is read before a read array command is issued

Table 21.6 Status Register

Bits in Status Register	Bits in FMLSTR	Status Name	Status		Value after Reset
			0	1	
SR0 (D0)	—	Reserved	—	—	—
SR1 (D1)	—	Reserved	—	—	—
SR2 (D2)	—	Reserved	—	—	—
SR3 (D3)	—	Reserved	—	—	—
SR4 (D4)	FMPRSF	Programming status	Completed successfully	Ended with error	0
SR5 (D5)	FMERSF	Erase status	Completed successfully	Ended with error	0
SR6 (D6)	—	Reserved	—	—	
SR7 (D7)	FMRDY	Sequencer status	Busy	Ready	1

[Legend]

SR0 to SR7: Status register data

D0 to D7: Data bus from which the bit is read when a read status register command is issued.

Note: The FMERSF (SR5) and FMPRSF (SR4) bits are cleared to 0 by a clear status register command.

When the FMERSF (SR5) or FMPRSF (SR4) bit is 1, the program, block erase, and block blank check commands are not accepted.

3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, $V_{IH}min = V_{CC} \times 0.9$, and $V_{IL}max = 0.3$ V.
4. I_{CC} depends on V_{CC} and f as follows:
   $I_{CC}max = 5.2$ (mA) + 1.66 (mA/(MHz)) × f (normal operation)
   $I_{CC}max = 2.6$ (mA) + 1.28 (mA/(MHz)) × f (sleep mode)
5. Applied when $\overline{RES}$ is low at power-on.

Table 25.17 Permissible Output Currents

Conditions: $V_{CC} = 3.0$ V to 3.6 V, $AV_{CC} = 3.0$ V to 3.6 V, $V_{ref} = 3.0$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V*

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	All output pins except the I^2C pins	I_{OL}	—	—	4.0	mA
	I^2C output pins	I_{OL}	—	—	8.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in table 25.29.

Note: * When the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
PF0/$\overline{\text{WAIT-A}}$/ $\overline{\text{OE-A}}$*[1]	1, 2, 3, 4, 7	T	T	[$\overline{\text{WAIT-A}}$ input] T [$\overline{\text{OE-A}}$ output] T [$\overline{\text{OE-A}}$ output, OPE = 1] H [Other than the above] Keep	[$\overline{\text{WAIT-A}}$ input] T [$\overline{\text{OE-A}}$ output, OPE = 0] T [Other than the above] Keep	[$\overline{\text{WAIT-A}}$ input] $\overline{\text{WAIT-A}}$ [$\overline{\text{OE-A}}$ output, OPE = 0] $\overline{\text{OE-A}}$ [Other than the above] I/O port
PG6/$\overline{\text{BREQ-A}}$	1, 2, 3, 4, 7	T	T	[$\overline{\text{BREQ-A}}$ input] T [Other than the above] Keep	[$\overline{\text{BREQ-A}}$ input] $\overline{\text{BREQ-A}}$ [Other than the above] Keep	[$\overline{\text{BREQ-A}}$ input] $\overline{\text{BREQ-A}}$ [Other than the above] I/O port
PG5/$\overline{\text{BACK-A}}$	1, 2, 3, 4, 7	T	T	[$\overline{\text{BACK-A}}$ output] $\overline{\text{BACK-A}}$ [Other than the above] Keep	[$\overline{\text{BACK-A}}$ output] $\overline{\text{BACK-A}}$ [Other than the above] Keep	[$\overline{\text{BACK-A}}$ output] $\overline{\text{BACK-A}}$ [Other than the above] I/O port
PG4/ $\overline{\text{BREQO-A}}$/ $\overline{\text{CS4}}$	1, 2, 3, 4, 7	T	T	[$\overline{\text{BREQO-A}}$ output] $\overline{\text{BREQO-A}}$ [$\overline{\text{CS4}}$ output, OPE = 0] T [$\overline{\text{CS4}}$ output, OPE = 1] H [Other than the above] Keep	[$\overline{\text{BREQO-A}}$ output] $\overline{\text{BREQO-A}}$ [$\overline{\text{CS4}}$ output] T [Other than the above] Keep	[$\overline{\text{BREQO-A}}$ output] $\overline{\text{BREQO-A}}$ [$\overline{\text{CS4}}$ output] $\overline{\text{CS4}}$ [Other than the above] I/O port