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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24268nvfqv

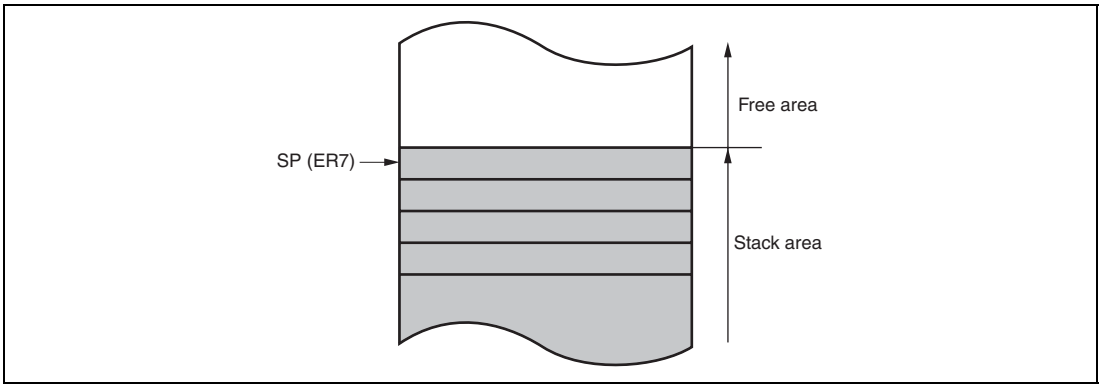

Figure 2.8 Stack

2.4.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0.)

2.4.3 Extended Register (EXR)

EXR is an 8-bit register that can be manipulated by the LDC, STC, ANDC, ORC, and XORC instructions. When these instructions except for the STC instruction is executed, all interrupts including NMI will be masked for three states after execution is completed.

Bit	Bit Name	Initial Value	R/W	Description
7	T	0	R/W	Trace Bit When this bit is set to 1, a trace exception is started each time an instruction is executed. When this bit is cleared to 0, instructions are executed in sequence.
6 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	I2	1	R/W	These bits designate the interrupt mask level (0 to 7). For details, refer to section 5, Interrupt Controller.
1	I1	1	R/W	
0	I0	1	R/W	

(5) Idle Cycle in Case of DRAM Space Access after Normal Space Access

In a DRAM space access following a normal space access, the settings of bits ICIS2, ICIS1, ICIS0, and IDLC in BCR are valid. However, in the case of consecutive reads in different areas, for example, if the second read is a full access to DRAM space, only a T_p cycle is inserted, and a T_i cycle is not. The timing in this case is shown in figure 6.81.

Note: The DRAM interface is not supported by the 5-V version.

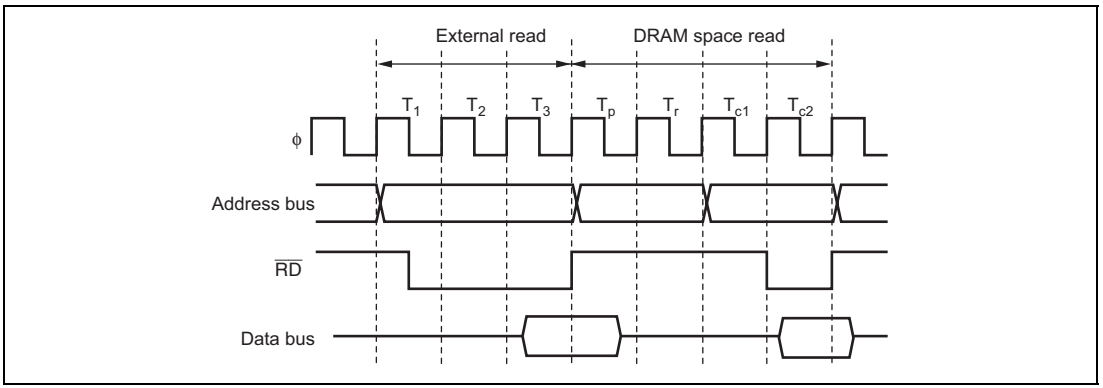

Figure 6.81 Example of DRAM Full Access after External Read (CAST = 0)

In burst access in RAS down mode, the settings of bits ICIS2, ICIS1, ICIS0, and IDLC are valid and an idle cycle is inserted. The timing in this case is illustrated in figures 6.82 and 6.83.

Table 7.4 DMAC Transfer Modes

Transfer Mode		Transfer Source	Remarks
Short address mode	Dual address mode • 1-byte or 1-word transfer for a single transfer request • Specify source and destination addresses to transfer data in two bus cycles. (1) Sequential mode • Memory address incremented or decremented by 1 or 2 • Number of transfers: 1 to 65,536 (2) Idle mode • Memory address fixed • Number of transfers: 1 to 65,536 (3) Repeat mode • Memory address incremented or decremented by 1 or 2 • Continues transfer after sending number of transfers (1 to 256) and restoring the initial value	• TPU channel 0 to 5 compare match/input capture A interrupt • SCI transmit data empty interrupt • SCI receive data full interrupt • A/D converter conversion end interrupt • External request	• Up to 4 channels can operate independently • External request applies to channel B only • Single address mode applies to channel B only
	Single address mode • 1-byte or 1-word transfer for a single transfer request • 1-bus cycle transfer by means of $\overline{\text{DACK}}$ pin instead of using address for specifying I/O • Sequential mode, idle mode, or repeat mode can be specified	• External request	

ETCRAL is decremented by 1 each time a byte or word transfer is performed. In response to a single transfer request, burst transfer is performed until the value in ETCRAL reaches H'00. ETCRAL is then loaded with the value in ETCRAH. At this time, the value in the MAR register for which a block designation has been given by the BLKDIR bit in DMACRA is restored in accordance with the DTSZ, SAID/DAID, and SAIDE/DAIDE bits in DMACR.

ETCRB is decremented by 1 after every block transfer, and when the count reaches H'0000 the DTE bit in DMABCRL is cleared and transfer ends. If the DTIE bit in DMABCRL is set to 1 at this point, an interrupt request is sent to the CPU or DTC.

8.4.6 Repeat Area Function

The EXDMAC has a function for designating a repeat area for source addresses and/or destination addresses. When a repeat area is designated, the address register values repeat within the range specified as the repeat area. Normally, when a ring buffer is involved in a transfer, an operation is required to restore the address register value to the buffer start address each time the address register value is the last address in the buffer (i.e. when ring buffer address overflow occurs), but if the repeat area function is used, the operation that restores the address register value to the buffer start address is performed automatically within the EXDMAC.

The repeat area function can be set independently for the source address register and the destination address register.

The source address repeat area is specified by bits SARA4 to SARA0 in EDACR, and the destination address repeat area by bits DARA4 to DARA0 in EDACR. The size of each repeat area can be specified independently.

When the address register value is the last address in the repeat area and repeat area overflow occurs, DMA transfer can be temporarily halted and an interrupt request sent to the CPU. If the SARIE bit in EDACR is set to 1, when the source address register overflows the repeat area, the IRF bit is set to 1 and the EDA bit cleared to 0 in EDMDR, and transfer is terminated. If EDIE = 1 in EDMDR, an interrupt is requested. If the DARIE bit in EDACR is set to 1, the above applies to the destination address register.

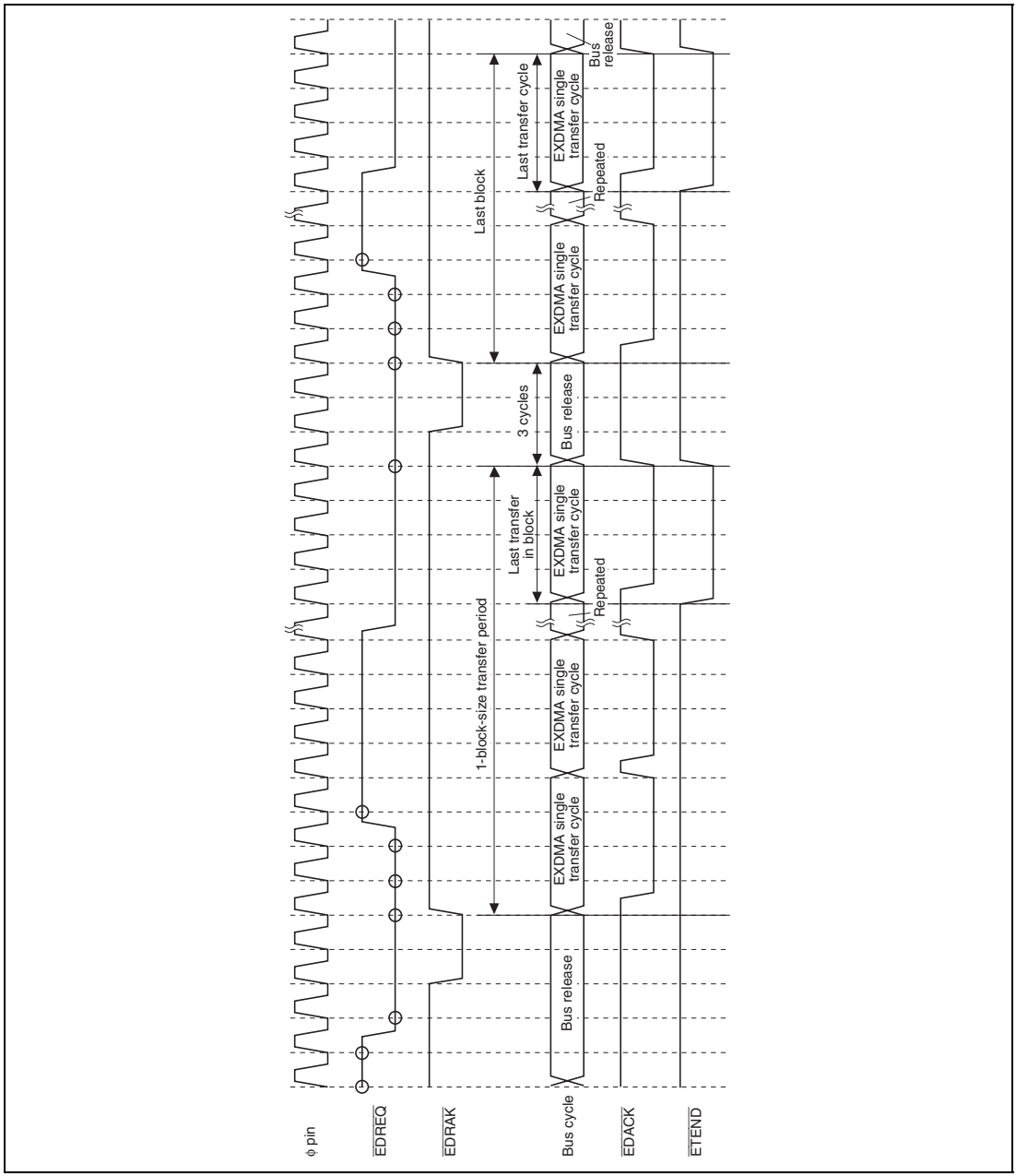

Figure 8.40 External Request/Cycle Steal Mode/Block Transfer Mode (No Contention/Single Address Mode/Falling Edge Sensing/BGUP = 0)

- P25/$\overline{\text{WAIT-B}}$/PO5-A/TIOCB4-A/TMO1-A

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bit WAITE in BCR of the bus controller, TPU channel 4 settings (by bits MD3 to MD0 in TMDR_4, bits IOB3 to IOB0 in TIOR_4, and bits CCLR1 and CCLR0 in TCR_4), bits OS3 to OS0 in TCSR_1 of the 8-bit timer, bit NDER5 in NDERL of the PPG, bits PPGS, TPUS, and TMRS in PFCR3, bit WAITS in PFCR4, and bit P25DDR.

- Modes 1, 2, and 4 Modes 3 and 7 (EXPE = 1)

WAITE	0					1
TPU channel 4 settings	(1) in table below	(2) in table below				—
OS3 to OS0	—	All 0			Not all 0	—
P25DDR	—	0	1	1	—	—
NDER5	—	—	0	1	—	—
Pin function	TIOCB4-A output*3	P25 input	P25 output	PO5-A output*2	TMO1-A output*4	$\overline{\text{WAIT-B}}$ input*5
		TIOCB4-A input*1*3				

- Modes 3 and 7 (EXPE = 0)

WAITE	—				
TPU channel 4 settings	(1) in table below	(2) in table below			
OS3 to OS0	—	All 0			Not all 0
P25DDR	—	0	0	1	1
NDER5	—	—	—	0	1
Pin function	TIOCB4-A output*3	P25 input	P25 output	PO5-A output*2	TIO1-A output*4
		TIOCB4-A input*1*3			

Notes: 1. TIOCB4-A input when MD3 to MD0 = B'0000 or B'01xx and IOB3 to IOB0 = B'10xx.
2. When using as PO5-A output, set PPGS in PFCR3 to 0 before other register setting.
3. When using as TIOCB4-A input/output, set TPUS in PFCR3 to 0 before other register setting.
4. When using as TMO1-A output, set TMRS in PFCR3 to 0 before other register setting.
5. $\overline{\text{WAIT-B}}$ input when the WAITS bit in PFCR4 is 1. Not used as $\overline{\text{WAIT-B}}$ input pin when WAITS is 0.

- PC1/A1/TIOCB9

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, TPU channel 9 settings (by bits MD3 to MD0 in TMDR_9, bits IOB3 to IOB0 in TIORH_9, and bits CCLR2 to CCLR0 in TCR_9), and bit PC1DDR.

Operating mode	1, 2	4 3, 7 (EXPE = 1)		3, 7 (EXPE = 0)		
TPU channel 9 settings	—	—		(1) in table below	(2) in table below	
PC1DDR	—	0	1	—	0	1
Pin function	A1 output	PC1 input	A1 output	TIOCB9 output	PC1 input	PC1 output
					TIOCB9 input*	

TPU channel 9 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

Note: * TIOCB9 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

11.10.3 Caution on Cycle Setting

When counter clearing by compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

$$f = \frac{\phi}{(N + 1)}$$

Where f: Counter frequency
ϕ: Operating frequency
N: TGR set value

11.10.4 Contention between TCNT Write and Clear Operations

If the counter clearing signal is generated in the T_2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed. Figure 11.46 shows the timing in this case.

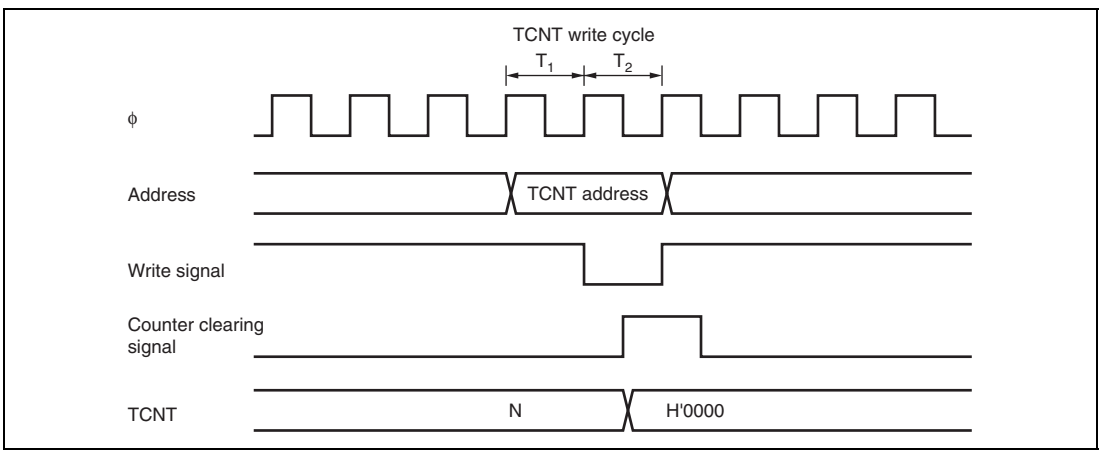

Figure 11.46 Contention between TCNT Write and Clear Operations

12.4.5 Sample Setup Procedure for Non-Overlapping Pulse Output

Figure 12.8 shows a sample procedure for setting up non-overlapping pulse output.

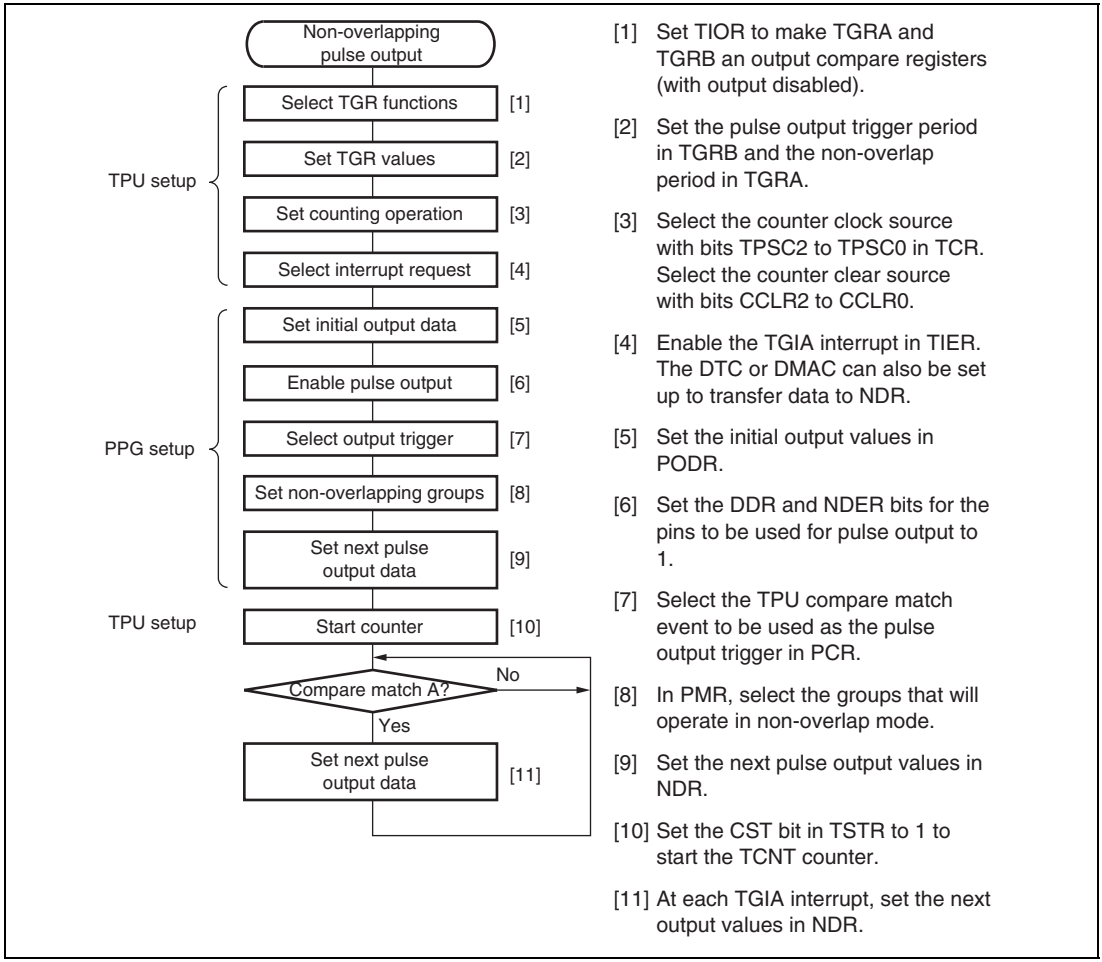

Figure 12.8 Setup Procedure for Non-Overlapping Pulse Output (Example)

13.5.2 Timing of CMFA and CMFB Setting when Compare-Match Occurs

The CMFA and CMFB flags in TCSR are set to 1 by a compare match signal generated when the TCOR and TCNT values match. The compare match signal is generated at the last state in which the match is true, just before the timer counter is updated. Therefore, when TCOR and TCNT match, the compare match signal is not generated until the next incrementation clock input. Figure 13.6 shows this timing.

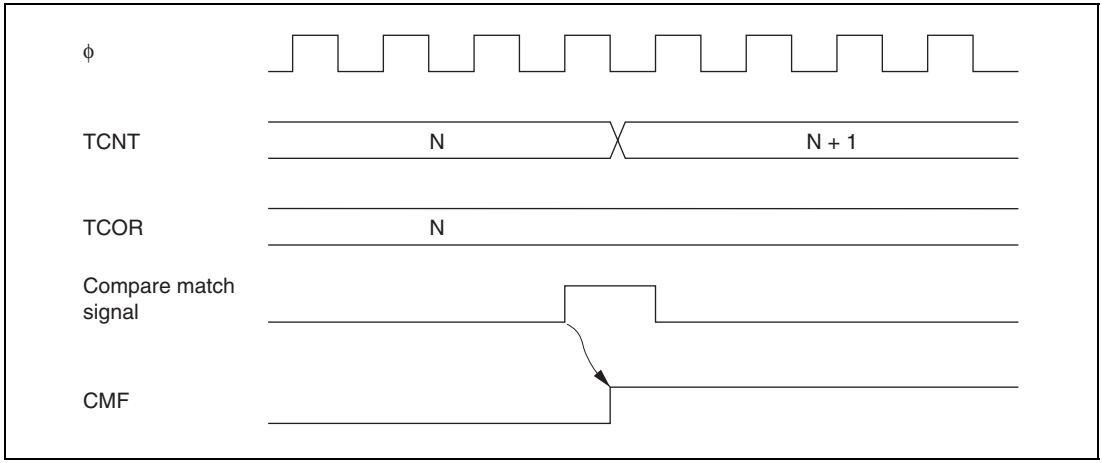

Figure 13.6 Timing of CMF Setting

14.4 Operation

14.4.1 Watchdog Timer Mode

To use the WDT as a watchdog timer mode, set the WT/$\overline{IT}$ and TME bits in TCSR to 1.

If TCNT overflows without being rewritten because of a system crash or other error, the $\overline{WDTOVF}$ signal is output.

This ensures that TCNT does not overflow while the system is operating normally. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflow occurs. This $\overline{WDTOVF}$ signal can be used to reset the chip internally in watchdog timer mode.

If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, a signal that resets this LSI internally is generated at the same time as the $\overline{WDTOVF}$ signal. If a reset caused by a signal input to the $\overline{RES}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{RES}$ pin reset has priority and the WOVF bit in RSTCSR is cleared to 0.

The $\overline{WDTOVF}$ signal is output for 132 states when RSTE = 1, and for 130 states when RSTE = 0. The internal reset signal is output for 518 states.

When TCNT overflows in watchdog timer mode, the WOVF bit in RSTCSR is set to 1. If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, an internal reset signal is generated to the entire chip.

15.6 Operation in Clocked Synchronous Mode

Figure 15.14 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses. One character of communication data consists of 8-bit data. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

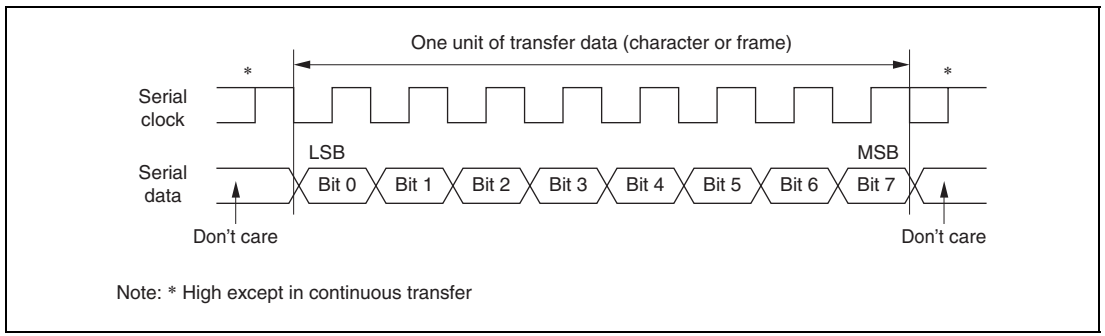

Figure 15.14 Data Format in Clocked Synchronous Communication (For LSB-First)

15.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the serial clock is output from the SCK pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

(1) Transmission

In transmission, the output signal (UART frame) from the SCI is converted to an IR frame by the IrDA interface (see figure 15.34).

When the serial data is 0, a high pulse of 3/16 the bit rate (interval equivalent to the width of one bit) is output (initial value). The high-level pulse can be varied according to the setting of bits IrCKS2 to IrCKS0 in IrCR.

In the specification, the high pulse width is fixed at a minimum of 1.41 µs, and a maximum of (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 µs. When system clock φ is 20 MHz, 1.6 µs can be set for a high pulse width with a minimum value of 1.41 µs.

When the serial data is 1, no pulse is output.

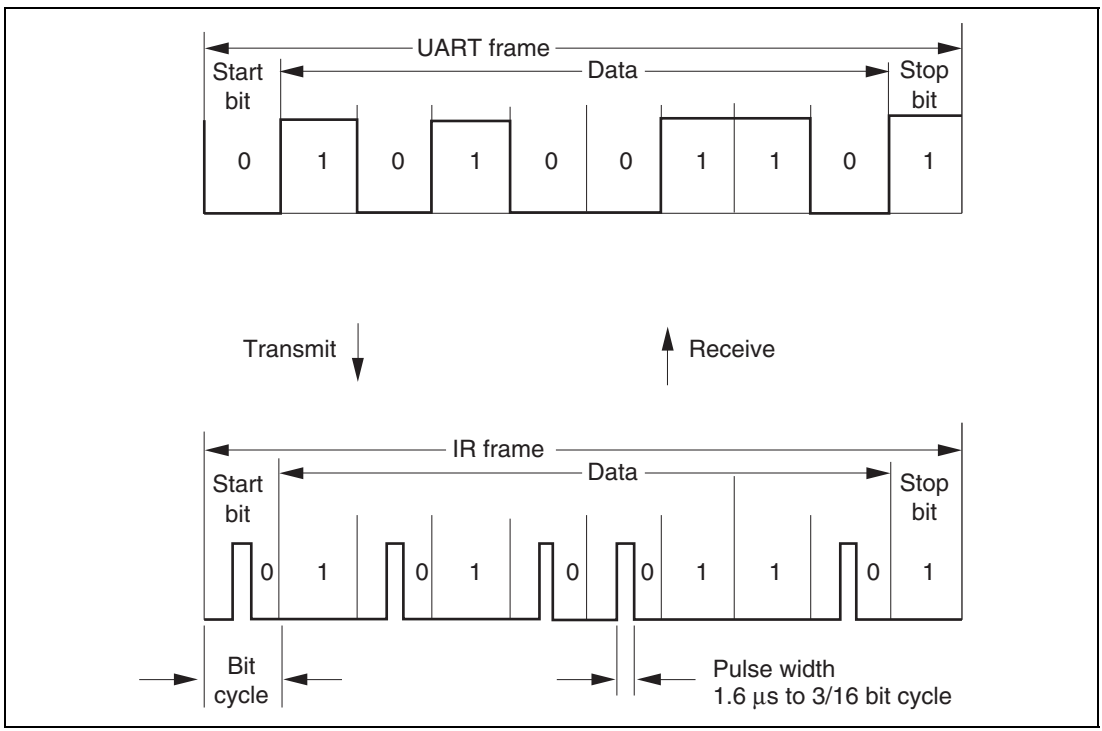

Figure 15.34 IrDA Transmit/Receive Operations

19.3.6 SS Control Register 2 (SSCR2)

SSCR2 is a register that enables/disables the open-drain outputs of the SSO, SSI, SSCK, and $\overline{SCS}$ pins, selects the assert timing of the $\overline{SCS}$ pin, data output timing of the SSO pin, and set timing of the TEND bit.

Bit	Bit Name	Initial Value	R/W	Description
7	SDOS	0	R/W	Serial Data Pin Open Drain Select Selects whether the serial data output pin is used as a CMOS or an NMOS open drain output. Pins to output serial data differ according to the register setting. For details, 19.4.3, Relationship between Data Input/Output Pins and Shift Register. 0: CMOS output 1: NMOS open drain output
6	SSCKOS	0	R/W	SSCK Pin Open Drain Select Selects whether the SSCK pin is used as a CMOS or an NMOS open drain output. 0: CMOS output 1: NMOS open drain output
5	SCSOS	0	R/W	$\overline{SCS}$ Pin Open Drain Select Selects whether the $\overline{SCS}$ pin is used as a CMOS or an NMOS open drain output. 0: CMOS output 1: NMOS open drain output
4	TENDSTS	0	R/W	Selects the timing of setting the TEND bit (valid in SSU and master mode). 0: Sets the TEND bit when the last bit is being transmitted 1: Sets the TEND bit after the last bit is transmitted

23.4 SDRAMϕ Clock Output Control

Output of the SDRAMϕ clock can be controlled by the SDPSTP bit in SCKCR. When the SDPSTP bit is set to 1, the SDRAMϕ clock stops at the end of the bus cycle and the pin can be used as a general port. SDRAMϕ clock output is enabled when the SDPSTP bit is cleared to 0 regardless of the DDR value. Table 23.5 shows the state of the SDRAMϕ pin in each processing state.

Note: The SDRAM interface is not supported by the H8S/2426 group and H8S/2424 group.

Table 23.5 SDRAMϕ Pin State in Each Processing State

Register Setting						
SDPSTP	DDR	Normal Operating State	Sleep Mode	Software Standby Mode	Hardware Standby Mode	All Module Clocks Stop Mode
0	X	SDRAMϕ output	SDRAMϕ output	Fixed low	High impedance	SDRAMϕ output
1	0	High impedance	High impedance	High impedance	High impedance	High impedance
1	1	PH1/CS5/RAS5 output	H1/CS5/RAS5 output	H1/CS5/RAS5 output	High impedance	H1/CS5/RAS5 output

Note: SDRAM is not available in the H8S/2426 and H8S/2424 Groups.
In these products, this pin functions as a general pin regardless of the SDPSTP bit setting.

Register Abbreviation	Reset	High-Speed	Clock Division	Sleep	Module Stop	All Module Clock Stop	Software Standby	Hardware Standby	Module
PCODR	Initialized	—	—	—	—	—	—	Initialized	PORT
PDODR	Initialized	—	—	—	—	—	—	Initialized	
PEODR	Initialized	—	—	—	—	—	—	Initialized	
PFODR	Initialized	—	—	—	—	—	—	Initialized	
PGODR	Initialized	—	—	—	—	—	—	Initialized	
PHODR	Initialized	—	—	—	—	—	—	Initialized	
PJODR	Initialized	—	—	—	—	—	—	Initialized	
ICCRA_0	Initialized	—	—	—	—	—	—	Initialized	IIC2_0
ICCRB_0	Initialized	—	—	—	—	—	—	Initialized	
ICMR_0	Initialized	—	—	—	—	—	—	Initialized	
ICIER_0	Initialized	—	—	—	—	—	—	Initialized	
ICSR_0	Initialized	—	—	—	—	—	—	Initialized	
SAR_0	Initialized	—	—	—	—	—	—	Initialized	
ICDRT_0	Initialized	—	—	—	—	—	—	Initialized	
ICDRR_0	Initialized	—	—	—	—	—	—	Initialized	
ICCRA_1	Initialized	—	—	—	—	—	—	Initialized	IIC2_1
ICCRB_1	Initialized	—	—	—	—	—	—	Initialized	
ICMR_1	Initialized	—	—	—	—	—	—	Initialized	
ICIER_1	Initialized	—	—	—	—	—	—	Initialized	
ICSR_1	Initialized	—	—	—	—	—	—	Initialized	
SAR_1	Initialized	—	—	—	—	—	—	Initialized	
ICDRT_1	Initialized	—	—	—	—	—	—	Initialized	
ICDRR_1	Initialized	—	—	—	—	—	—	Initialized	
ICCRA_2	Initialized	—	—	—	—	—	—	Initialized	IIC2_2
ICCRB_2	Initialized	—	—	—	—	—	—	Initialized	
ICMR_2	Initialized	—	—	—	—	—	—	Initialized	
ICIER_2	Initialized	—	—	—	—	—	—	Initialized	
ICSR_2	Initialized	—	—	—	—	—	—	Initialized	
SAR_2	Initialized	—	—	—	—	—	—	Initialized	
ICDRT_2	Initialized	—	—	—	—	—	—	Initialized	
ICDRR_2	Initialized	—	—	—	—	—	—	Initialized	

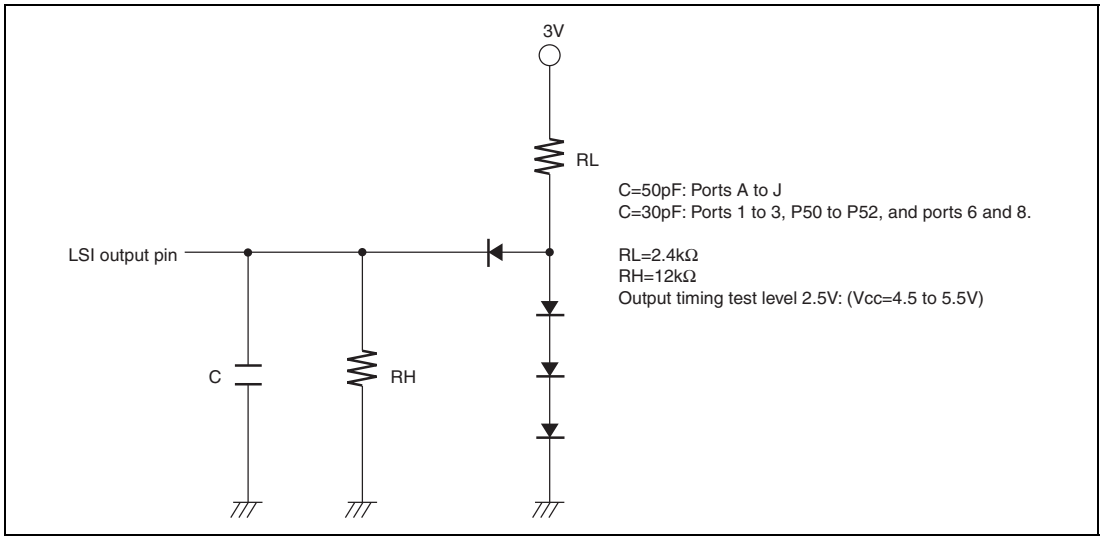

Figure 25.52 Output Load Circuit

(2) Control Signal Timing

Table 25.31 Control Signal Timing

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	ns	Figure 25.56
$\overline{RES}$ pulse width	t_{RESW}	2	—	ms	
NMI setup time	t_{NMIS}	150	—	ns	Figure 25.57
NMI hold time	t_{NMIH}	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—		

Notes: 1. When programming is to be performed multiple times on a system, reduce the effective number of programming operations by shifting the writing addresses in sequence and so on until the remaining blank area is as small as possible and only then erasing the entire block once. For example, if sets of 16 bytes are being programmed, erasing the block once after programming the maximum number of sets (256) minimizes the effective number of programming operations.

We recommend keeping information on the number of times erasure is performed for each block, and setting up the limit on the number of times.

2. If an erase error occurs during erasure, execute the clear status command and then the erase command at least 3 times until the erase does not recur.

*1. Determination of the number of times for programming/erasure operations.

Number of times programming/erasure is performed in each block.

When the number of times for programming/erasure operations is n (n = 100), data can be erased n times in each block.

For example, if programming of 4 bytes is done 1024 times, each at a different address in a 4-kbyte per block, and the block is then erased, this counts as programming/erasure one time.

However, programming of any location in a block multiple times is not possible (overwriting is prohibited).

*2. This is the number of times for which all electrical characteristics are guaranteed.