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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SSU, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24269nvfqv

Table 6.6 Relation between Settings of Bits MXC2 to MXC0 and Address Multiplexing

	DRAMCR			Shift Size	Address Pins																
	MXC2	MXC1	MXC0		A23 to A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Row address	0	0	0	8 bits	A23 to A16	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
			1	9 bits	A23 to A16	A15	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
		1	0	10 bits	A23 to A16	A15	A14	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			1	11 bits	A23 to A16	A15	A14	A13	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
	1	×	×	Reserved (setting prohibited)																	
Column address	0	×	×	—	A23 to A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	1	×	×	Reserved (setting prohibited)																	

[Legend]

×: Don't care.

6.7.3 Data Bus

If a bit in ABWCR corresponding to an area designated as DRAM space is set to 1, that area is designated as 8-bit DRAM space; if the bit is cleared to 0, the area is designated as 16-bit DRAM space. In 16-bit DRAM space, ×16-bit configuration DRAM can be connected directly.

In 8-bit DRAM space the upper half of the data bus, D15 to D8, is enabled, while in 16-bit DRAM space both the upper and lower halves of the data bus, D15 to D0, are enabled.

Access sizes and data alignment are the same as for the basic bus interface: see section 6.5.1, Data Size and Data Alignment.

The setting of bits TPC1 and TPC0 is also valid for T_p states in refresh cycles.

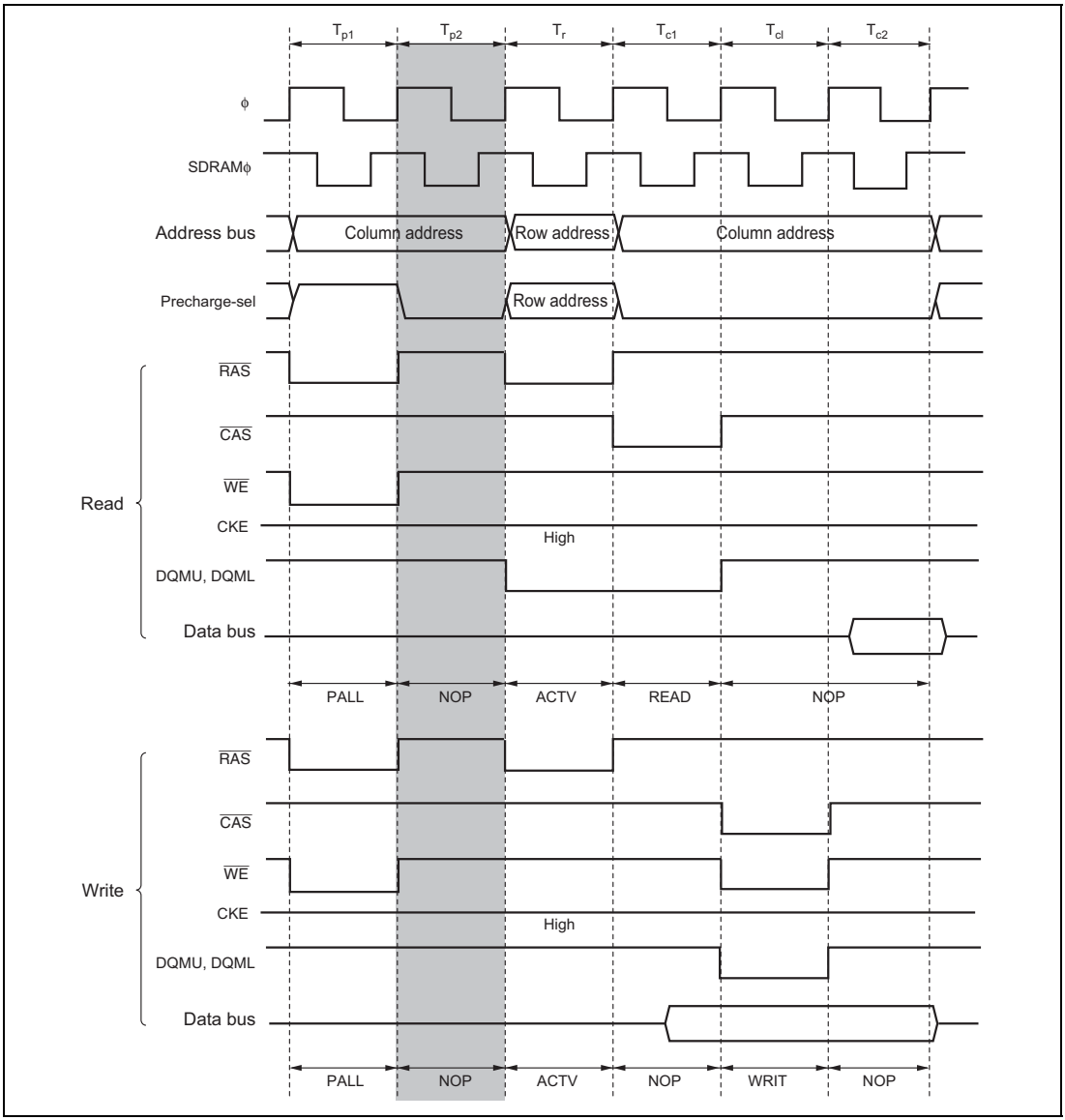

Figure 6.59 Example of Timing with Two-State Precharge Cycle (TPC1 = 0, TPC0 = 1, SDWCD = 0, CAS Latency 2)

Previous Access	Next Access	ICIS2	ICIS1	ICIS0	DRMI	IDLC	Idle cycle
Normal space write	Normal space read	0	—	—	—	—	Disabled
		1	—	—	—	0	1 state inserted
						1	2 states inserted
	DRAM*1/continuous synchronous DRAM*2 space read	0	—	—	—	—	Disabled
		1	—	—	—	0	1 state inserted
						1	2 states inserted
DRAM*1/continuous synchronous DRAM*2 space write	Normal space read	0	—	—	—	—	Disabled
		1	—	—	—	0	1 state inserted
						1	2 states inserted
	DRAM*1/continuous synchronous DRAM*2 space read	0	—	—	—	—	Disabled
		1	—	—	—	0	1 state inserted
						1	2 states inserted

Notes: 1. The DRAM interface is not supported by the 5-V version.
2. Not supported by the H8S/2426 Group and H8S/2424 Group.

Figure 7.9 illustrates operation in single address mode (when sequential mode is specified).

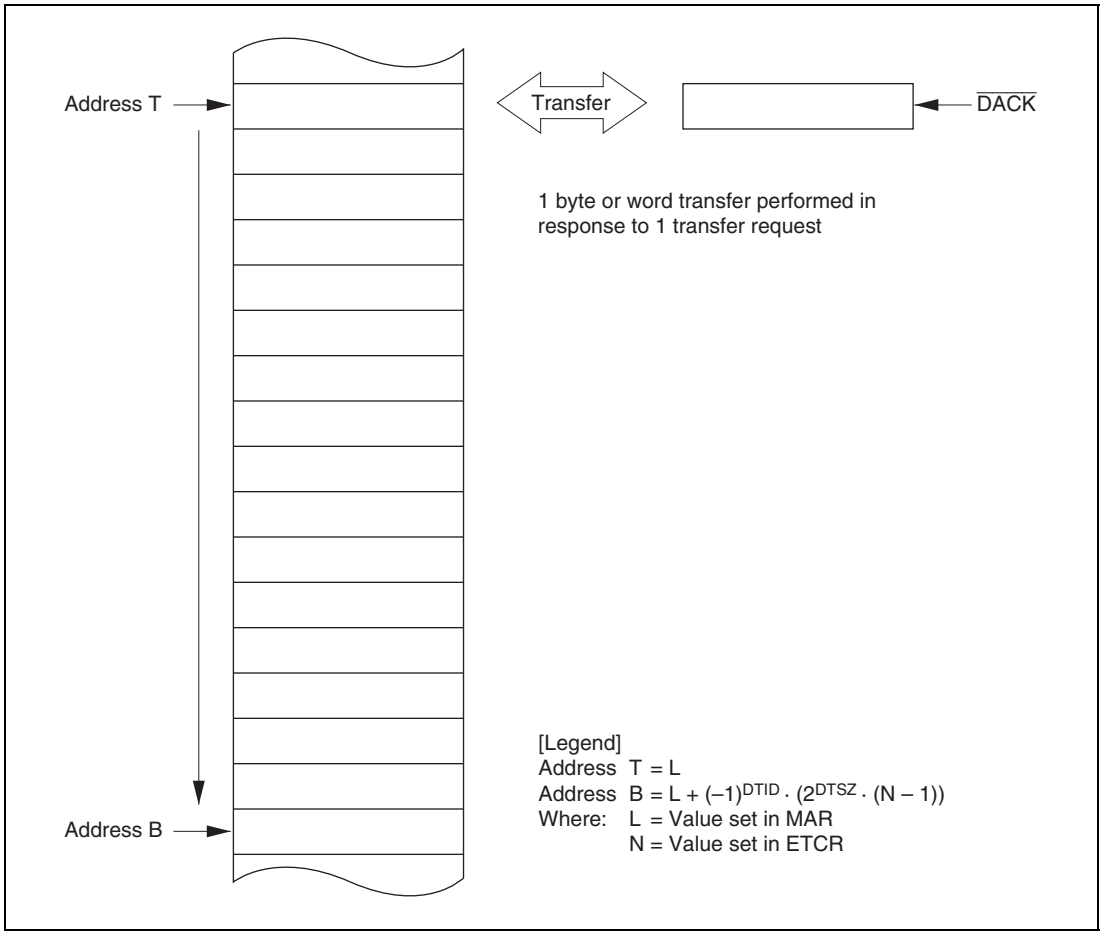

Figure 7.9 Operation in Single Address Mode (When Sequential Mode Is Specified)

Bit	Bit Name	Initial Value	R/W	Description
7	DAT1	0	R/W	Destination Address Update Mode
6	DAT0	0	R/W	These bits specify incrementing/decrementing of the transfer destination address (EDDAR). When an external device with DACK is designated as the transfer destination in single address mode, the specification by these bits is ignored. 0x: Fixed 10: Incremented (+1 in byte transfer, +2 in word transfer) 11: Decremented (–1 in byte transfer, –2 in word transfer)
5	DARIE	0	R/W	Destination Address Repeat Interrupt Enable When this bit is set to 1, in the event of destination address repeat area overflow the IRF bit is set to 1 and the EDA bit cleared to 0 in EDMDR, and transfer is terminated. If the EDIE bit in EDMDR is 1 when the IRF bit in EDMDR is set to 1, an interrupt request is sent to the CPU. When used together with block transfer mode, a destination address repeat interrupt is requested at the end of a block-size transfer. If the EDA bit is set to 1 in EDMDR for the channel on which transfer is terminated by a destination address repeat interrupt, transfer can be resumed from the state in which it ended. If a destination address repeat area has not been designated, this bit is ignored. 0: Destination address repeat interrupt is not requested 1: When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

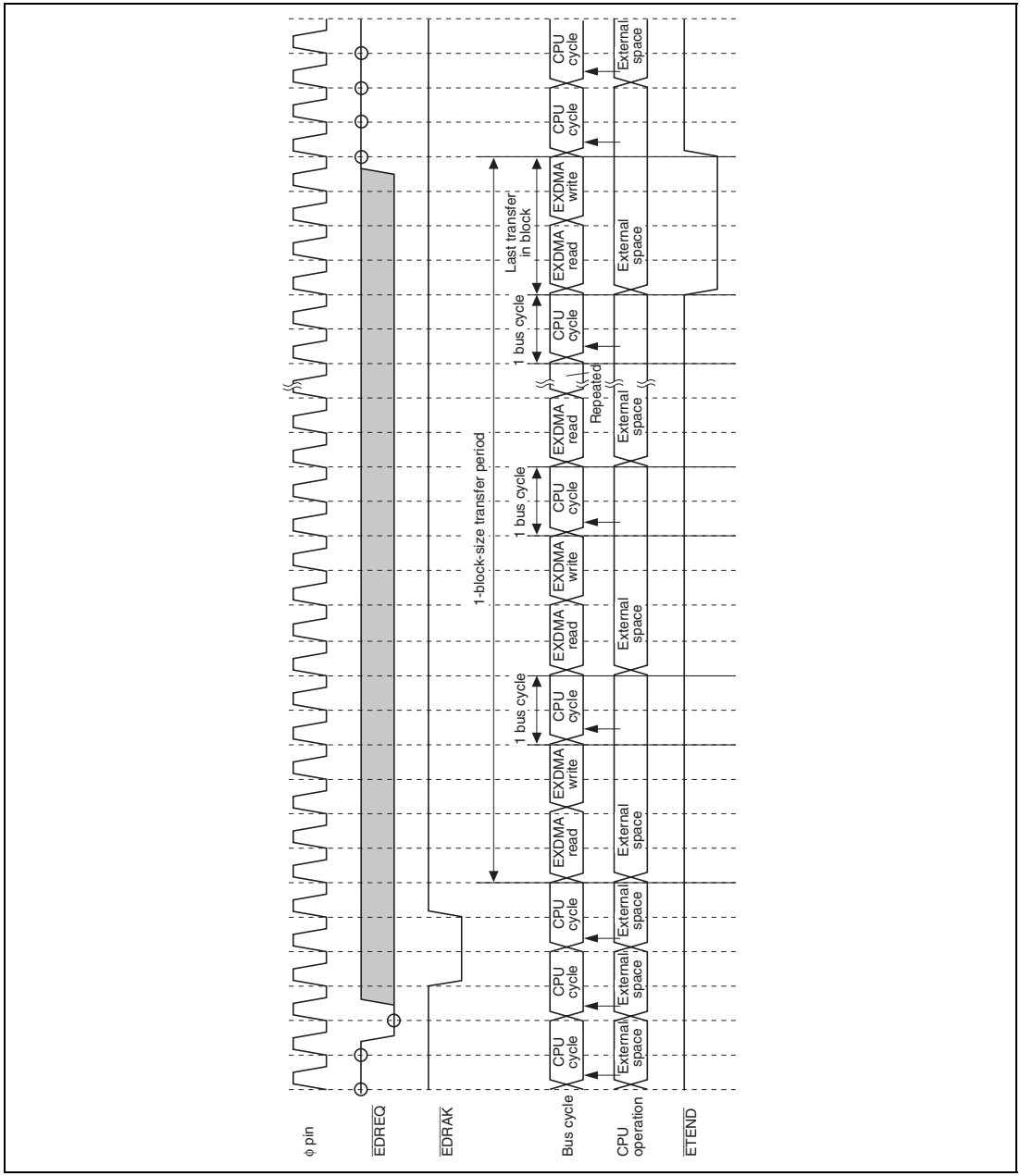

Figure 8.42 External Request/Cycle Steal Mode/Block Transfer Mode (CPU Cycles/Dual Address Mode/Low Level Sensing/BGUP = 1)

SSU settings	(1)	(2)	(1)	(2)	(1)	(3)	(3)	(2)	(3)	(2)	(3)	(1)	(3)	(3)	(1)	(3)	(3)
SSUMS	0							0				1*1					
BIDE	0							1*2				0					
MSS	0				1			0		1		0			1		
TE	0		1		0	1		0	1	0	1	0	1		0	1	
RE	0	1	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1
Pin state	—	SSO input	—	SSO input	—	SSO output	SSO output	SSO input	SSO output	SSO input	SSO output	—	SSO output	SSO output	—	SSO output	SSO output

[Legend]

—: Not used as the SSU pin (can be used as an I/O port).

Notes: See tables 19.4 to 19.6.

1. Do not set BIDE to 1 when SSUMS = 1 in SSU.
2. Do not specify that TE = RE = 1 when operating with BIDE = 1 (bidirectional mode).

- P13/$\overline{\text{TEND1}}$/PO11/TIOCD0/TCLKB

  The pin function is switched as shown below according to the combination of bit TEE1 in DMATCR of the DMAC, TPU channel 0 settings (by bits MD3 to MD0 in TMDR_0, bits IOD3 to IOD0 in TIORL_0, and bits CCLR2 to CCLR0 in TCR_0), bits TPSC2 to TPSC0 in TCR_0 to TCR_2, bit NDER11 in NDERH of the PPG, and bit P13DDR.

TEE1	0				1
TPU channel 0 settings	(1) in table below	(2) in table below			—
P13DDR	—	0	1	1	—
NDER11	—	—	0	1	—
Pin function	TIOCD0 output	P13 input	P13 output	PO11 output	$\overline{\text{TEND1}}$ output
		TIOCD0 input*1			
	TCLKB input*2				

Notes: 1. TIOCD0 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

2. TCLKB input when the setting for any of TCR_0 to TCR_2 is TPSC2 to TPSC0 = B'101. TCLKB input when phase counting mode is set for channels 1 and 5.

TPU channel 3 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000, B'0100, B'1xxx	B'0001 to B'0011, B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

[Legend]

x: Don't care

Notes: 1. TIOCA4-A input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.
2. TIOCB4 output disabled.
3. When using as PO4-A output, set PPGS in PFCR3 to 0 before other register setting.
4. When using as TIOCA4-A input/output, set TPUS in PFCR3 to 0 before other register setting.
5. When using as TMO0-A output, set TMRS in PFCR3 to 0 before other register setting.
6. When using as RxD4-A input, set RXD4S in PFCR4 to 0 before other register setting.

10.4 Port 4

Port 4 is an 8-bit input-only port that also has other functions, such as analog input pins. Port 4 has the following register.

- Port 4 register (PORT4)

10.4.1 Port 4 Register (PORT4)

PORT4 is an 8-bit read-only register that shows the pin states of port 4. PORT4 cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P47	—*	R	The pin states are always read from this register.
6	P46	—*	R	
5	P45	—*	R	
4	P44	—*	R	
3	P43	—*	R	
2	P42	—*	R	
1	P41	—*	R	
0	P40	—*	R	

Note: * Determined by the states of pins P47 to P40.

10.4.2 Pin Functions

Port 4 also functions as the pins for A/D converter analog inputs and interrupt inputs (the H8S/2424 Group). The correspondence between pins is as follows.

(1) Pin Functions of H8S/2426 Group and H8S/2426R Group

- P40/AN0_0, P41/AN1_0, P42/AN2_0, P43/AN3_0, P44/AN4_0, P45/AN5_0, P46/AN6_0, P47/AN7_0

Pin function	ANn_0 input

[Legend]
n = 7 to 0

10.5.5 Pin Functions

Port 5 pins also function as the pins for SCI I/Os, A/D converter inputs, interrupt inputs, I^2C I/Os, bus control signal I/Os, PPG outputs, TPU I/Os, and 8-bit timer I/Os. The correspondence between the register specification and the pin functions is shown below.

- P53/$\overline{\text{IRQ3-A}}$/$\overline{\text{ADTRG0-A}}$

  The pin function is switched as shown below according to the combination of bits TRGS1, TRGS0, and EXTRGS in ADCR_0 of the ADC, bit P53DDR, and bit ITS3 in ITSR of the interrupt controller.

P53DDR	0	1
Pin function	P53 input	P53 output
	$\overline{\text{ADTRG0-A}}$ input*1	
	$\overline{\text{IRQ3-A}}$ interrupt input*2	

Notes: 1. $\overline{\text{ADTRG0-A}}$ input when the EXTRGS bit in ADCR0 is 0, and TRGS1 = TRGS0 = 1.
2. $\overline{\text{IRQ3-A}}$ input when the ITS3 bit in ITSR is 0.

SSU settings	(2)	(1)	(2)	(4)	(3)	(1)
SSUMS	0					1
MSS	0	1				x
CSS1	x	0		1		x
CSS0	x	0	1	0	1	x
Pin state	$\overline{SCS}$ input	—	$\overline{SCS}$ input	Automatic $\overline{SCS}$ I/O	$\overline{SCS}$ output	—

[Legend]

x: Don't care

—: Not used as the SSU pin (can be used as an I/O port).

Note: See tables 19.4 to 19.6.

Section 18 D/A Converter

18.1 Features

D/A converter features are listed below.

- 8-bit resolution
- Output channels: Two channels
- Maximum conversion time of 10 μs (with 20 pF load)
- Output voltage of 0 V to Vref
- D/A output hold function in software standby mode
- Module stop state can be set.

18.2 Input/Output Pins

Table 18.1 shows the pin configuration of the D/A converter.

Table 18.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power pin	AV_{CC}	Input	Analog power
Analog ground pin	AV_{SS}	Input	Analog ground
Reference voltage pin	Vref	Input	Reference voltage of D/A converter
Analog output pin 2	DA2	Output	Channel 2 analog output
Analog output pin 3	DA3	Output	Channel 3 analog output

Bit	Bit Name	Initial Value	R/W	Description
3	SCSATS	0	R/W	Selects the assertion timing of the $\overline{SCS}$ pin (valid in SSU and master mode). 0: Min. values of t_{LEAD} and t_{LAG} are $1/2 \times t_{SUcyc}$ 1: Min. values of t_{LEAD} and t_{LAG} are $3/2 \times t_{SUcyc}$
2	SSODTS	0	R/W	Selects the data output timing of the SSO pin (valid in SSU and master mode) 0: While BIDE = 0, MSS = 1, and TE = 1 or while BIDE = 1, TE = 1, and RE = 0, the SSO pin outputs data 1: While BIDE = 0, MSS = 1, and TE = 1 or while BIDE = 1, TE = 1, and RE = 0, the SSO pin outputs data while the SCS pin is driven low
1, 0	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

(12) User ROM Sum Check

The boot program will add all the data bytes in the user ROM area and return the result in response to a user ROM sum check command.

Command	H'4B

- Command, H'4B, (1 byte): Sum check for user ROM

Response	H'5B	Size	Checksum of user ROM	SUM

- Response, H'5B, (1 byte): Response to the user ROM sum check
- Size (1 byte): The number of bytes that represents the checksum
  This is fixed to 4.
- Checksum of user ROM (4 bytes): Result of checksum calculation for the user ROM area; the total of all the data in the ROM, in byte units.
- SUM (1 byte): Sum check for data being transmitted

(13) Data Flash Sum Check

The boot program will add all the data bytes in the data flash area and return the result in response to a data flash sum check command.

Command	H'61

- Command, H'61, (1 byte): Sum check for data flash

Response	H'71	Size	Checksum of data flash	SUM

- Response, H'71, (1 byte): Response to the data flash sum check
- Size (1 byte): The number of bytes that represents the checksum
  This is fixed to 4.
- Checksum of data flash (4 bytes): Result of checksum calculation for the data flash area; the total of all the data in the data flash, in byte units.
- SUM (1 byte): Checksum value that makes the sum of the bytes from the command to the SUM byte become H'00.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TCR_11	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_11
TMDR_11	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_11	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_11	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_11	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_11	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_11	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_11	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
P1ODR	P17ODR	P16ODR	P15ODR	P14ODR	P13ODR	P12ODR	P11ODR	P10ODR	PORT
P2ODR	P27ODR	P26ODR	P25ODR	P24ODR	P23ODR	P22ODR	P21ODR	P20ODR	
P5ODR	—	—	—	—	P53ODR	P52ODR	P51ODR	P50ODR	
P6ODR	—	—	P65ODR	P64ODR	P63ODR	P62ODR	P61ODR	P60ODR	
P8ODR	—	—	P85ODR	P84ODR	P83ODR	P82ODR	P81ODR	P80ODR	
PBODR	PB7ODR	PB6ODR	PB5ODR	PB4ODR	PB3ODR	PB2ODR	PB1ODR	PB0ODR	
PCODR	PC7ODR	PC6ODR	PC5ODR	PC4ODR	PC3ODR	PC2ODR	PC1ODR	PC0ODR	
PDODR	PD7ODR	PD6ODR	PD5ODR	PD4ODR	PD3ODR	PD2ODR	PD1ODR	PD0ODR	
PEODR	PE7ODR	PE6ODR	PE5ODR	PE4ODR	PE3ODR	PE2ODR	PE1ODR	PE0ODR	
PFODR	PF7ODR	PF6ODR	PF5ODR	PF4ODR	PF3ODR	PF2ODR	PF1ODR	PF0ODR	
PGODR	—	PG6ODR	PG5ODR	PG4ODR	PG3ODR	PG2ODR	PG1ODR	PG0ODR	
PHODR	—	—	—	—	PH3ODR	PH2ODR	PH1ODR	PH0ODR	
PJODR	—	—	—	—	—	—	PJ1ODR	PJ0ODR	
ICCRA_0	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0	IIC2_0
ICCRB_0	BBSY	SCP	SDAO	—	SCLO	—	IICRST	—	
ICMR_0	—	WAIT	—	—	BCWP	BC2	BC1	BC0	
ICIER_0	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT	
ICSR_0	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ	
SAR_0	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	—	
ICDRT_0	ICDRT7	ICDRT6	ICDRT5	ICDRT4	ICDRT3	ICDRT2	ICDRT1	ICDRT0	
ICDRR_0	ICDRR7	ICDRR6	ICDRR5	ICDRR4	ICDRR3	ICDRR2	ICDRR1	ICDRR0	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
FLMCR1	—	CBIDB	—	—	—	—	—	FMCMDEN	FLASH
FLMDBPR	—	—	—	—	—	—	—	FMDBPT0	
FLMSTR	—	—	FMERSF	—	FMPRSF	—	—	FMRDY	
ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	BSC
ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0	
WTCRAH	—	W72	W71	W70	—	W62	W61	W60	
WTCRAL	—	W52	W51	W50	—	W42	W41	W40	
WTCRBH	—	W32	W31	W30	—	W22	W21	W20	
WTCRBL	—	W12	W11	W10	—	W02	W01	W00	
RDNCR	RDN7	RDN6	RDN5	RDN4	RDN3	RDN2	RDN1	RDN0	
CSACRH	CSXH7	CSXH6	CSXH5	CSXH4	CSXH3	CSXH2	CSXH1	CSXH0	
CSACRL	CSXT7	CSXT6	CSXT5	CSXT4	CSXT3	CSXT2	CSXT1	CSXT0	
BROMCRH	BSRM0	BSTS02	BSTS01	BSTS00	—	—	BSWD01	BSWD00	
BROMCRL	BSRM1	BSTS12	BSTS11	BSTS10	—	—	BSWD11	BSWD10	
BCR	BRLE	BREQOE	—	IDLC	ICIS1	ICIS0	WDBE	WAITE	
	—	—	—	—	—	ICIS2	—	—	
MPXCR	MPXE	—	—	—	—	—	—	ADDEX	
DRAMCR	OEE	RAST	—	CAST	—	RMTS2	RMTS1	RMTS0	
	BE	RCDM	DDS	EDDS	—	MXC2	MXC1	MXC0	
DRACCR	DRMI	—	TPC1	TPC0	SDWCD	—	RCD1	RCD0	
	—	—	—	—	CKSPE	—	RDXC1	RDXC0	
REFCR	CMF	CMIE	RCW1	RCW0	—	RTCK2	RTCK1	RTCK0	
	RFSHE	CBRM	RLW1	RLW0	SLFRF	TPCS2	TPCS1	TPCS0	
RTCNT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
RTCOR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Item			Symbol	Min.	Max.	Unit	Test Conditions
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 25.40
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 25.42
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 25.41
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 25.43
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{cyc}	Figure 25.44
		Synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	1.5	t_{cyc}	
	Input clock falling time		t_{SCKf}	—	1.5		
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 25.45
	Receive data setup time (synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	ns	Figure 25.46
IIC2	SCL input cycle time		t_{SCL}	12 t_{cyc} +600	—	ns	Figure 25.47
	SCL input high pulse width		t_{SCLH}	3 t_{cyc} +300	—	ns	
	SCL input low pulse width		t_{SCLL}	5 t_{cyc} +300	—	ns	
	SCL, SDA Input falling time		t_{Sf}	—	300	ns	
	SCL, SDA Input spike pulse removal time		t_{SP}	—	1 t_{cyc}	ns	
	SDA input bus free time		t_{BUF}	5 t_{cyc}	—	ns	
	Start condition input hold time		t_{STAH}	3 t_{cyc}	—	ns	
	Retransmit start condition input setup time		t_{STAS}	3 t_{cyc}	—	ns	
	Stop condition input setup time		t_{STOS}	3 t_{cyc}	—	ns	
	Data input setup time		t_{SDAS}	1 t_{cyc} +20	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		Cb	—	400	pF	
	SCL, SDA falling time		t_{Sf}	—	300	ns	

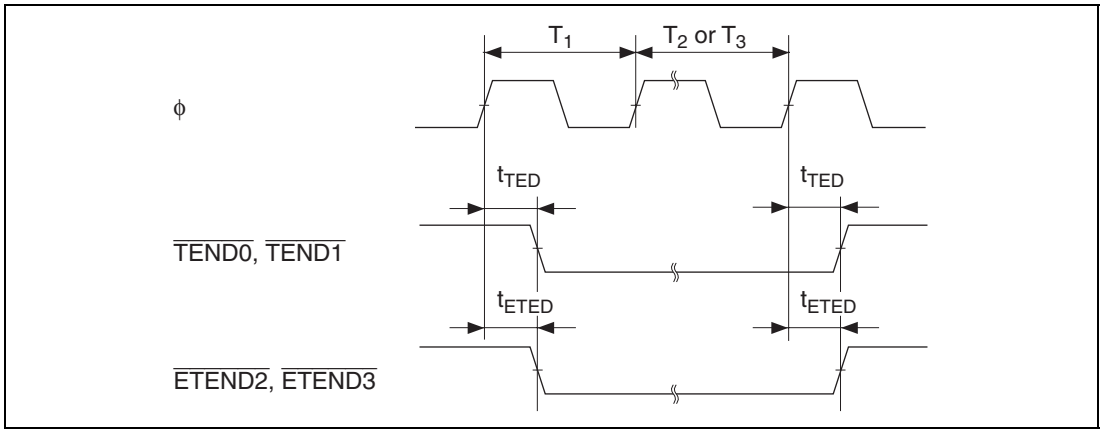

Figure 25.33 DMAC and EXDMAC, TEND/ETEND Output Timing

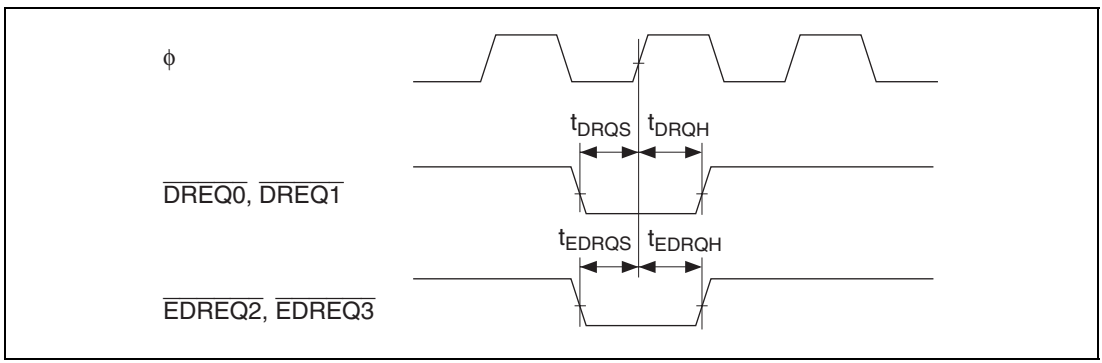

Figure 25.34 DMAC and EXDMAC, DREQ/EDREQ Input Timing

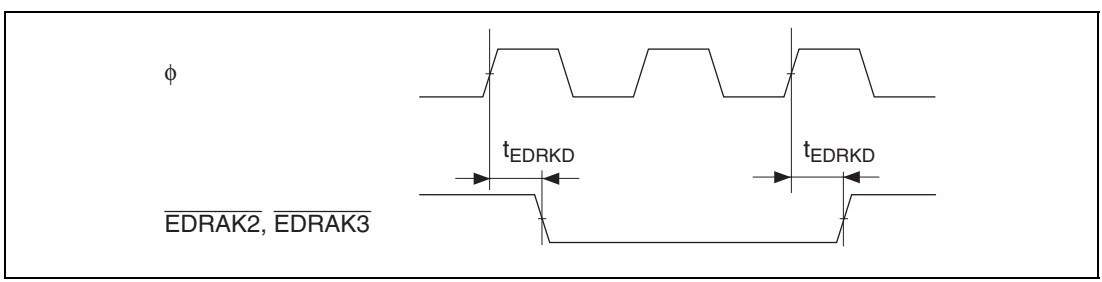

Figure 25.35 EXDMAC, EDRAK Output Timing

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