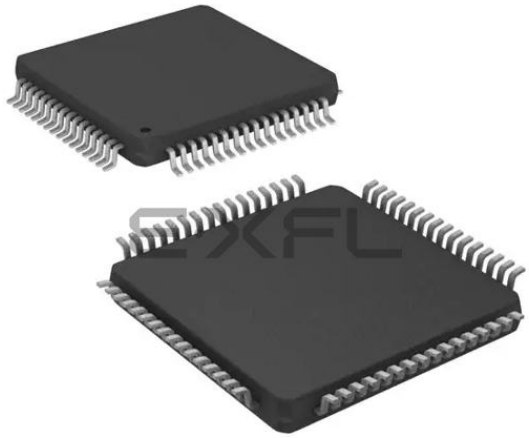

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg332f1024-qfp64

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG332 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32GG332F512G-E-QFP64	512	128	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32GG332F1024G-E-QFP64	1024	128	48	1.98 - 3.8	-40 - 85	TQFP64

Adding the suffix 'R' to the part number (e.g. EFM32GG332F512G-E-QFP64R) denotes tape and reel.

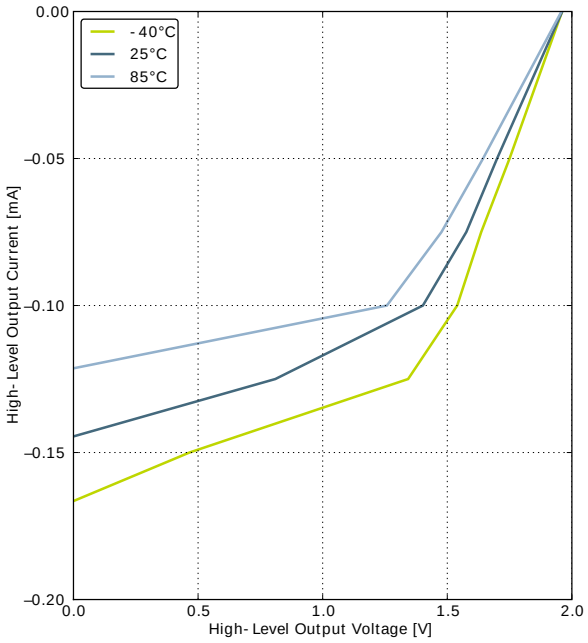
Visit **www.silabs.com** for information on global distributors and representatives.

Table 3.5. Power Management

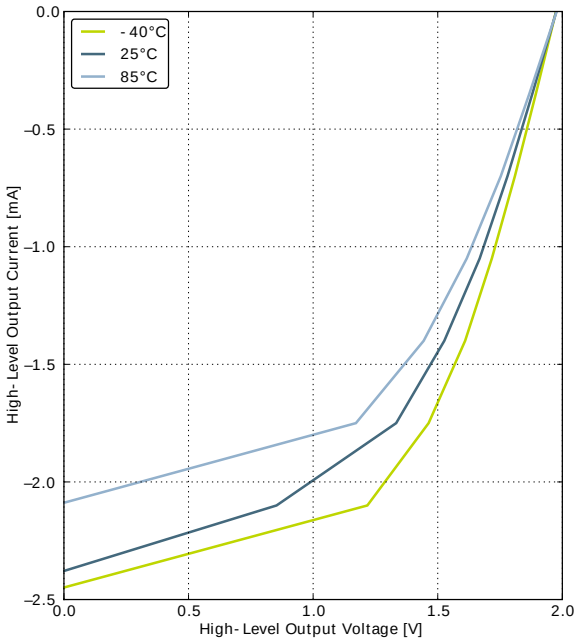
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.74		1.98	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.57		1.70	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF
C_{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		µF
C_{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		µF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V_{DD}			V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V_{DD}			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V_{DD}		V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.20V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}		±0.1	±40	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.10V_{DD}			V

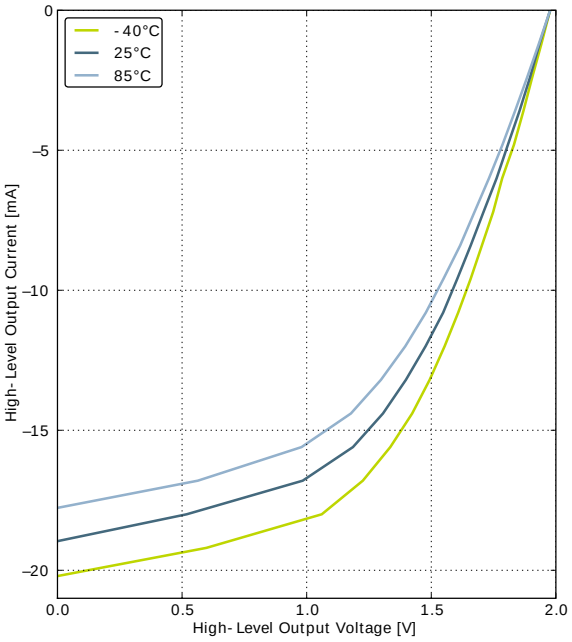
Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



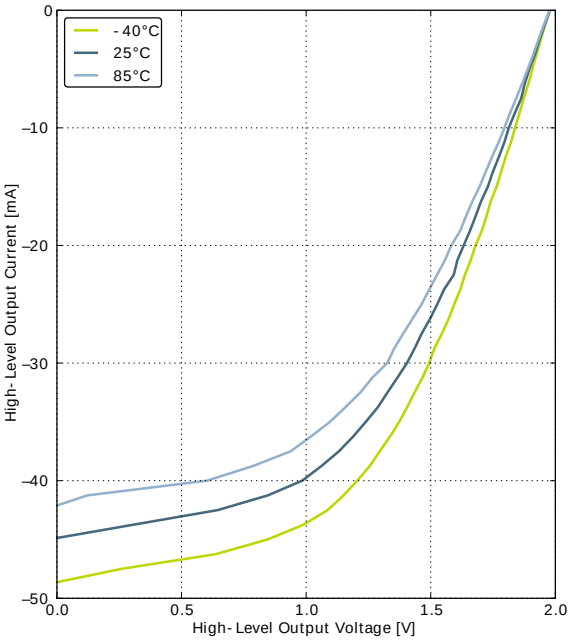
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

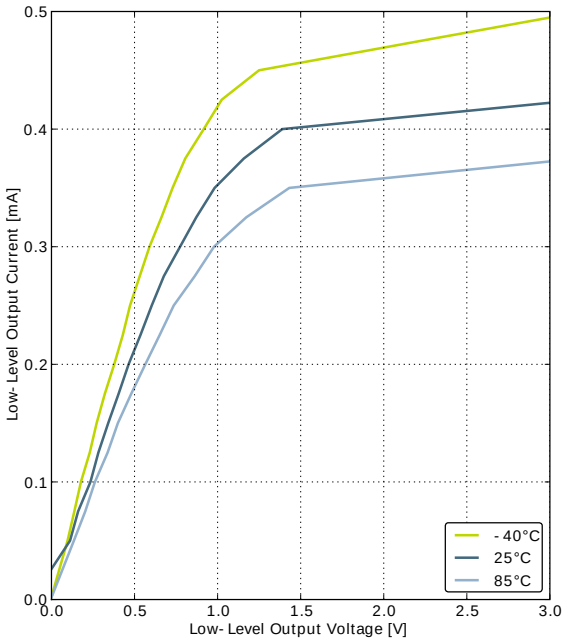


GPIO_Px_CTRL DRIVEMODE = STANDARD

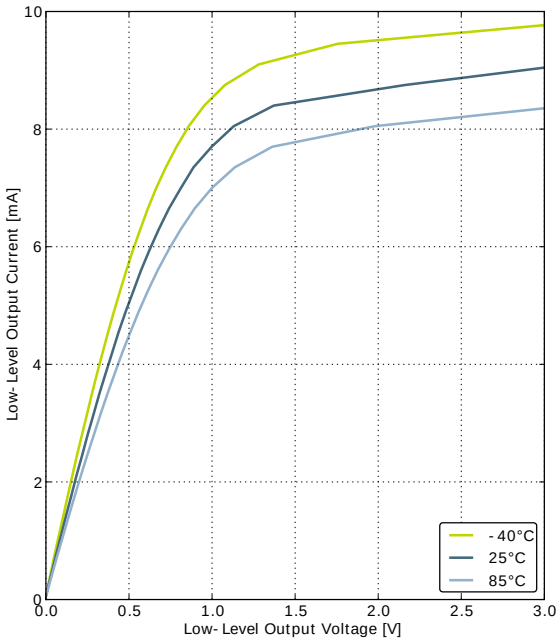


GPIO_Px_CTRL DRIVEMODE = HIGH

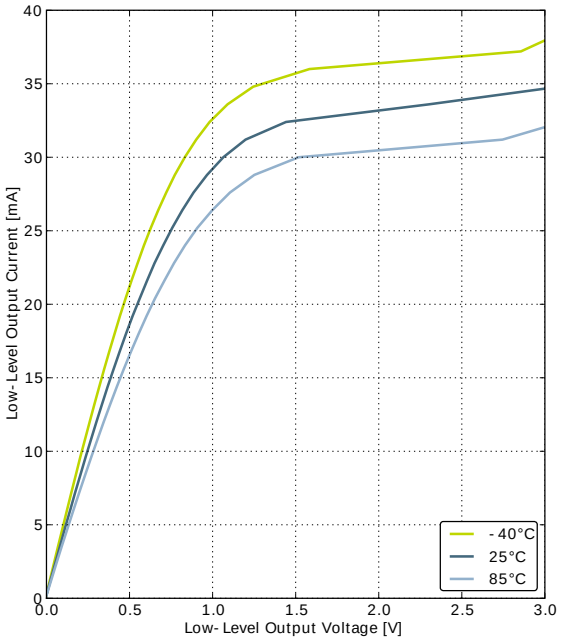
Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



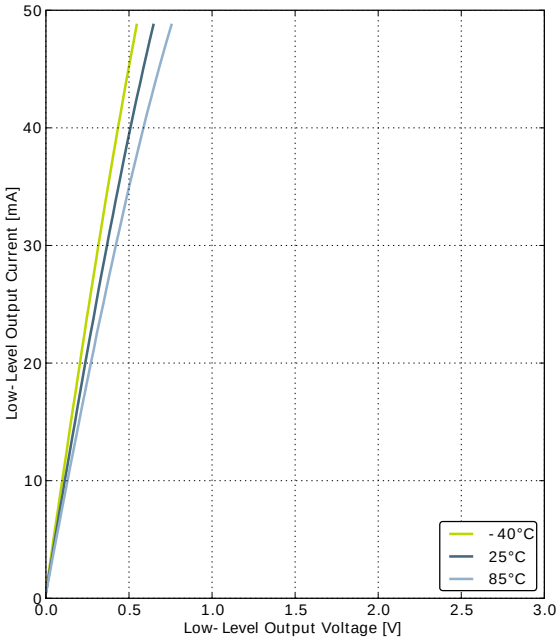
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1]See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

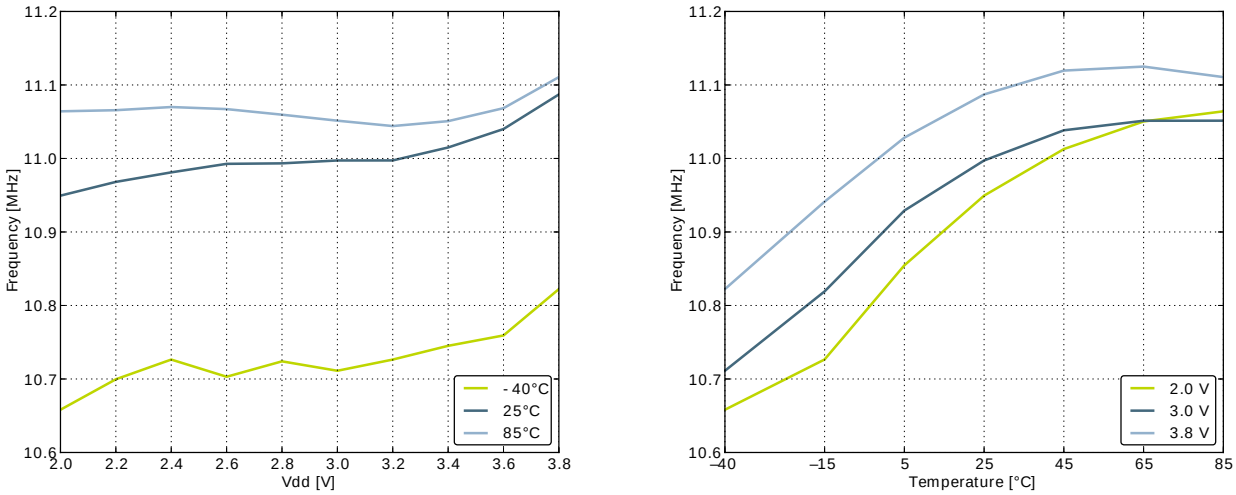


Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

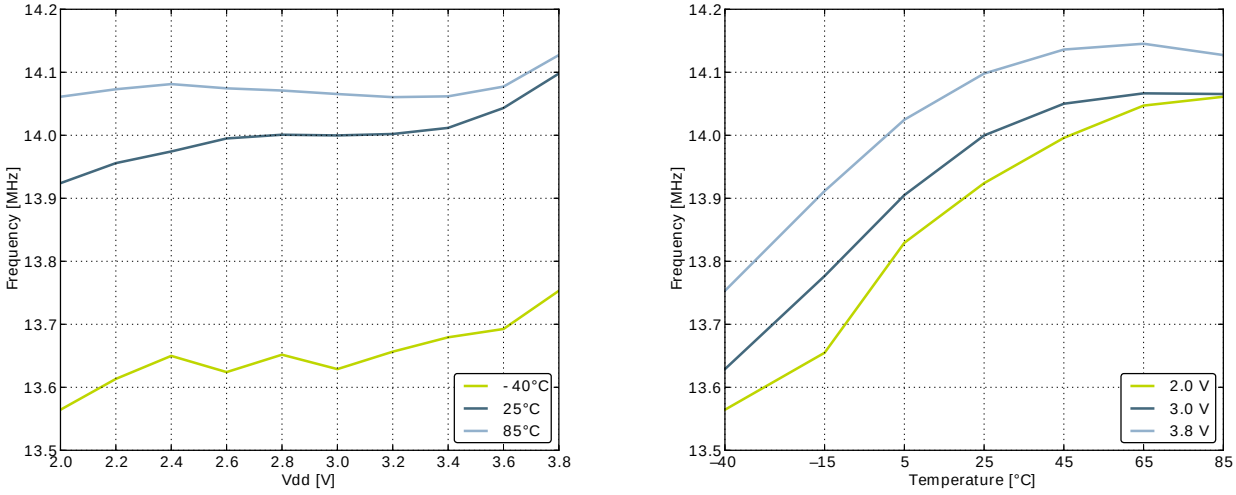
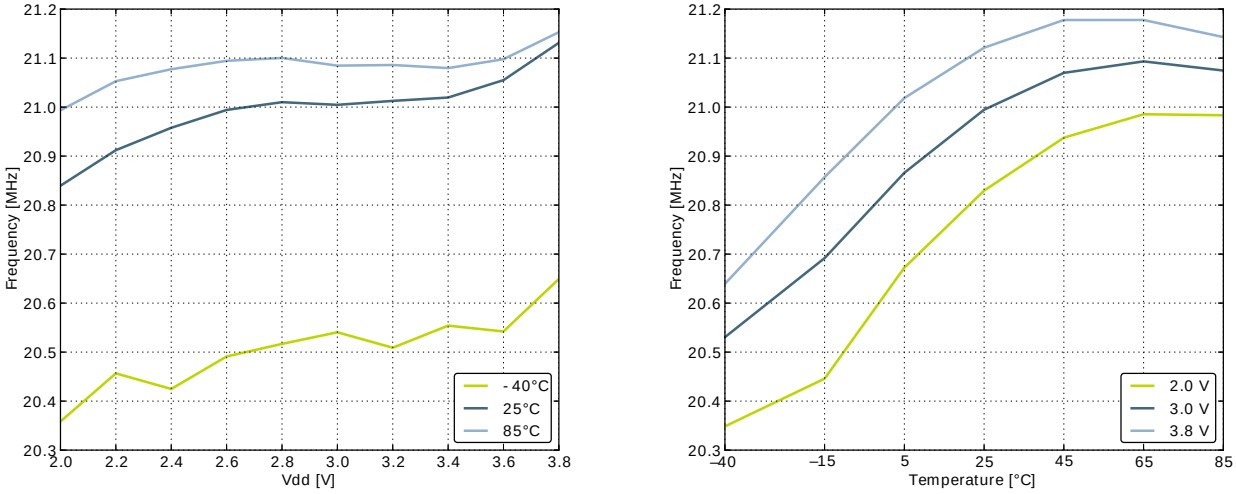


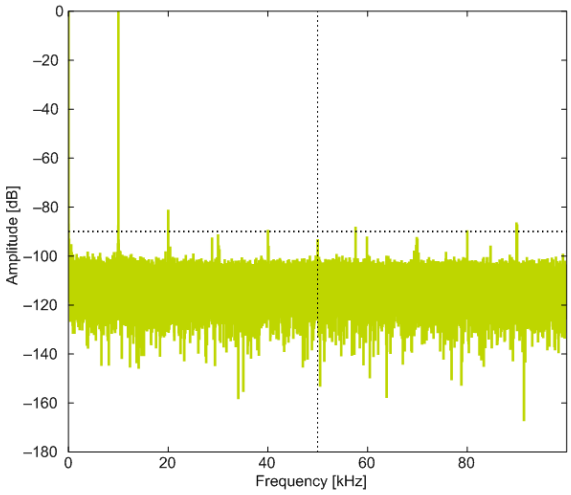
Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature



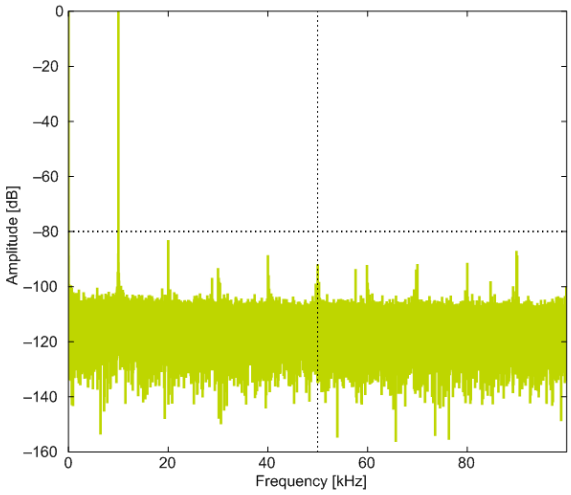
Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADCCLK Cycles
		8 bit	11			ADCCLK Cycles
		12 bit	13			ADCCLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADCCLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB

3.10.1 Typical performance

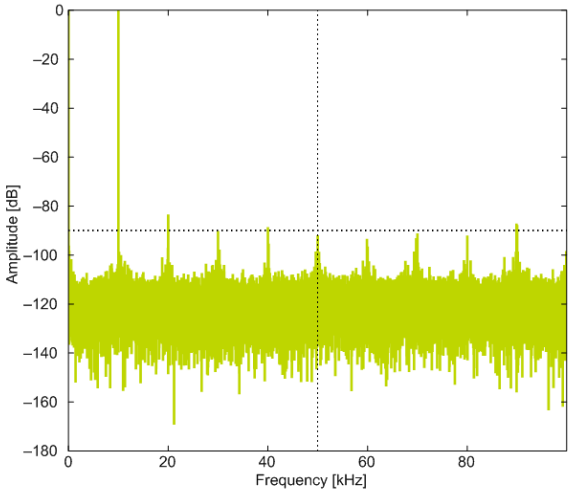
Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



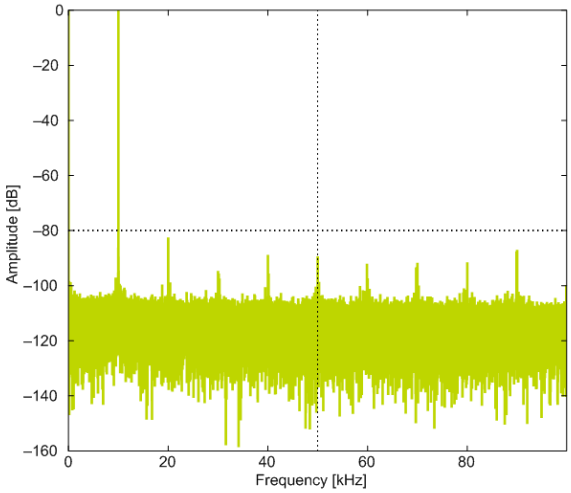
1.25V Reference



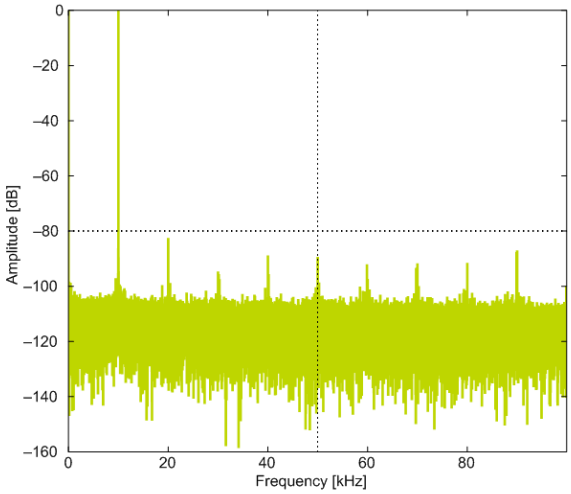
2.5V Reference



2XVDDVSS Reference

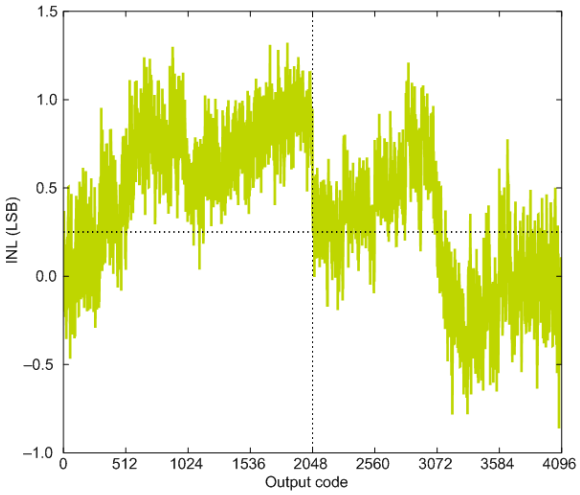


5VDIFF Reference

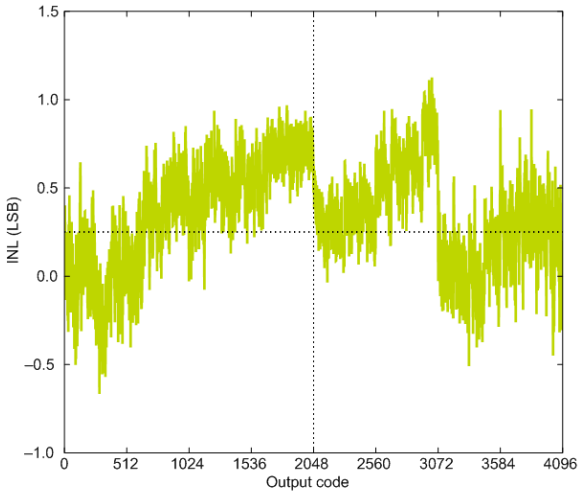


VDD Reference

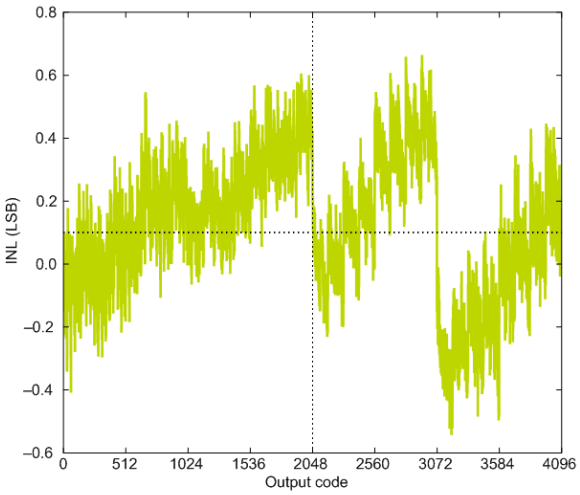
Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C



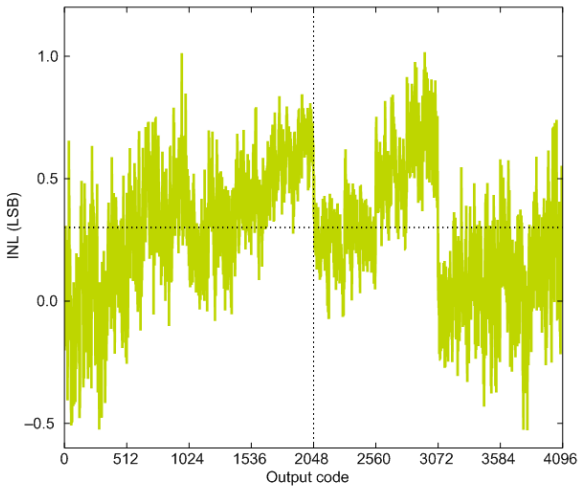
1.25V Reference



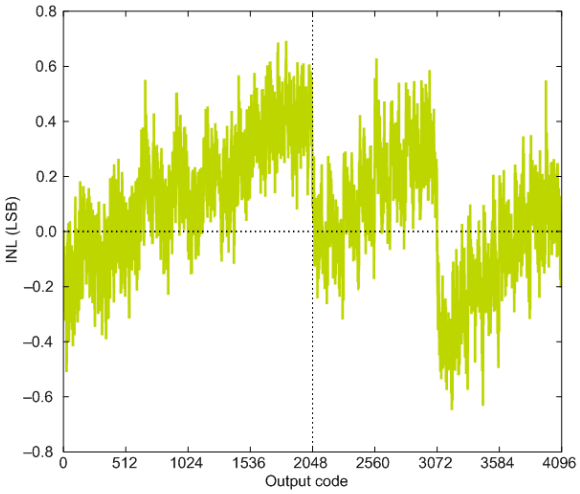
2.5V Reference



2XVDDVSS Reference

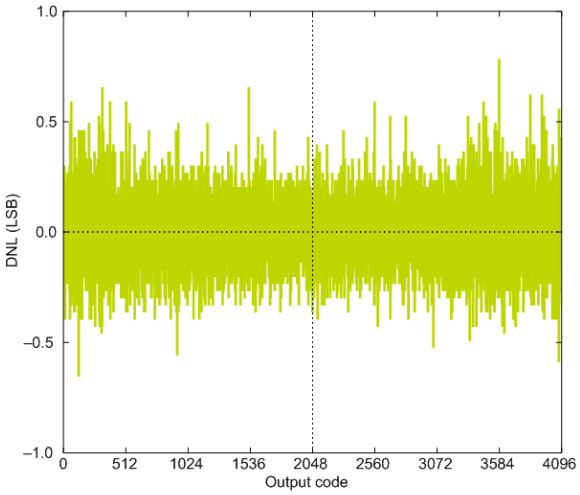


5VDIFF Reference

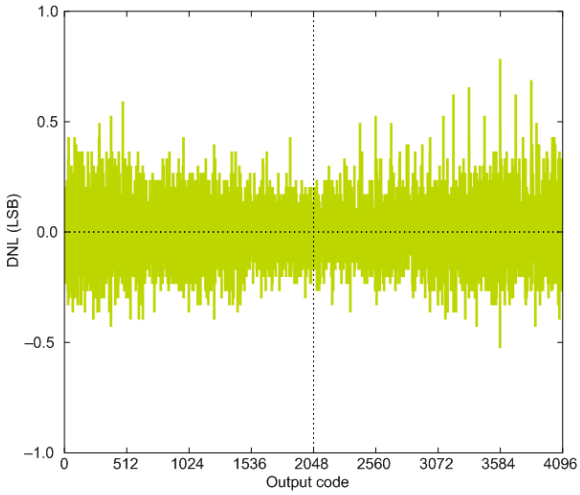


VDD Reference

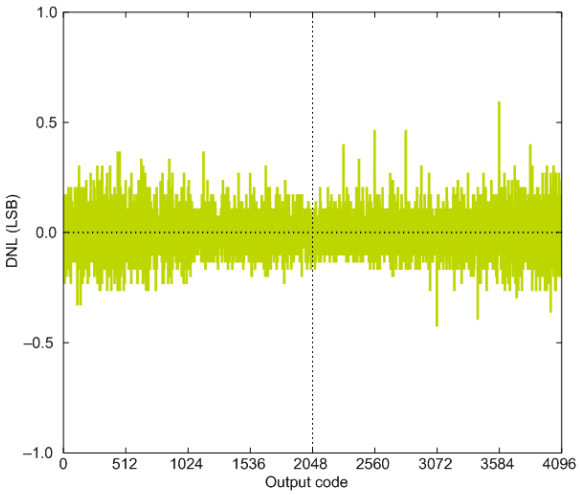
Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C



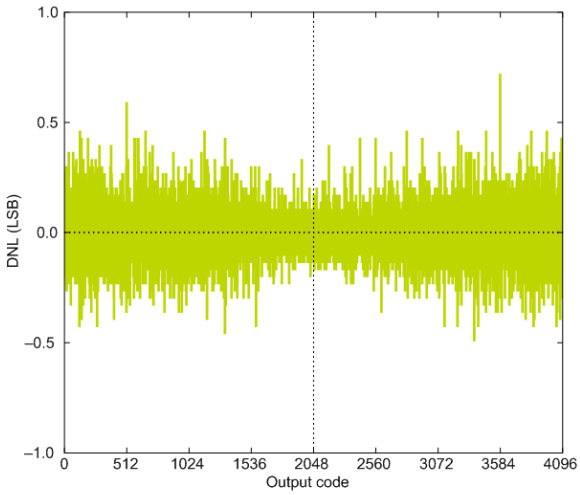
1.25V Reference



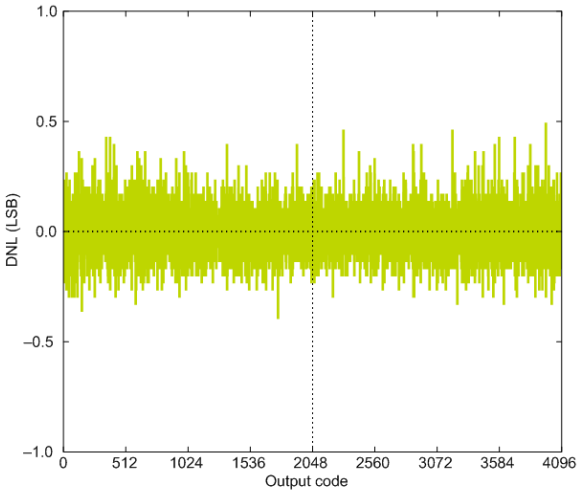
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference

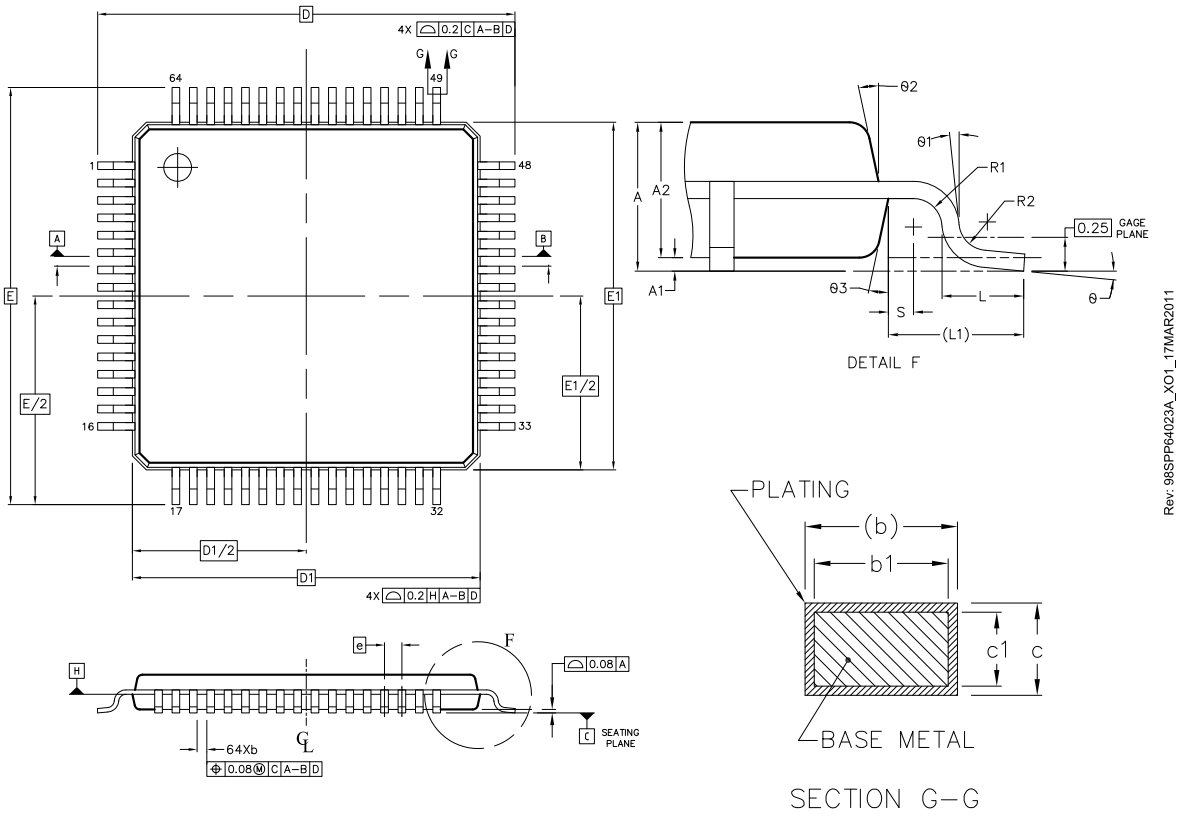


VDD Reference

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
30	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	LETIM0_OUT0 #0 TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	LETIM0_OUT1 #0 TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		I2C0_SDA #2 LEU1_TX #0	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		I2C0_SCL #2 LEU1_RX #0	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
44	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
45	USB_VREGI				
46	USB_VREGO				
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 I2C0_SDA #5 LEU0_TX #3	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 I2C0_SCL #5 LEU0_RX #3	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	USB_VBUS	USB 5.0 V VBUS input.			
53	PF12			USB_ID	
54	PF5		TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8		PCNT2_S0IN #1		PRS_CH3 #1
58	PE9		PCNT2_S1IN #1		
59	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX

4.5 TQFP64 Package

Figure 4.3. TQFP64



Note:

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

Table 4.4. QFP64 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	1.10	1.20	L1		-	
A1	0.05	-	0.15	R1	0.08	-	-
A2	0.95	1.00	1.05	R2	0.08	-	0.20

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. TQFP64 PCB Land Pattern

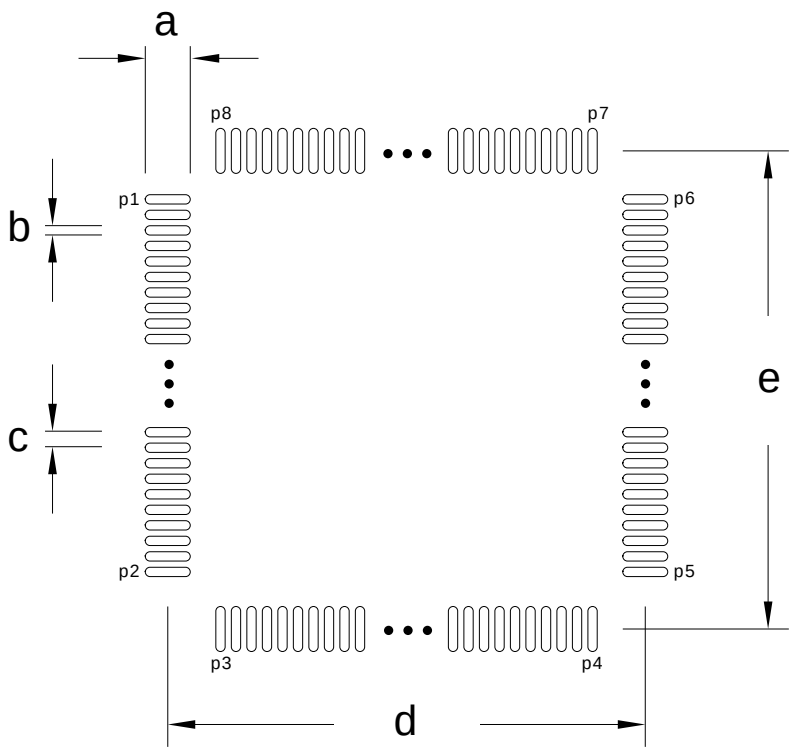


Table 5.1. QFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32	-	-
e	11.50	P5	33	-	-

Figure 5.3. TQFP64 PCB Stencil Design

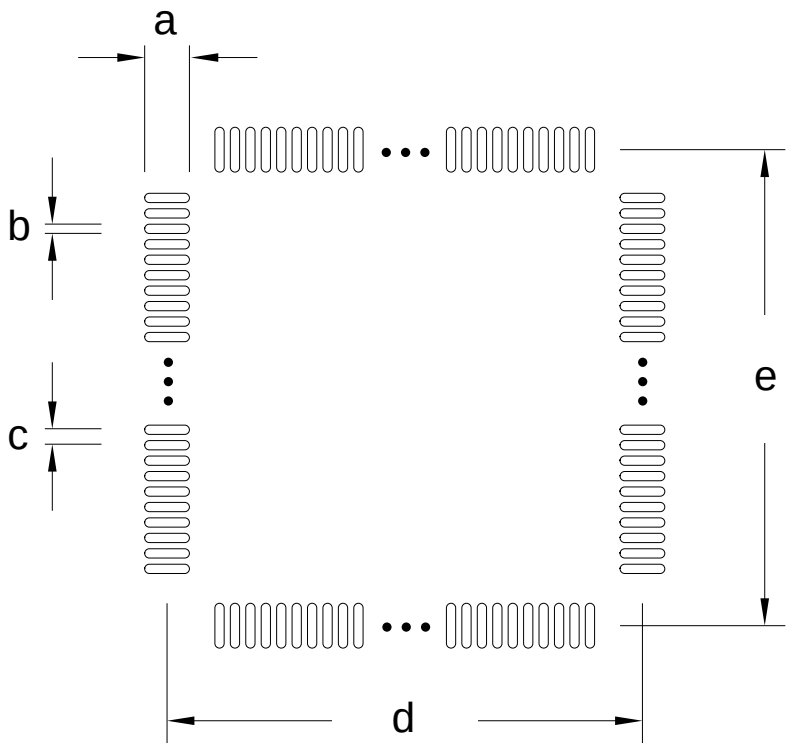


Table 5.3. QFP64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	11.50
e	11.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 57) .

5.2 Soldering Information

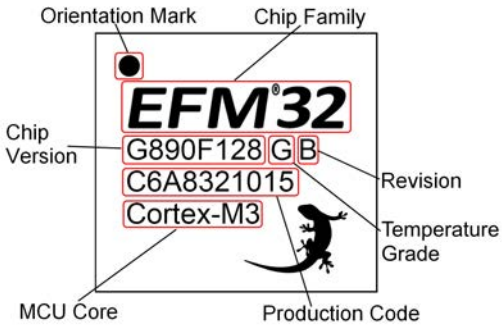
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 62) .

6.3 Errata

Please see the errata document for EFM32GG332 for description and resolution of device erratas. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Added the USB bootloader information.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.5 Revision 1.10

June 28th, 2013

Initial preliminary release.

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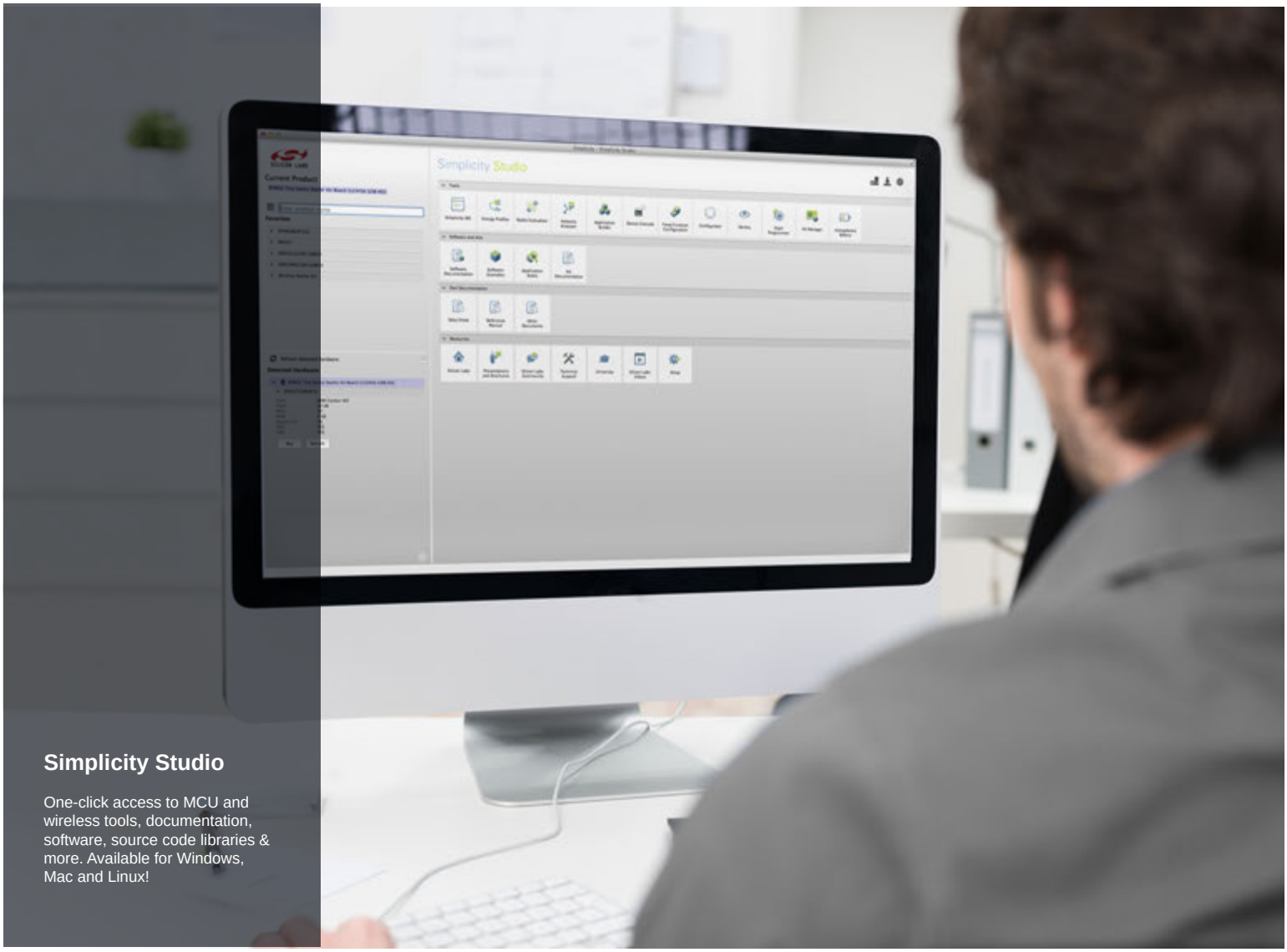

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