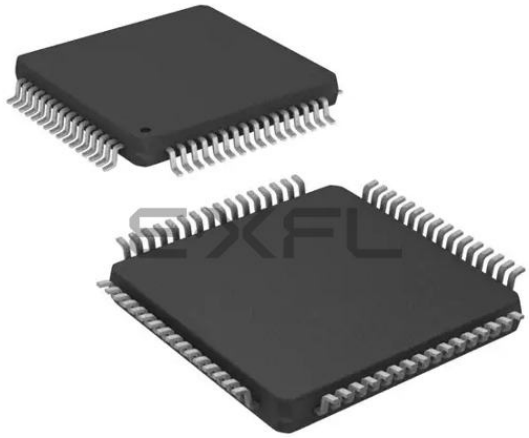
# Silicon Labs - EFM32GG332F512-QFP64 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.85V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg332f512-qfp64 |

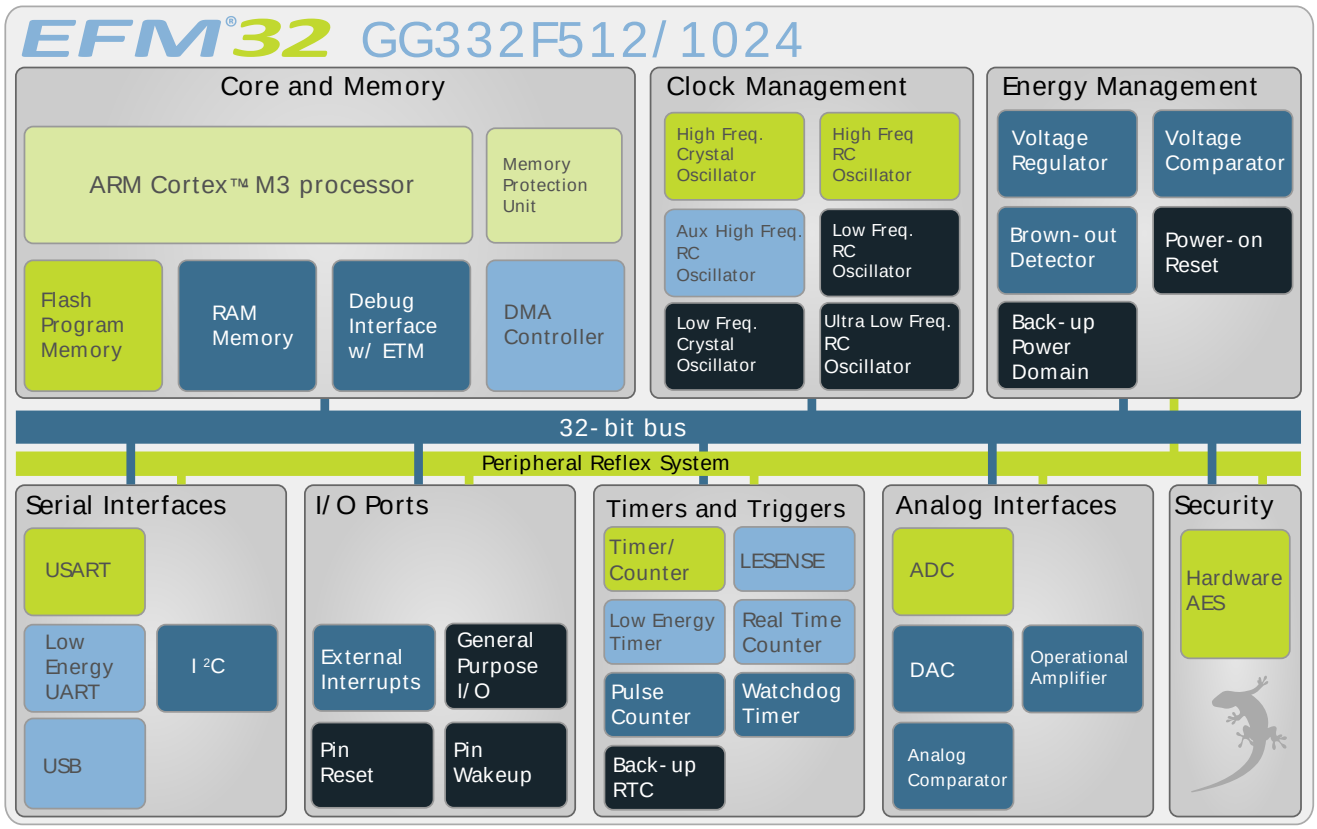
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG332 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG332 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***




### 2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 2.1.26 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG332 to keep track of time and retain data, even if the main power source should drain out.

### 2.1.27 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.28 General Purpose Input/Output (GPIO)

In the EFM32GG332, there are 50 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32GG332 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

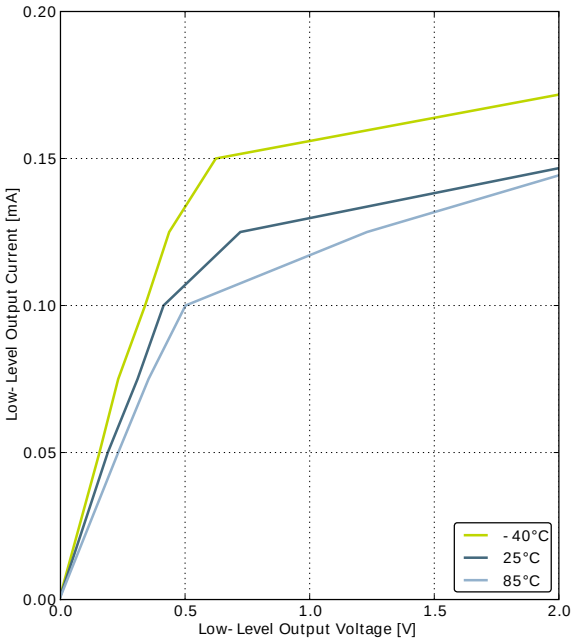
***Table 2.1. Configuration Summary***

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |

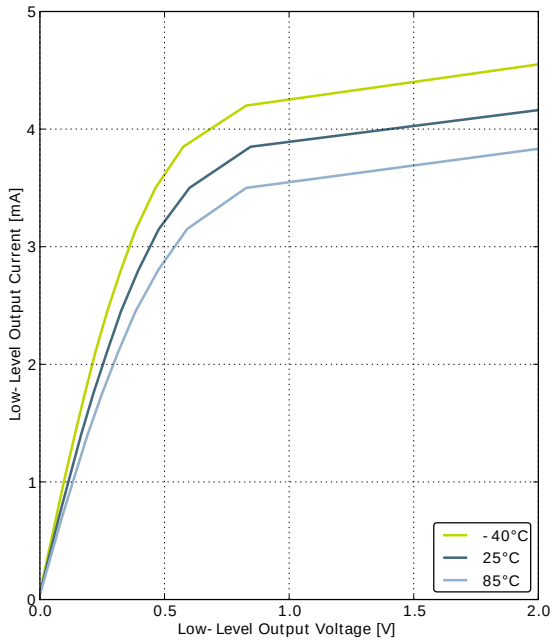
### Table 3.5. Power Management

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | EM0 | 1.74 | | 1.96 | V |
| | | EM2 | 1.74 | | 1.98 | V |
| $V_{BODintthr-}$ | BOD threshold on falling internally regulated supply voltage | | 1.57 | | 1.70 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGO}$ | USB voltage regulator out decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGI}$ | USB voltage regulator in decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | | 4.7 | | µF |

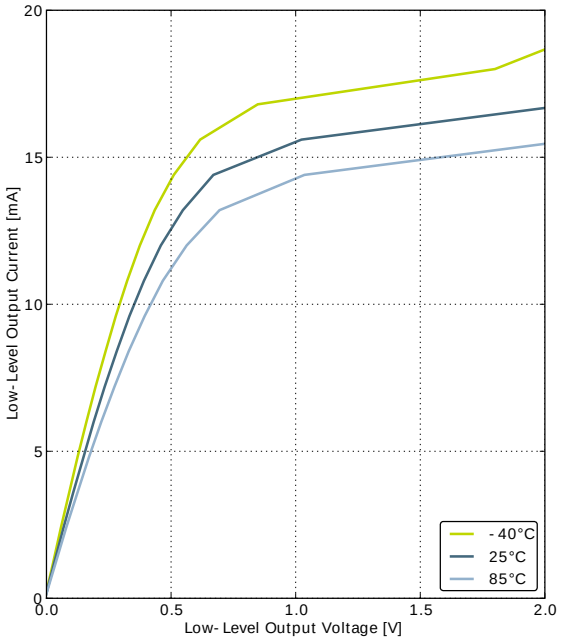
***Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage***



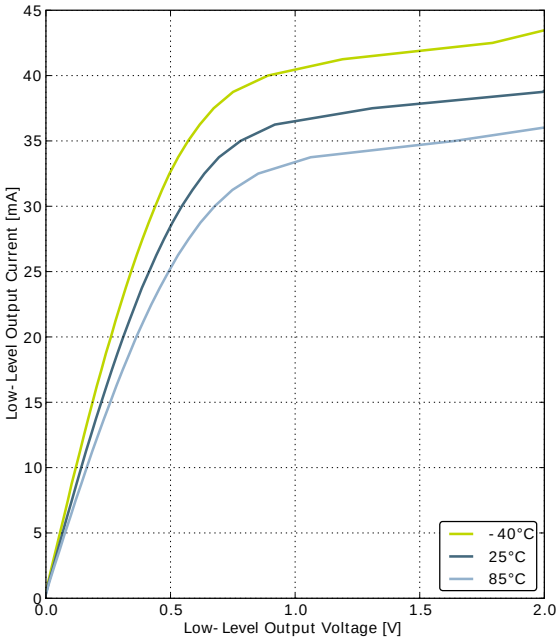

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

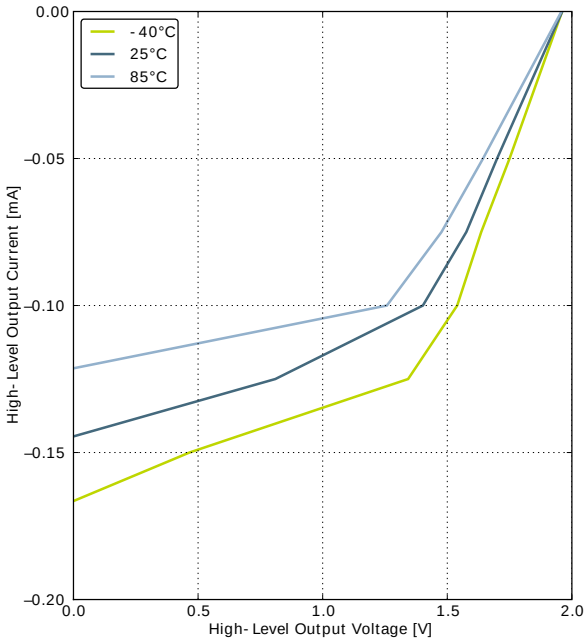



GPIO_Px_CTRL DRIVEMODE = STANDARD

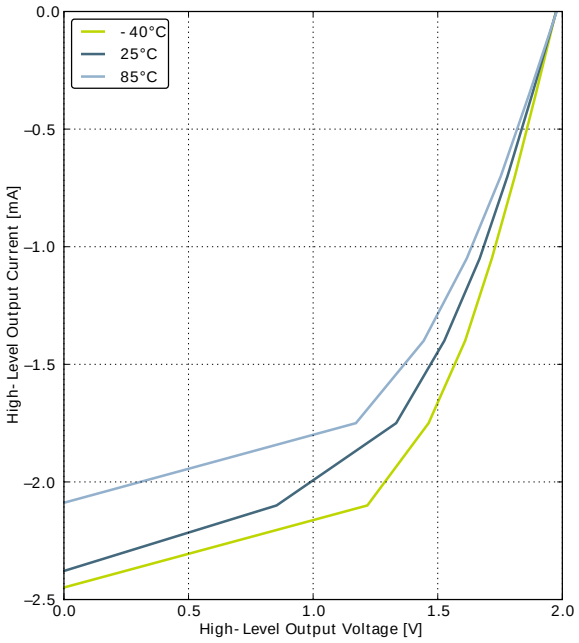



GPIO_Px_CTRL DRIVEMODE = HIGH

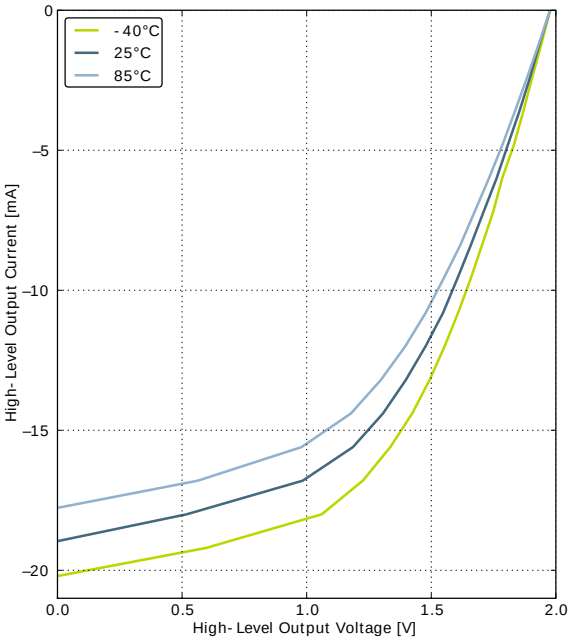
***Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage***



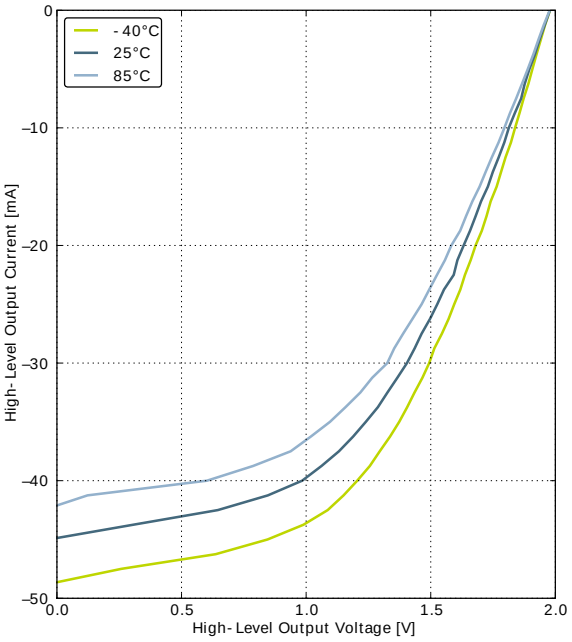

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

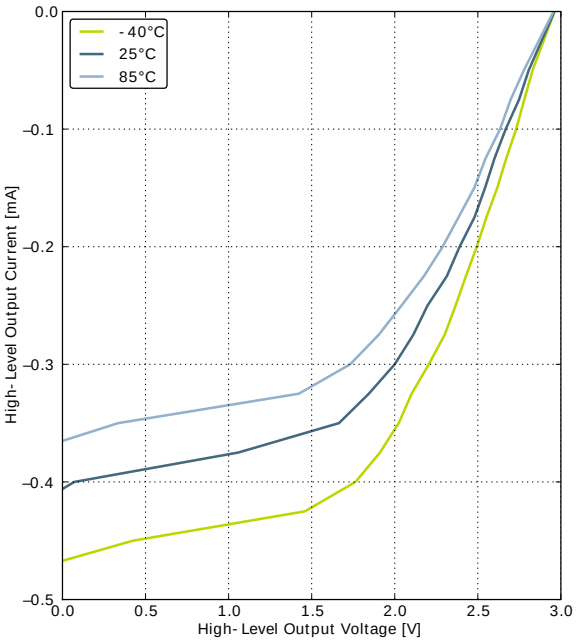



GPIO_Px_CTRL DRIVEMODE = STANDARD

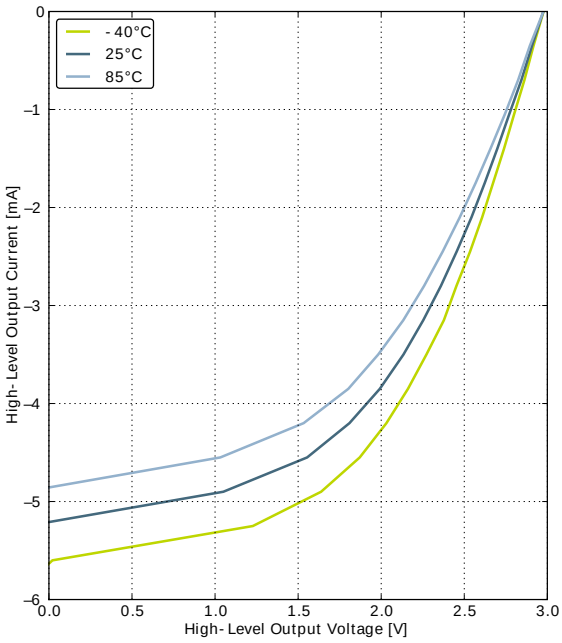



GPIO_Px_CTRL DRIVEMODE = HIGH

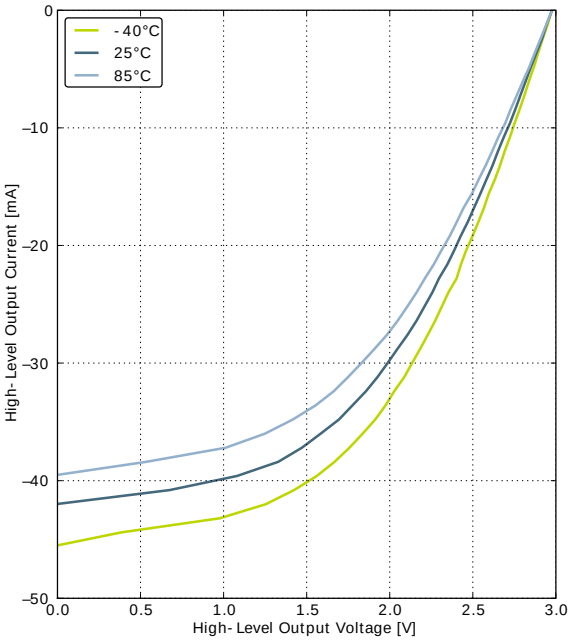
***Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage***



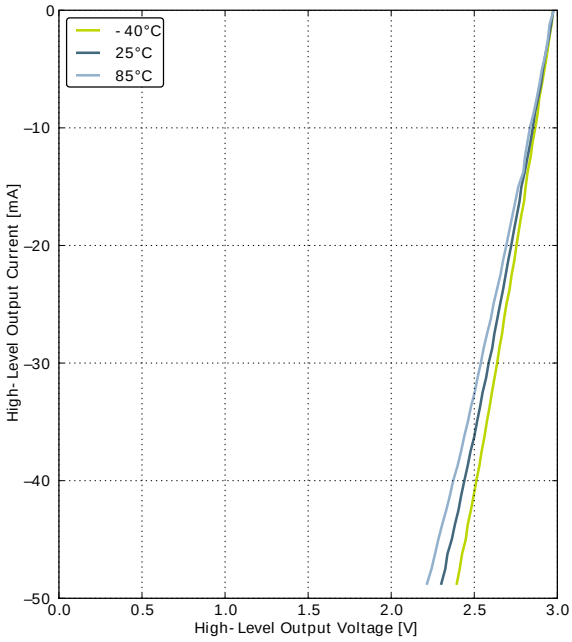

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD



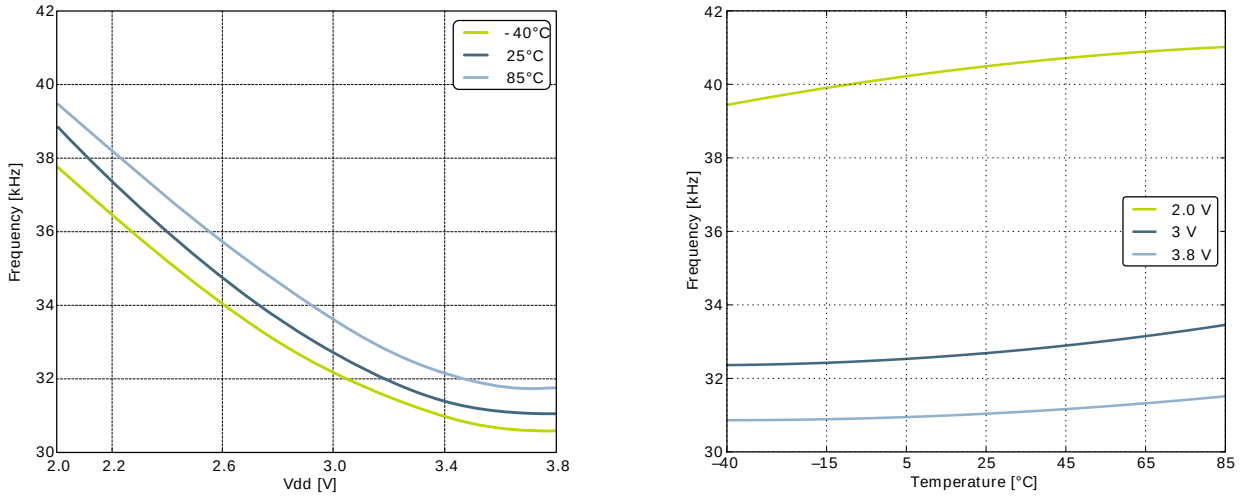

GPIO_Px_CTRL DRIVEMODE = HIGH

## 3.9.3 LFRCO

*Table 3.10. LFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 300 | 900 | nA |
| $TUNESTEP_{L-FRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

*Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage*




## 3.9.4 HFRCO

*Table 3.11. HFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48[1] | 6.60[1] | 6.72[1] | MHz |
| | | 1 MHz frequency band | 1.15[2] | 1.20[2] | 1.25[2] | MHz |
| $t_{HFRCO\_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| | Settling time after band switch | | | 25 | | Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 67 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 63 | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 70 | | dB |
| $SINAD_{ADC}$ | SIgnal-to-Noise And Distortion-ratio (SINAD) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 62 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 62 | 65 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 69 | | dB |
| $SFDR_{ADC}$ | Spurious-Free Dynamic Range (SFDR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 64 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 73 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 66 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 77 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 75 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 69 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | | 0.3 | | mV |
| | | After calibration, differential | -3 | 0.3 | 3 | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/°C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.2 | ±3.0 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | | 13 | 17 | µA |
| $G_{OL}$ | Open Loop Gain | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 101 | | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 98 | | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 91 | | dB |
| $GBW_{OPAMP}$ | Gain Bandwidth Product | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 6.1 | | MHz |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 1.8 | | MHz |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.25 | | MHz |
| $PM_{OPAMP}$ | Phase Margin | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, $C_L$=75 pF | | 64 | | ° |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| $R_{INPUT}$ | Input Resistance | | | 100 | | Mohm |
| $R_{LOAD}$ | Load Resistance | | 200 | | | Ohm |
| $I_{LOAD\_DC}$ | DC Load Current | | | | 11 | mA |
| $V_{INPUT}$ | Input Voltage | OPAxHCMDIS=0 | $V_{SS}$ | | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$-1.2, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 3.2 | | V/µs |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 0.8 | | V/µs |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.1 | | V/µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0 | | 101 | | $µV_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1 | | 141 | | $µV_{RMS}$ |

*Figure 3.27. OPAMP Negative Power Supply Rejection Ratio*

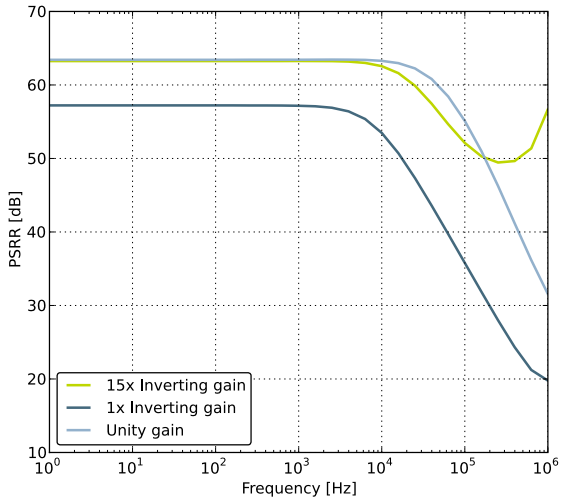



*Figure 3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}$=1V*

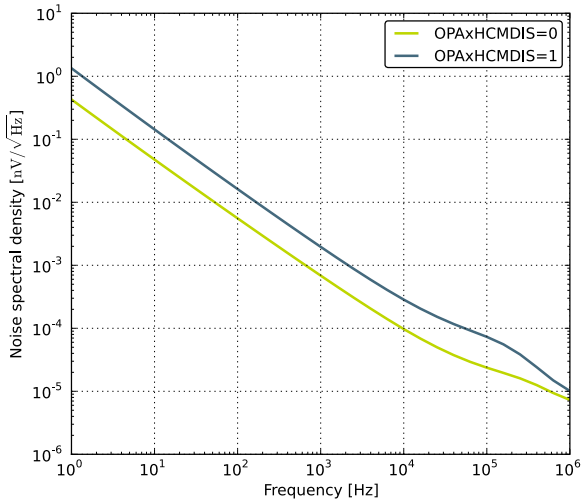
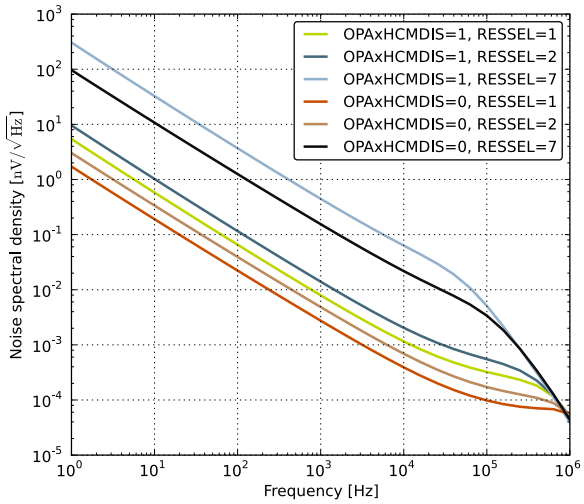



*Figure 3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)*



| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3<br>OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4<br>OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6<br>OPAMP_P1 | LETIM0_OUT0 #0<br>TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7<br>OPAMP_N1 | LETIM0_OUT1 #0<br>TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | I2C0_SDA #2<br>LEU1_TX #0 | LES_CH6 #0<br>ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | I2C0_SCL #2<br>LEU1_RX #0 | LES_CH7 #0<br>ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | USB_VREGI | | | | |
| 46 | USB_VREGO | | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |
| 49 | PF0 | | TIM0_CC0 #5<br>LETIM0_OUT0 #2 | US1_CLK #2<br>I2C0_SDA #5<br>LEU0_TX #3 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5<br>LETIM0_OUT1 #2 | US1_CS #2<br>I2C0_SCL #5<br>LEU0_RX #3 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 58 | PE9 | | PCNT2_S1IN #1 | | |
| 59 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 60 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 61 | PE12 | | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 62 | PE13 | | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 63 | PE14 | | TIM3_CC0 #0 | LEU0_TX #2 | |
| 64 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 52). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

***Note***

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

***Table 4.2. Alternate functionality overview***

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG332* is shown in Table 4.3 (p. 56). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | - | - | - | - | - | - |
| Port F | - | - | - | PF12 | PF11 | PF10 | - | - | - | - | PF5 | - | - | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32GG332* is shown in Figure 4.2 (p. 56) .

***Figure 4.2. Opamp Pinout***

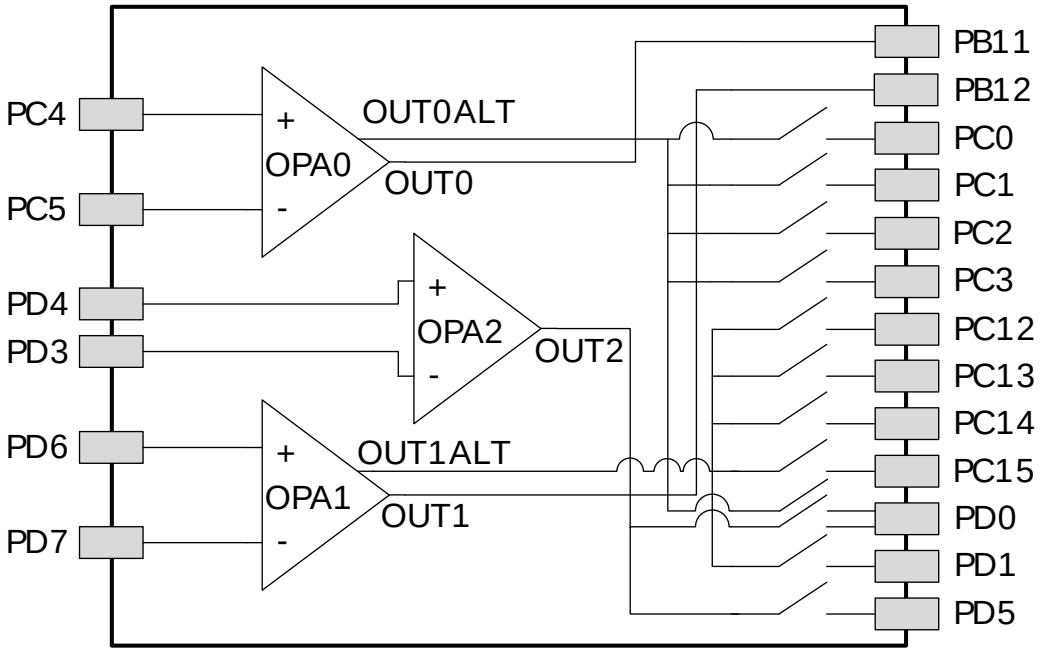


*Figure 5.2. TQFP64 PCB Solder Mask*

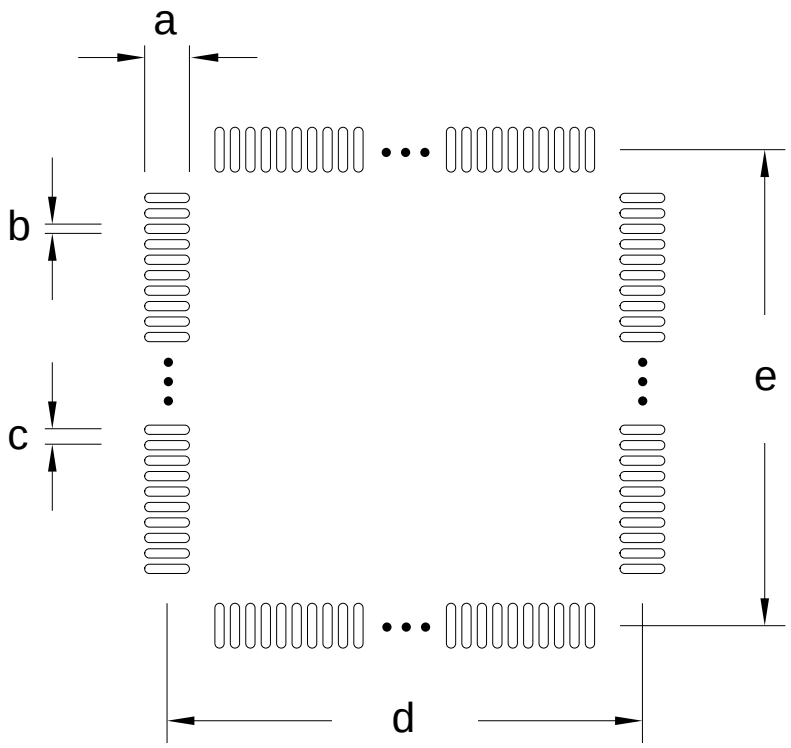



*Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

# 7 Revision History

## 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for $INL_{ADC}$ and $DNL_{ADC}$ parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

## 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

## 7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

## 7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.10 Revision 0.90

June 29th, 2011

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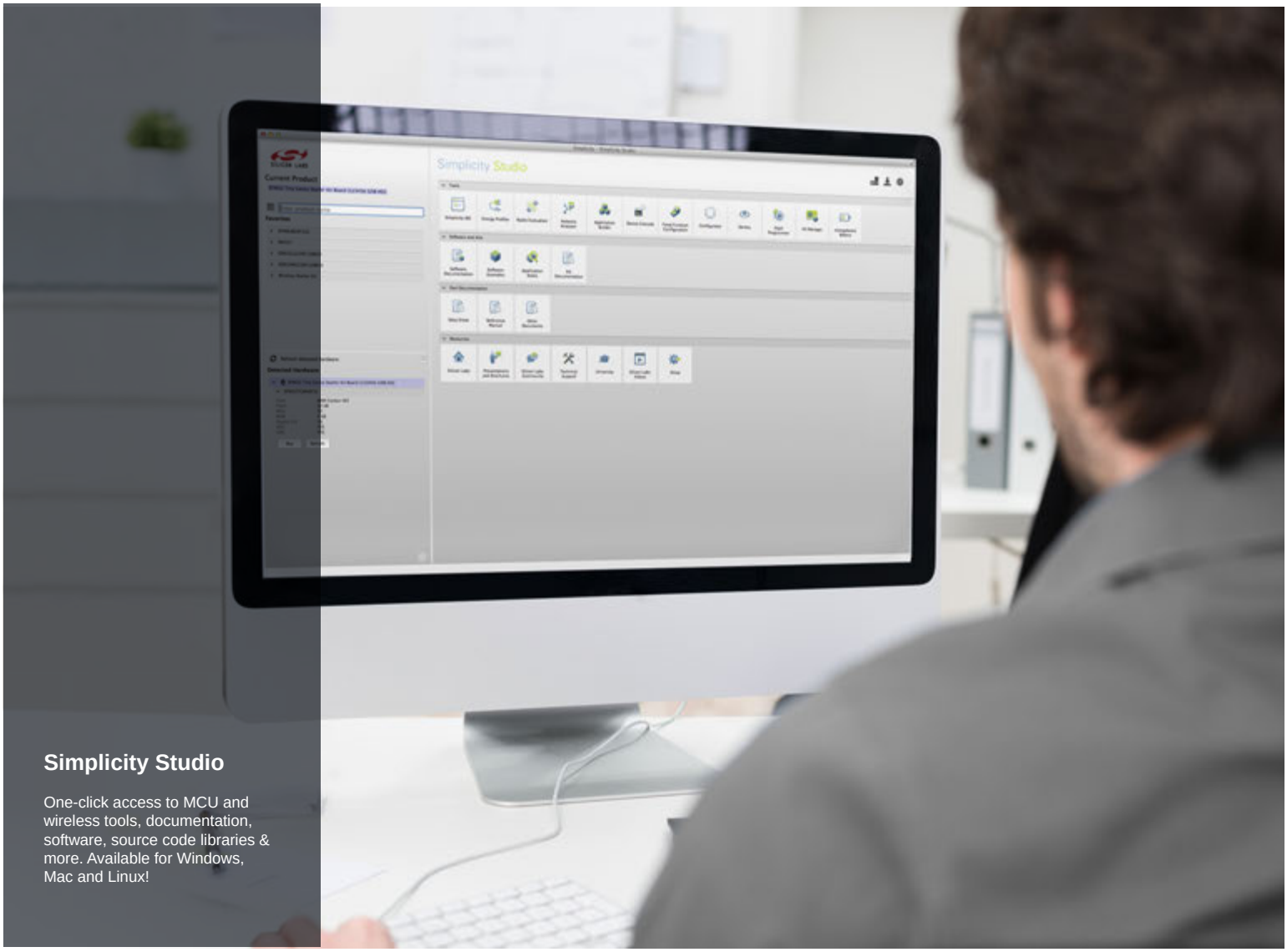
# List of Figures

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