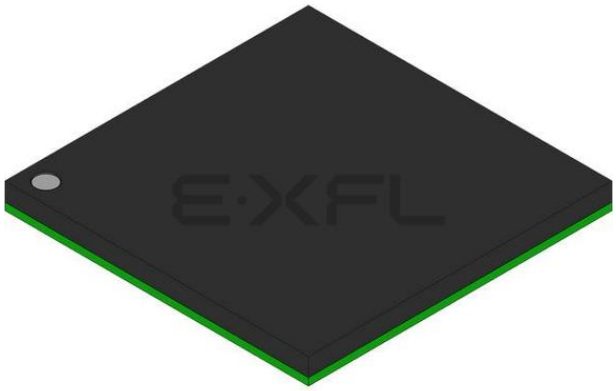

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5232cvm100j

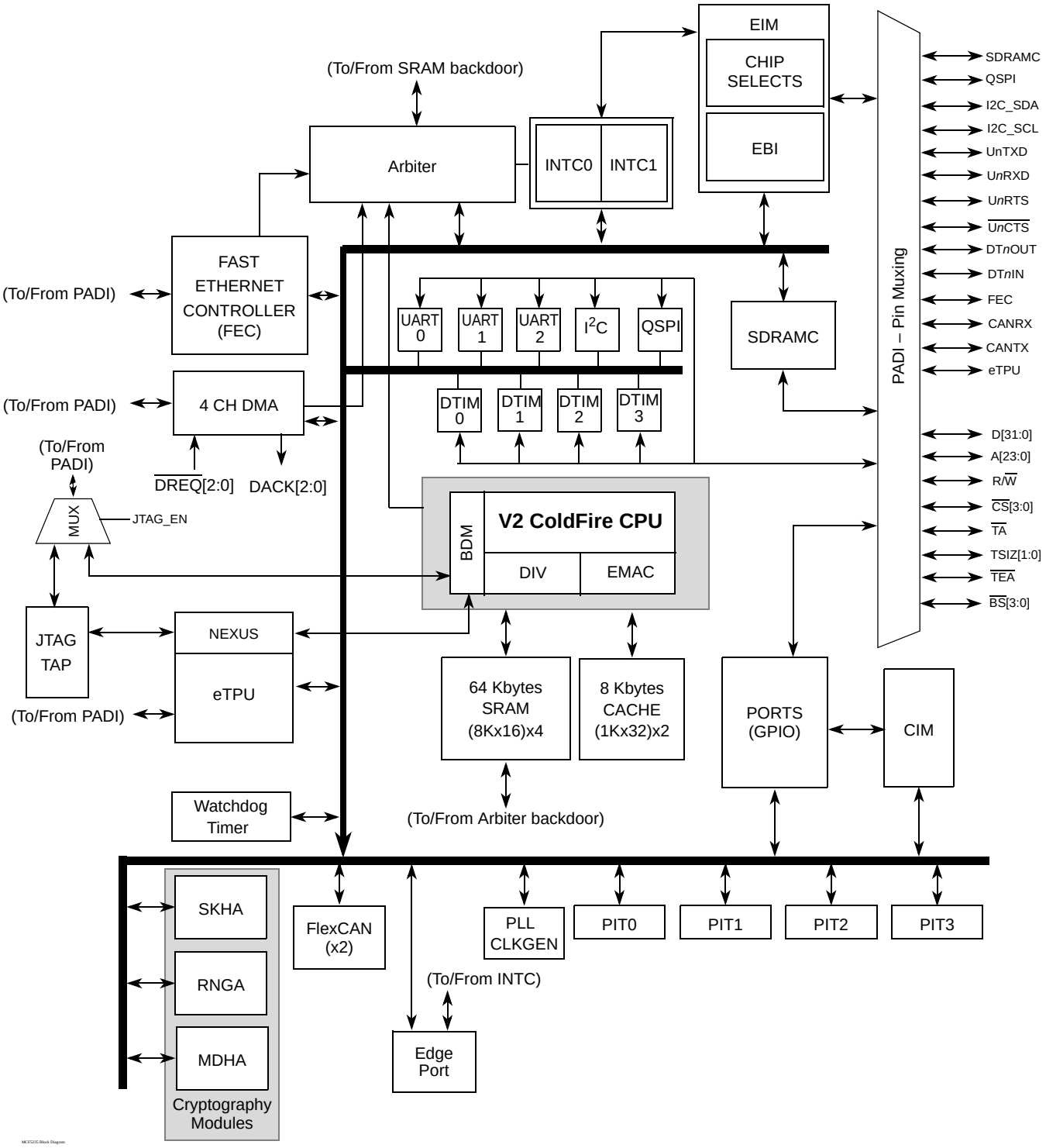
1 MCF523*x* Family Configurations

Table 1. MCF523*x* Family Configurations

Module	MCF5232	MCF5233	MCF5234	MCF5235
ColdFire V2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x	x
Enhanced Time Processor Unit with memory (eTPU)	16-ch 6K	32-ch 6K	16-ch 6K	32-ch 6K
System Clock	up to 150 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 144			
Instruction/Data Cache	8 Kbytes			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	x	x	x	x
External Interface Module (EIM)	x	x	x	x
4-channel Direct-Memory Access (DMA)	x	x	x	x
SDRAM Controller	x	x	x	x
Fast Ethernet Controller (FEC)	—	—	x	x
Cryptography - Security module for data packets processing	—	—	—	x
Watchdog Timer (WDT)	x	x	x	x
Four Periodic Interrupt Timers (PIT)	x	x	x	x
32-bit DMA Timers	4	4	4	4
QSPI	x	x	x	x
UART(s)	3	3	3	3
I^2C	x	x	x	x
FlexCAN 2.0B - Controller-Area Network communication module	1	2	1	2
General Purpose I/O Module (GPIO)	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x	x	x
Package	160 QFP 196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Block Diagram

The superset device in the MCF523*x* family comes in a 256 mold array process ball grid array (MAPBGA) package. Figure shows a top-level block diagram of the MCF5235, the superset device.



3 Features

For a detailed feature list see the MCF5235 Reference Manual (MCF5235RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF523*x* signals, consult the *MCF5235 Reference Manual* (MCF5235RM).

4.1 Signal Properties

Table 2 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF523x Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
Reset									
$\overline{\text{RESET}}$	—	—	—	I	83	N13	T15	T15	T15
$\overline{\text{RSTOUT}}$	—	—	—	O	82	P13	T14	T14	T14
Clock									
EXTAL	—	—	—	I	86	M14	P16	P16	P16
XTAL	—	—	—	O	85	N14	R16	R16	R16
CLKOUT	—	—	—	O	89	K14	M16	M16	M16
Mode Selection									
CLKMOD[1:0]	—	—	—	I	19,20	G5, H5	J3, J2	J3, J2	J3, J2
$\overline{\text{RCON}}$	—	—	—	I	79	K10	P13	P13	P13
External Memory Interface and Ports									
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	126, 125, 124	B11, C11, D11	B14, C14, A15	B14, C14, A15	B14, C14, A15

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
U1RXD	PUARTL4	CAN0RX	—	I	136	D8	A11	A11	A11
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	—	F3	G1	G1	G1
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	—	G3	H3	H3	H3
U0TXD	PUARTL1	—	—	O	14	F1	H2	H2	H2
U0RXD	PUARTL0	—	—	I	13	F2	G2	G2	G2
DMA Timers									
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14	J15	J15	J15
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14	J16	J16	J16
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	—	M9	P10	P10	P10
DT2OUT	PTIMER4	DACK2	—	O	—	L9	R10	R10	R10
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	—	L6	P7	P7	P7
DT1OUT	PTIMER2	DACK1	—	O	—	M6	R7	R7	R7
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	—	E4	G4	G4	G4
DT0OUT	PTIMER0	DACK0	—	O	—	F4	G3	G3	G3
BDM/JTAG[2]									
DSCLK	—	TRST	—	I	70	N9	N11	N11	N11
PSTCLK	—	TCLK	—	O	68	P9	T10	T10	T10
$\overline{\text{BKPT}}$	—	TMS	—	I	71	P10	P11	P11	P11
DSI	—	TDI	—	I	73	M10	T11	T11	T11
DSO	—	TDO	—	O	72	N10	R11	R11	R11
JTAG_EN	—	—	—	I	78	K9	N13	N13	N13
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11	N14, P14, T13, R13	N14, P14, T13, R13	N14, P14, T13, R13
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10	T12, R12, P12, N12	T12, R12, P12, N12	T12, R12, P12, N12

6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5232CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	TPUCH6	TPUCH3	TPUCH2	QSPI_DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{CS3}$	$\overline{CS6}$	$\overline{CS4}$	A20	A17	VSS	A
B	TPUCH8	TPUCH7	TPUCH4	TPUCH0	QSPI_DIN	$\overline{BS3}$	QSPI_CS1	$\overline{U1CTS}$	$\overline{CS7}$	$\overline{CS1}$	A23	A19	A16	A15	B
C	TPUCH10	TPUCH9	TPUCH5	TPUCH1	QSPI_CLK	$\overline{BS2}$	$\overline{BS0}$	$\overline{U1RTS}$	$\overline{CS2}$	$\overline{CS5}$	A22	A18	A14	A13	C
D	TPUCH13	TPUCH12	TPUCH11	NC	NC	VDD	$\overline{BS1}$	U1RXD/CAN0RX	U1TXD/CAN0TX	$\overline{CS0}$	A21	A12	A11	A10	D
E	TPUCH14	TPUCH15	TCRCLK	DT0IN	OVDD	VSS	OVDD	SD_CKE	VSS	OVDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	$\overline{U0CTS}$	DT0OUT	TEST	VSS	OVDD	VSS	OVDD	VSS	VDD	A5	A4	A3	F
G	D31	D30	$\overline{U0RTS}$	VDD	CLKMOD1	OVDD	VSS	OVDD	VSS	LTPU ODIS	A2	A1	A0	DT3OUT	G
H	D29	D28	D27	D26	CLKMOD0	VSS	OVDD	OVDD	OVDD	UTPU ODIS	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	DT3IN	H
J	D25	D24	D23	D22	VSS	OVDD	VSS	OVDD	VSS	OVDD	I2C_SCL	I2C_SDA	R/$\overline{W}$	$\overline{TEA}$	J
K	D21	D20	D19	D18	OVDD	OVDD	VSS	OVDD	JTAG_EN	$\overline{RCON}$	$\overline{SD\_SRAS}$	$\overline{SD\_SCAS}$	$\overline{SD\_WE}$	CLKOUT	K
L	D17	D16	D10	VDD	D3	DT1IN	$\overline{IRQ5}$	$\overline{IRQ1}$	DT2OUT	PST0	DDATA0	$\overline{SD\_CS1}$	$\overline{SD\_CS0}$	VSSPLL	L
M	D15	D13	D9	D6	D2	DT1OUT	$\overline{IRQ6}$	$\overline{IRQ2}$	DT2IN	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	$\overline{OE}$	$\overline{IRQ7}$	$\overline{IRQ3}$	$\overline{TRST}$/DSCLK	TDO/DSO	PST2	DDATA2	$\overline{RESET}$	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{IRQ4}$	TCLK/PSTCLK	$\overline{TMS}$/$\overline{BKPT}$	PST1	DDATA1	$\overline{RSTOUT}$	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2. MCF5232CVMxxx Pinout (196 MAPBGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	ETXD1	TPUCH1	TPUCH0	VDD	$\overline{BS1}$	$\overline{BS0}$	U1RXD/ CAN0RX	U1TXD/ CAN0TX	$\overline{CS6}$	$\overline{CS4}$	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	ETXD2	ETXD3	ETXD0	QSPI_ CLK	$\overline{BS2}$	QSPI_ CS1	$\overline{U1RTS}$	$\overline{CS3}$	$\overline{CS1}$	A23	A20	A19	B
C	TPUCH10	TPUCH9	ERXD1	ERXD0	ETXCLK	ETXER	EMDIO	QSPI_ DIN	$\overline{BS3}$	SD_CKE	$\overline{U1CTS}$	$\overline{CS7}$	$\overline{CS5}$	A22	A18	A17	C
D	TPUCH12	TPUCH11	ERXD3	ERXD2	ERXER	ETXEN	EMDC	QSPI_ DOUT	QSPI_ CS0	U2RXD	U2TXD	$\overline{CS2}$	$\overline{CS0}$	A14	A15	A16	D
E	TPUCH14	TPUCH13	ERXCLK	ERXDV	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	ECOL	ECRS	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	$\overline{U0CTS}$	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	U0RTS	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{TEA}$	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	$\overline{SD\_WE}$	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/$\overline{W}$	L
M	D21	D22	D23	NC	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	$\overline{SD\_CS0}$	$\overline{SD\_ SRAS}$	$\overline{SD\_ SCAS}$	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	$\overline{IRQ5}$	$\overline{IRQ1}$	$\overline{TRST}$/ DSCLK	PST0	JTAG_ EN	DDATA3	$\overline{SD\_CS1}$	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	$\overline{IRQ4}$	DT2IN	TMS/ $\overline{BKPT}$	PST1	$\overline{RCON}$	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	$\overline{IRQ7}$	$\overline{IRQ3}$	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	$\overline{OE}$	$\overline{IRQ6}$	$\overline{IRQ2}$	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	$\overline{RST\ OUT}$	$\overline{RESET}$	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 5. MCF5234CVMxxx Pinout (256 MAPBGA)

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5232CAB80	MCF5232 RISC Microprocessor	160 QFP	80MHz	Yes	–40° to +85° C
MCF5232CVM100	MCF5232 RISC Microprocessor	196 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5232CVM150	MCF5232 RISC Microprocessor	196 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5233CVM100	MCF5233 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5233CVM150	MCF5233 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5234CVM100	MCF5234 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5234CVM150	MCF5234 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVM100	MCF5235 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5235CVM150	MCF5235 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVF150	MCF5235 RISC Microprocessor,	256 MAPBGA	150MHz	No	–40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5235 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5235.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	196 MAPBGA	160 QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	102	104	105[6]	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

6 At 100MHz.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D= P_{INT} + $P_{I/O}$

P_{INT}= $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3 DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	—	1.0	μA
High Impedance (Off-State) Leakage Current $V_{in} = V_{DD}$ or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	—	1.0	μA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	–10	—	– 130	μA

7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.

9 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$.

10 PLL is operating in 1:1 PLL mode.

11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

13 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.

14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.

15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..

2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.

3 Refer to figure A-19.

Timings listed in Table 11 are shown in Figure 10.

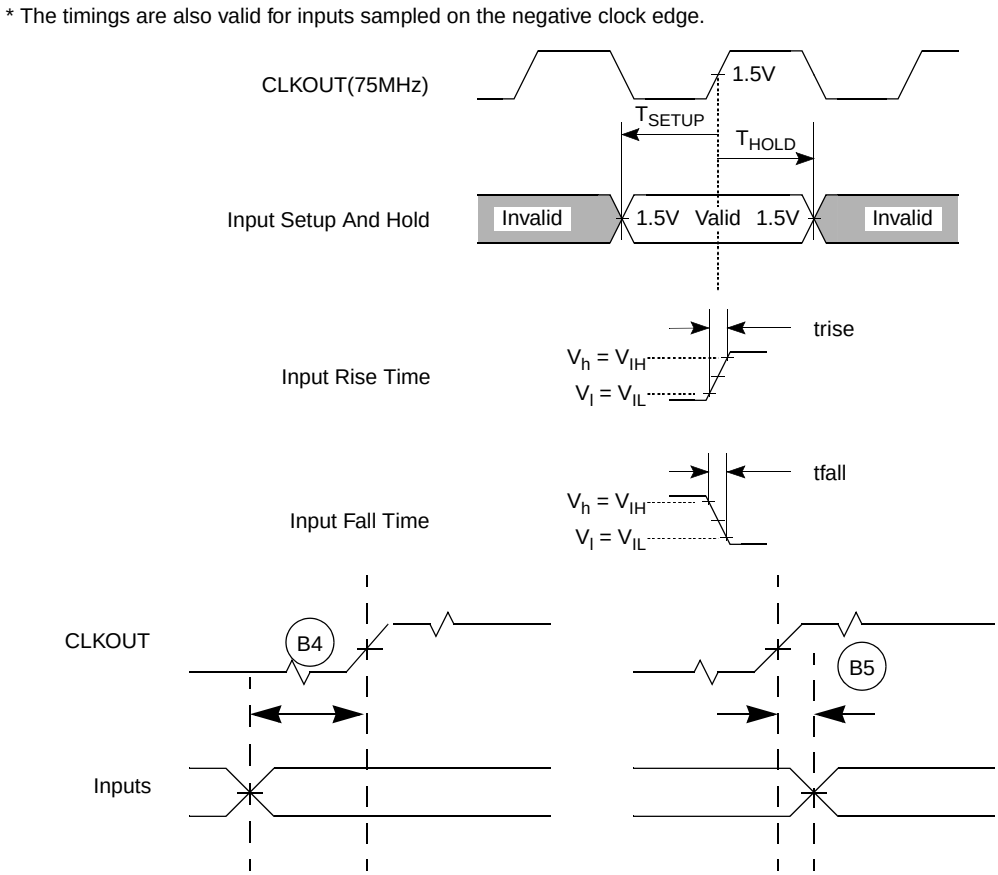


Figure 10. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 12 are shown in Figure 11, Figure 12, and Figure 13.

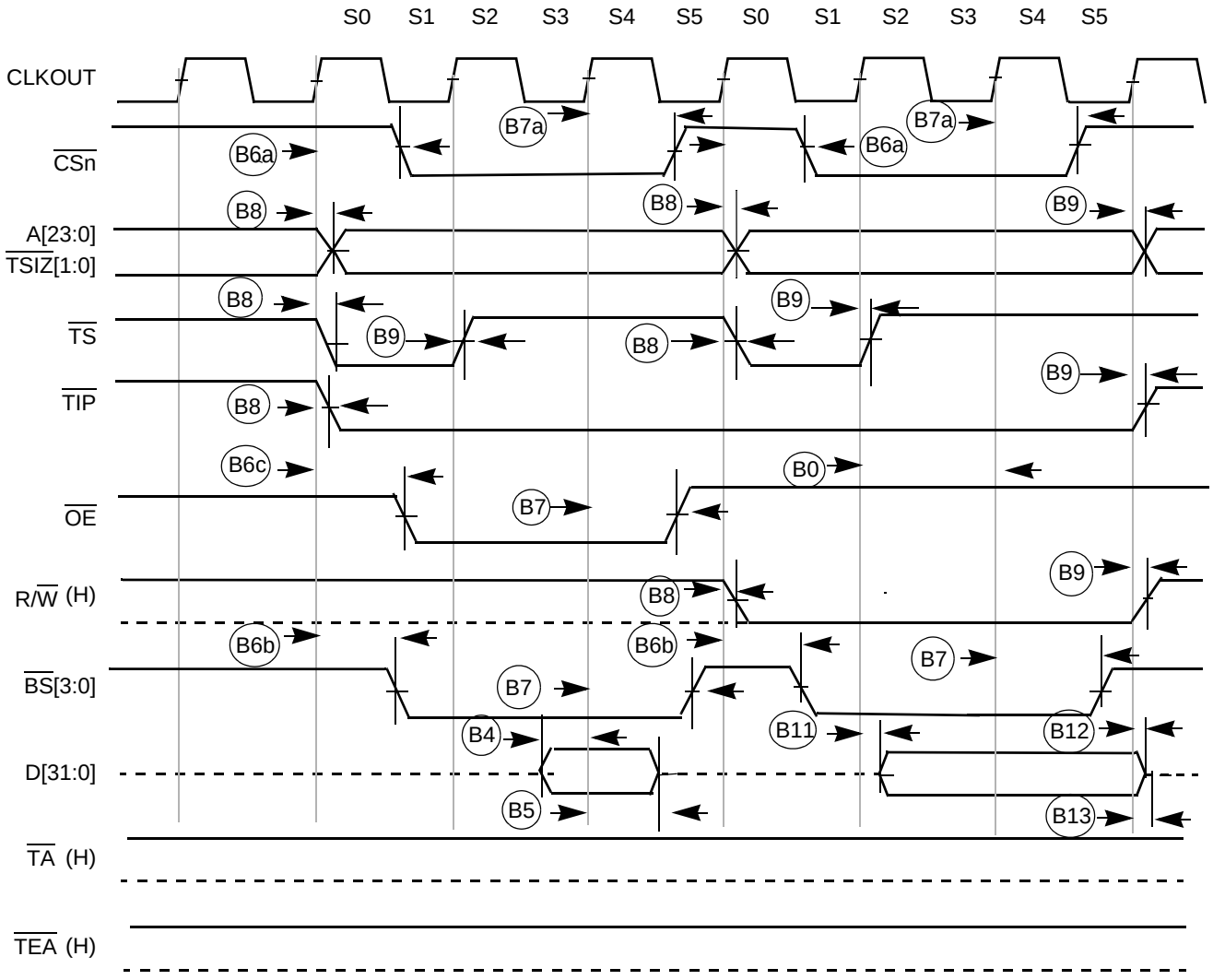


Figure 11. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 12 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

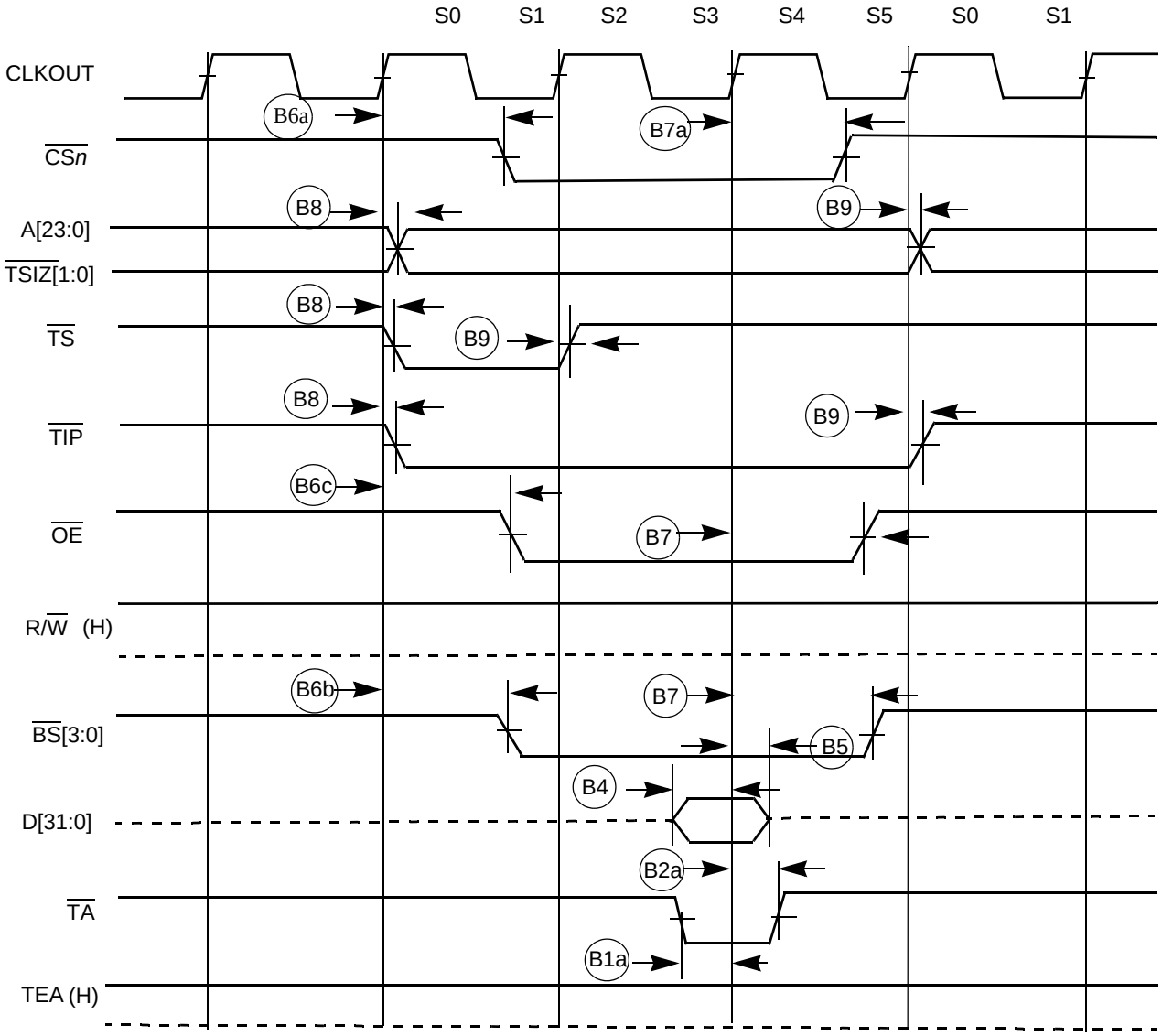


Figure 12. SRAM Read Bus Cycle Terminated by $\overline{TA}$

Figure 13 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

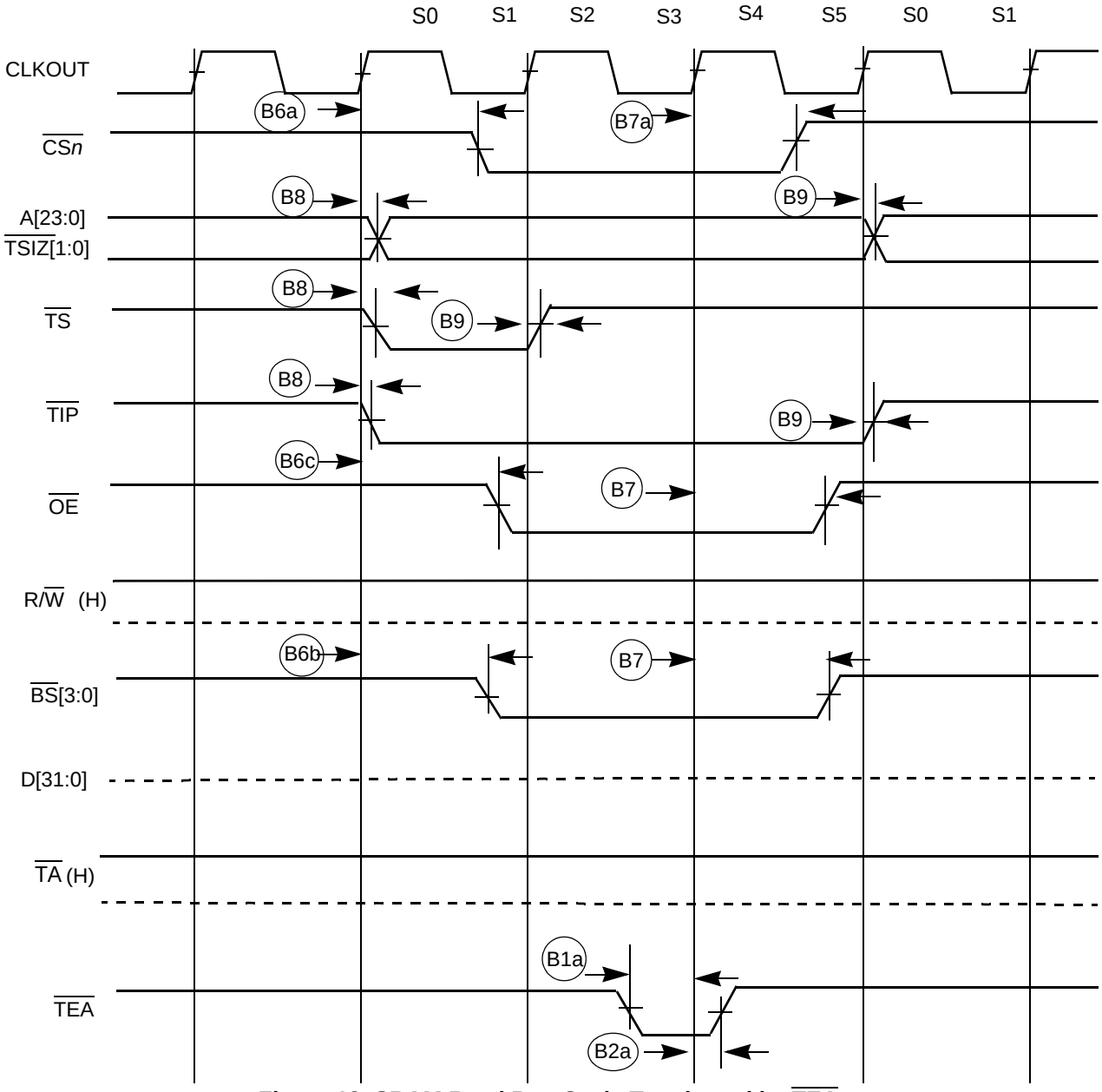


Figure 13. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

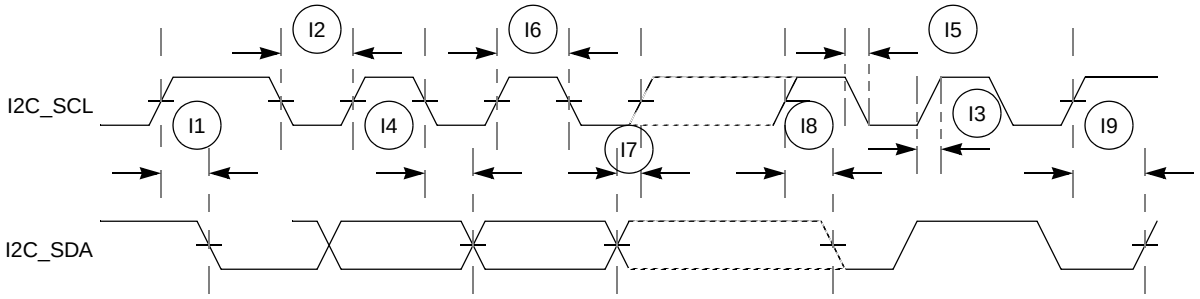


Figure 18. I²C Input/Output Timings

7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	ERXD[3:0], ERXDV, ERXER to ERXCLK setup	5	—	ns
M2	ERXCLK to ERXD[3:0], ERXDV, ERXER hold	5	—	ns
M3	ERXCLK pulse width high	35%	65%	ERXCLK period
M4	ERXCLK pulse width low	35%	65%	ERXCLK period

Figure 19 shows MII receive signal timings listed in Table 18.

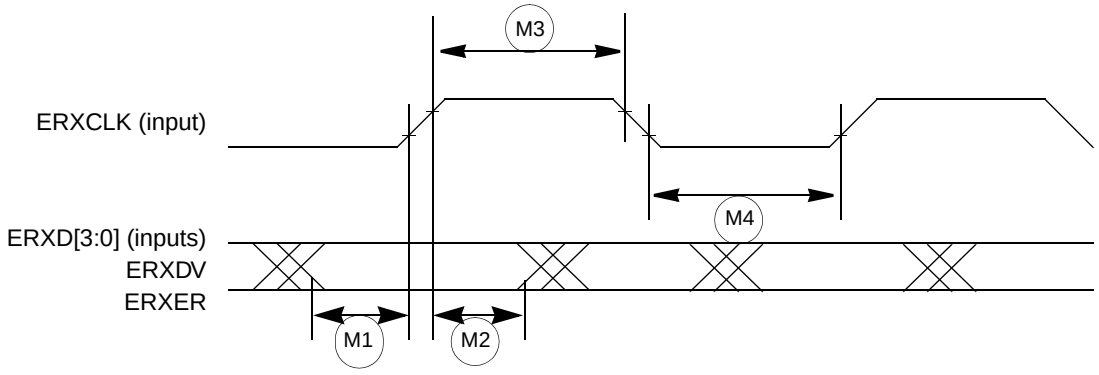


Figure 19. MII Receive Signal Timing Diagram

7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

Figure 22 shows MII serial management channel timings listed in Table 21.

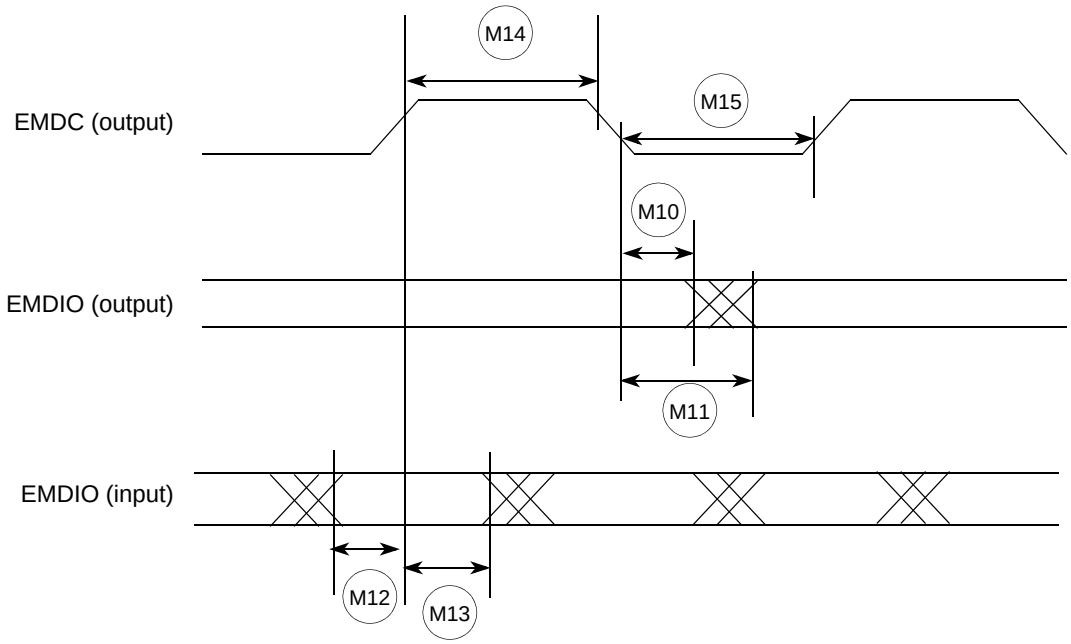


Figure 22. MII Serial Management Channel Timing Diagram

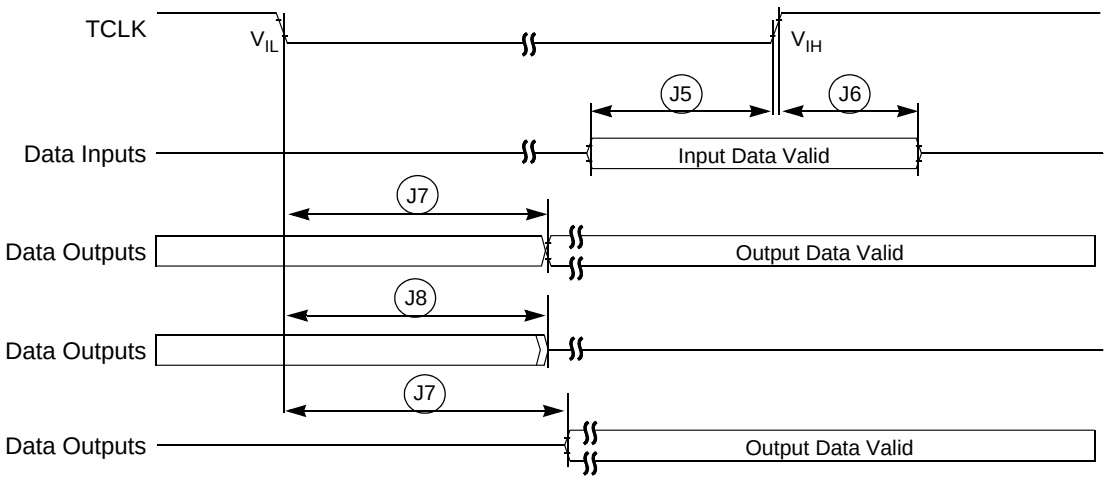


Figure 25. Boundary Scan (JTAG) Timing

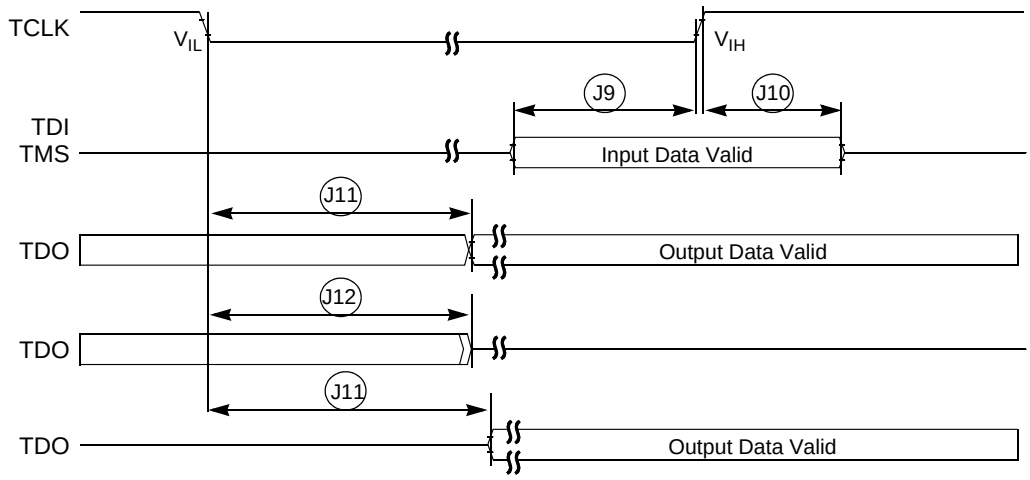


Figure 26. Test Access Port Timing

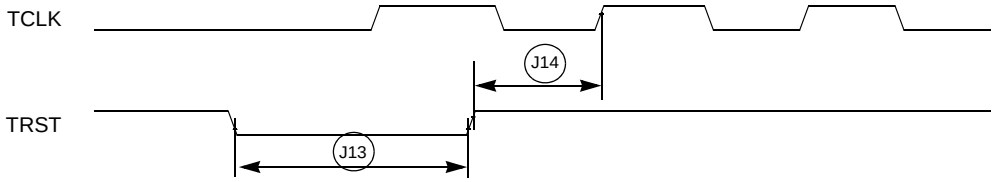


Figure 27. $\overline{\text{TRST}}$ Timing

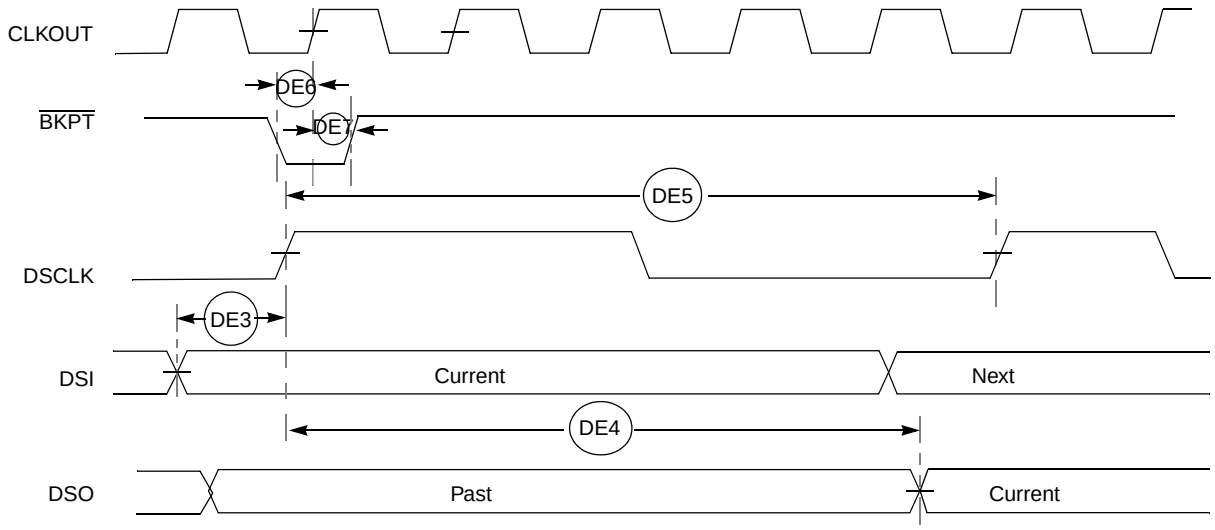


Figure 29. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF523*x* and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5235EC Revision History

Rev. No.	Substantive Change(s)
0	Preliminary release.
1	• Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Corrected Figure 8 pin 81. VDD instead of VSS • Changed instances of Motorola to Freescale
1.3	• Removed detailed signal description section. This information can be found in the MCF5235RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5235RM Chapter 1. • Corrected Figure 2 pin F10. VSS instead of VDD. Change made in Table 2 as well. • Corrected Figure 8 pin 81. OVDD instead of VDD. Change made in Table 2 as well. • Cleaned up many inconsistencies within the pinout figure signal names • Corrected document IDs in Documentation Table
1.4	• Added values for ‘Maximum operating junction temperature’ in Table 8. • Added typical values for ‘Core operating supply current (master mode)’ in Table 9. • Added typical values for ‘Pad operating supply current (master mode)’ in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.

Table 26. MCF5235EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.5	• Removed Overview, Features, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5235 Reference Manual. • Removed list of documentation table in Section 8, "Documentation.". An up-to-date list is always available on our web site.
1.6	• Table 9: Changed core supply voltage (V_{DD}) from 1.35-1.65 to 1.4-1.6.
1.7	• Table 10: Changed max f_{ICO} frequency from "75 MHz" to "150 MHz".
1.8	• Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." • Updated 196MAPBGA package dimensions, Figure 3.
2	• Table 2: Changed SD_CKE pin location from 139 to "—" for the 160QFP device. Changed QSPI_CS1 pin location from "—" to 139 for the 160QFP device. • Figure 8: Changed pin 139 label from "SD_CKE/QSPI_CS1" to "QSPI_CS1/SD_CKE". • Removed second sentence from Section 7.10.1, "MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)," and Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," as this feature is not supported on this device.
3	• Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, "Power Up Sequence" first bullet, changed "Use 1 µs" to "Use 1 ms". • Corrected position of spec D5 in Figure 14. • Table 14: Added $\overline{DACKn}$ and $\overline{DREQn}$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5235CVF150 in Table 6