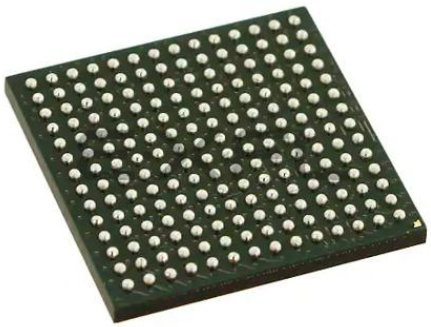

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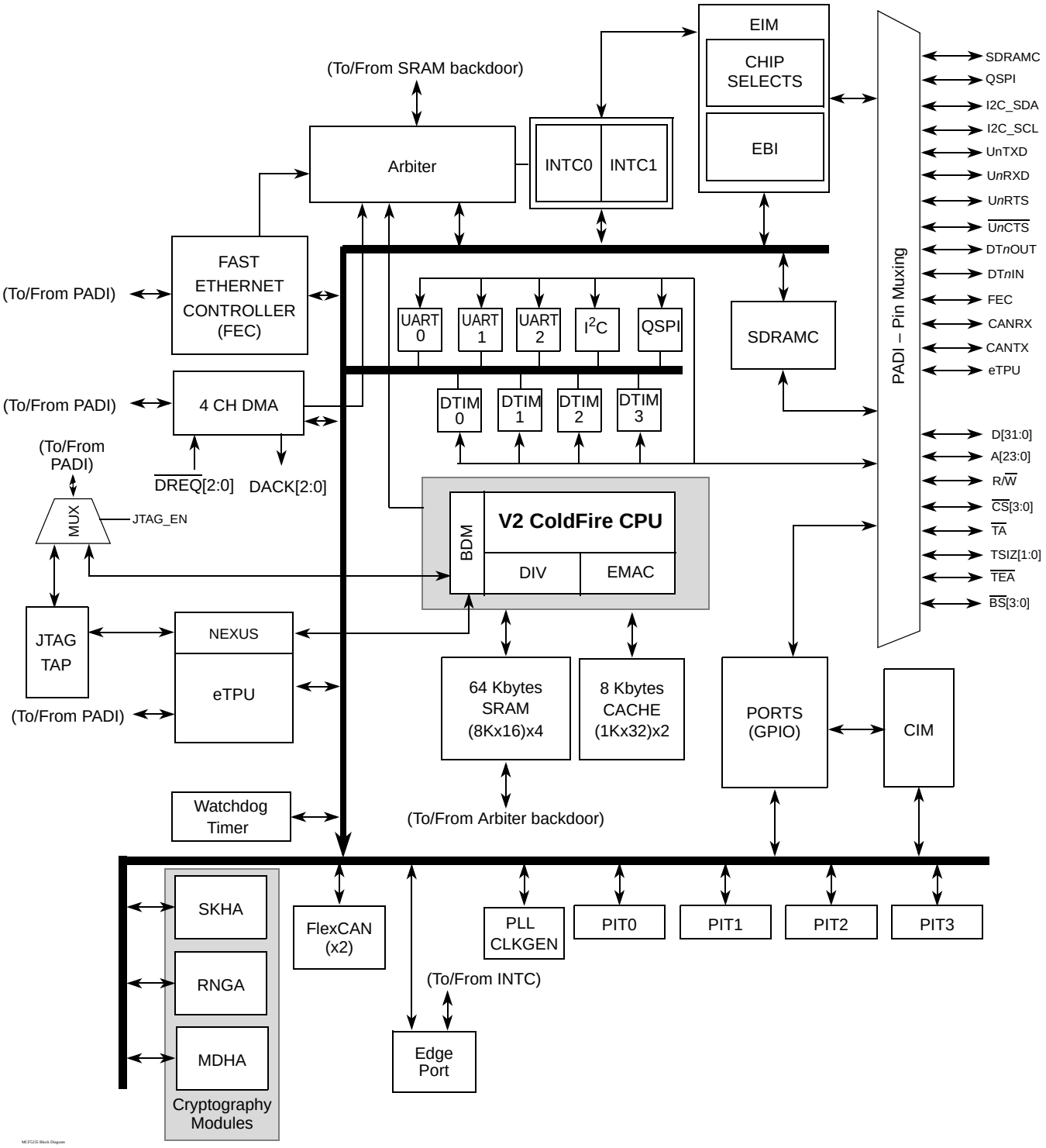
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5232cvm150j



3 Features

For a detailed feature list see the MCF5235 Reference Manual (MCF5235RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF523*x* signals, consult the *MCF5235 Reference Manual* (MCF5235RM).

4.1 Signal Properties

Table 2 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF523x Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
Reset									
$\overline{\text{RESET}}$	—	—	—	I	83	N13	T15	T15	T15
$\overline{\text{RSTOUT}}$	—	—	—	O	82	P13	T14	T14	T14
Clock									
EXTAL	—	—	—	I	86	M14	P16	P16	P16
XTAL	—	—	—	O	85	N14	R16	R16	R16
CLKOUT	—	—	—	O	89	K14	M16	M16	M16
Mode Selection									
CLKMOD[1:0]	—	—	—	I	19,20	G5, H5	J3, J2	J3, J2	J3, J2
$\overline{\text{RCON}}$	—	—	—	I	79	K10	P13	P13	P13
External Memory Interface and Ports									
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	126, 125, 124	B11, C11, D11	B14, C14, A15	B14, C14, A15	B14, C14, A15

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
Test									
TEST	—	—	—	I	18	F5	J4	J4	J4
PLL_TEST	—	—	—	I	—		R14	R14	R14
Power Supplies									
VDDPLL	—	—	—	I	87	M13	P15		
VSSPLL	—	—	—	I	84	L14	R15		
OVDD	—	—	—	I	1, 9, 17, 32, 41, 55, 62, 69, 81, 90, 95, 105, 114, 128, 132, 138, 146	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8	E6:11, F5, F7:10, F12, G5, G6, G11, G12, H5, H6, H11, H12, J5, J6, J11, J12, K5, K6, K11, K12, L5, L7:10, L12, M6:M11		
VSS	—	—	—	I	8, 16, 25, 31, 40, 54, 61, 67, 80, 88, 94, 104, 113, 127, 131, 137, 145, 153, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14	A1, A16, E5, E12, F6, F11, F16, G7:10, H7: 10, J1, J7:10, K7:10, L6, L11, M5, M12, N16, T1, T6, T16		
VDD	—	—	—	I	15, 53, 103, 144	D6, F11, G4, L4	A8, G16, H1, T5		

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

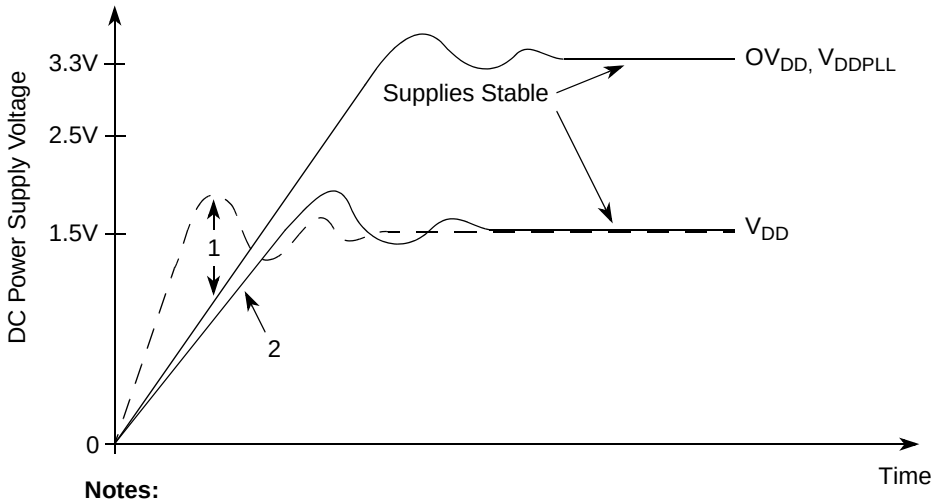
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF523*x*.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 μF, 0.1 μF, and 0.01 μF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 1 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 1. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.7.3 FlexCAN

The FlexCAN module interface to the CAN bus is composed of 2 pins: CANTX and CANRX, which are the serial transmitted data and the serial received data. The use of an external CAN transceiver to interface to the CAN bus is generally required. The transceiver is capable of driving the large current needed for the CAN bus and has current protection, against a defective CAN bus or defective stations.

5.7.4 BDM

Use the BDM interface as shown in the M523*x*EVB evaluation board user's manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF523*x* devices. See Table 2 for a list the signal names and pin locations for each device.

6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5232CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	TPUCH6	TPUCH3	TPUCH2	QSPI_DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{CS3}$	$\overline{CS6}$	$\overline{CS4}$	A20	A17	VSS	A
B	TPUCH8	TPUCH7	TPUCH4	TPUCH0	QSPI_DIN	$\overline{BS3}$	QSPI_CS1	$\overline{U1CTS}$	$\overline{CS7}$	$\overline{CS1}$	A23	A19	A16	A15	B
C	TPUCH10	TPUCH9	TPUCH5	TPUCH1	QSPI_CLK	$\overline{BS2}$	$\overline{BS0}$	$\overline{U1RTS}$	$\overline{CS2}$	$\overline{CS5}$	A22	A18	A14	A13	C
D	TPUCH13	TPUCH12	TPUCH11	NC	NC	VDD	$\overline{BS1}$	U1RXD/CAN0RX	U1TXD/CAN0TX	$\overline{CS0}$	A21	A12	A11	A10	D
E	TPUCH14	TPUCH15	TCRCLK	DT0IN	OVDD	VSS	OVDD	SD_CKE	VSS	OVDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	$\overline{U0CTS}$	DT0OUT	TEST	VSS	OVDD	VSS	OVDD	VSS	VDD	A5	A4	A3	F
G	D31	D30	$\overline{U0RTS}$	VDD	CLKMOD1	OVDD	VSS	OVDD	VSS	LTPU ODIS	A2	A1	A0	DT3OUT	G
H	D29	D28	D27	D26	CLKMOD0	VSS	OVDD	OVDD	OVDD	UTPU ODIS	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	DT3IN	H
J	D25	D24	D23	D22	VSS	OVDD	VSS	OVDD	VSS	OVDD	I2C_SCL	I2C_SDA	R/$\overline{W}$	$\overline{TEA}$	J
K	D21	D20	D19	D18	OVDD	OVDD	VSS	OVDD	JTAG_EN	$\overline{RCON}$	$\overline{SD\_SRAS}$	$\overline{SD\_SCAS}$	$\overline{SD\_WE}$	CLKOUT	K
L	D17	D16	D10	VDD	D3	DT1IN	$\overline{IRQ5}$	$\overline{IRQ1}$	DT2OUT	PST0	DDATA0	$\overline{SD\_CS1}$	$\overline{SD\_CS0}$	VSSPLL	L
M	D15	D13	D9	D6	D2	DT1OUT	$\overline{IRQ6}$	$\overline{IRQ2}$	DT2IN	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	$\overline{OE}$	$\overline{IRQ7}$	$\overline{IRQ3}$	$\overline{TRST}$/DSCLK	TDO/DSO	PST2	DDATA2	$\overline{RESET}$	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{IRQ4}$	TCLK/PSTCLK	$\overline{TMS}$/$\overline{BKPT}$	PST1	DDATA1	$\overline{RSTOUT}$	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2. MCF5232CVMxxx Pinout (196 MAPBGA)

6.2.1 Pinout—256 MAPBGA

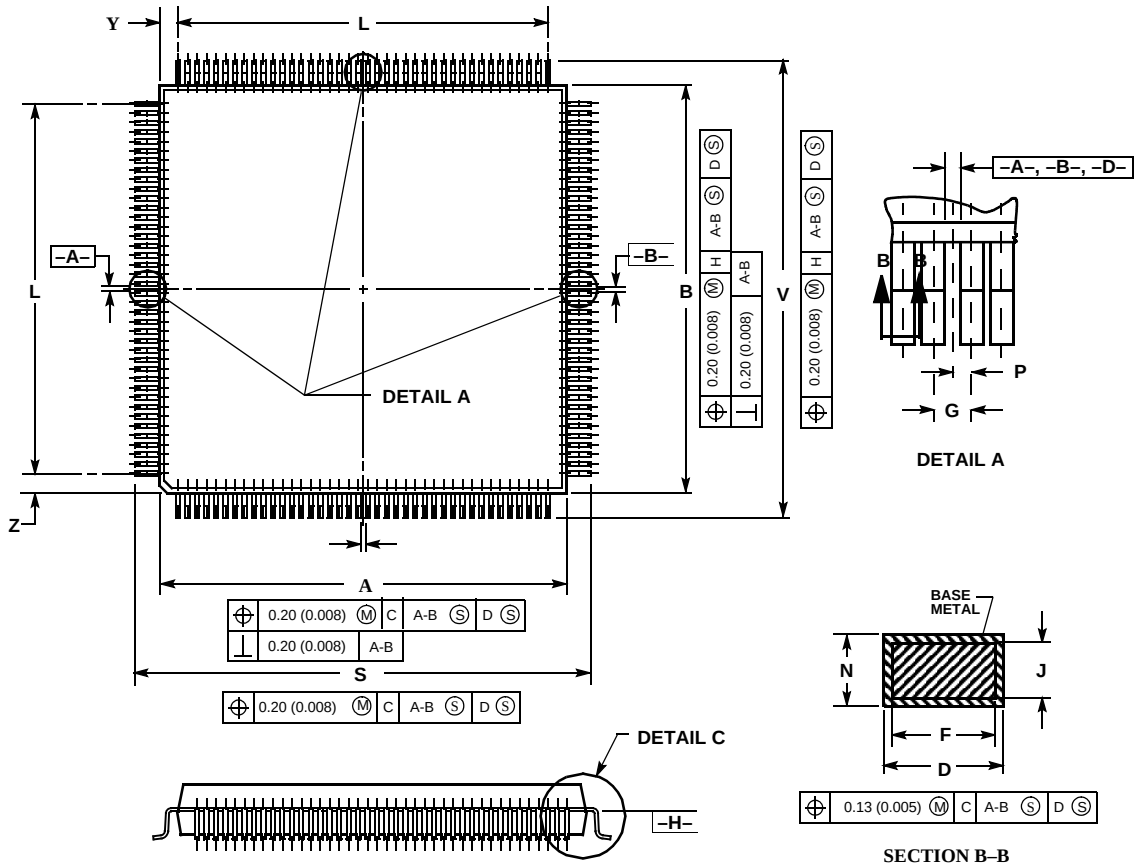
Figure 4 through Figure 6 show pinouts of the MCF5233CVMxxx, MCF5234CVMxxx, and MCF5235CVMxxx packages.

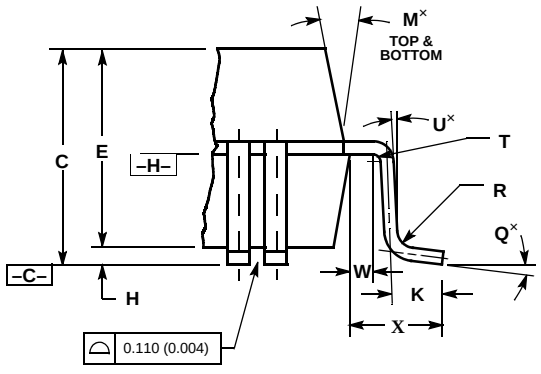
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	TPUCH17	TPUCH1	TPUCH0	VDD	BS1	BS0	U1RXD/ CAN0RX	U1TXD/ CAN0TX	CS6	CS4	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	TPUCH18	TPUCH19	TPUCH16	QSPI_ CLK	BS2	QSPI_ CS1	U1RTS	CS3	CS1	A23	A20	A19	B
C	TPUCH10	TPUCH9	TPUCH25	TPUCH24	TPUCH22	TPUCH20	I2C_SDA/ U2RXD	QSPI_ DIN	BS3	SD_CKE	U1CTS	CS7	CS5	A22	A18	A17	C
D	TPUCH12	TPUCH11	TPUCH27	TPUCH26	TPUCH23	TPUCH21	I2C_SCL/ U2TXD	QSPI_ DOUT	QSPI_ CS0	U2RXD/ CAN1RX	U2TXD/ CAN1TX	CS2	CS0	A14	A15	A16	D
E	TPUCH14	TPUCH13	TPUCH29	TPUCH28	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	TPUCH31	TPUCH30	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	U0CTS	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	U0RTS	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	TEA	TA	TIP	TS	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	SD_WE	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/W	L
M	D21	D22	D23	NC	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	SD_ CS0	SD_ SRAS	SD_ SCAS	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	IRQ5	IRQ1	TRST/ DSCLK	PST0	JTAG_ EN	DDATA3	SD_CS1	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	IRQ4	DT2IN	TMS/ BKPT	PST1	RCON	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	IRQ7	IRQ3	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	OE	IRQ6	IRQ2	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	RSTOUT	RESET	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MCF5233CVMxxx Pinout (256 MAPBGA)

6.4 Package Dimensions—160 QFP

Figure 9 shows MCF5232CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 9. 160 QFP Package Dimensions

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5232CAB80	MCF5232 RISC Microprocessor	160 QFP	80MHz	Yes	–40° to +85° C
MCF5232CVM100	MCF5232 RISC Microprocessor	196 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5232CVM150	MCF5232 RISC Microprocessor	196 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5233CVM100	MCF5233 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5233CVM150	MCF5233 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5234CVM100	MCF5234 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5234CVM150	MCF5234 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVM100	MCF5235 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5235CVM150	MCF5235 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVF150	MCF5235 RISC Microprocessor,	256 MAPBGA	150MHz	No	–40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5235 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5235.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	196 MAPBGA	160 QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	102	104	105[6]	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

6 At 100MHz.

Table 9. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	—	 7 7	pF
Load Capacitance[4] Low drive strength High drive strength	C_L		 — —	 25 50	 pF pF
Core Operating Supply Current [5] Master Mode	I_{DD}	 —	 135	 150	 mA
Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 100 TBD	 — —	 mA μA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total processor Limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10		 1.0 10	 mA mA

1 Refer to Table 10 for additional PLL specifications.

2 Refer to the MCF5235 signals section for pins having weak internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.

5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

6 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.

9 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$.

10 PLL is operating in 1:1 PLL mode.

11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

13 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.

14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.

15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..

2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.

3 Refer to figure A-19.

Timings listed in Table 11 are shown in Figure 10.

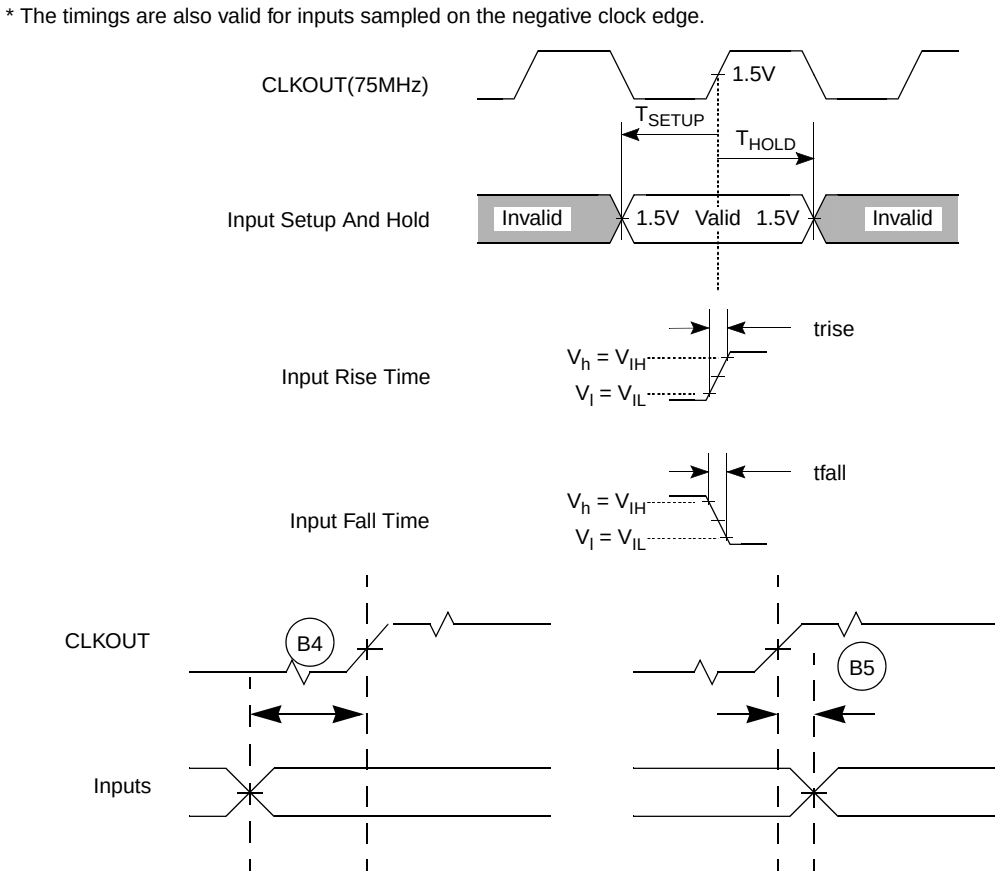


Figure 10. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

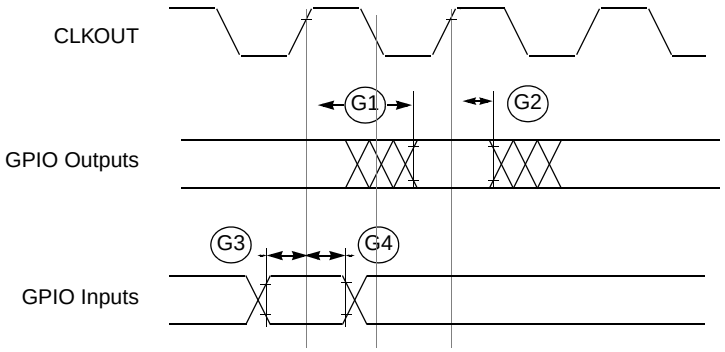


Figure 16. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

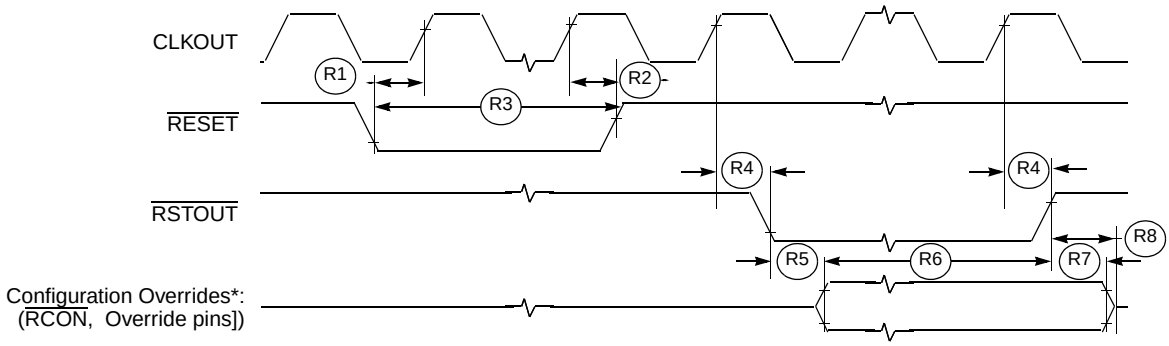


Figure 17. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

Figure 22 shows MII serial management channel timings listed in Table 21.

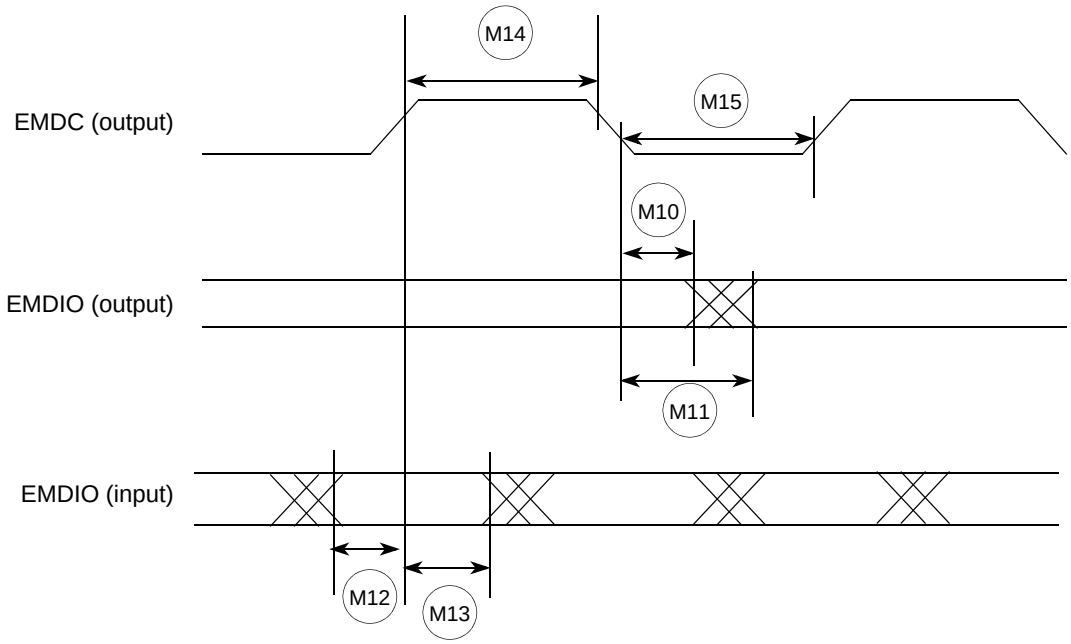


Figure 22. MII Serial Management Channel Timing Diagram

7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 23.

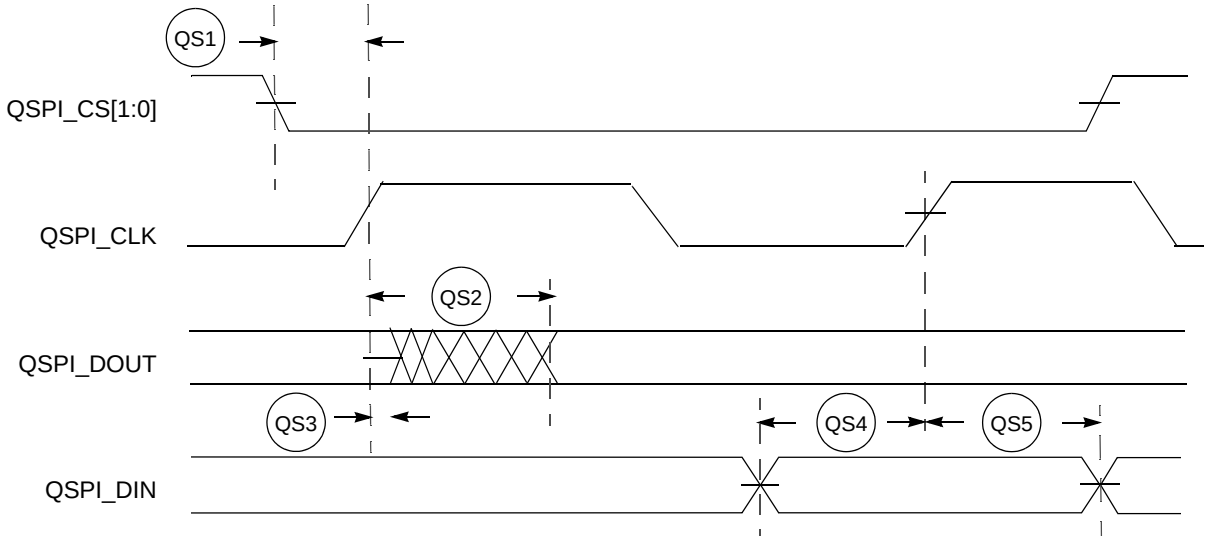


Figure 23. QSPI Timing

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

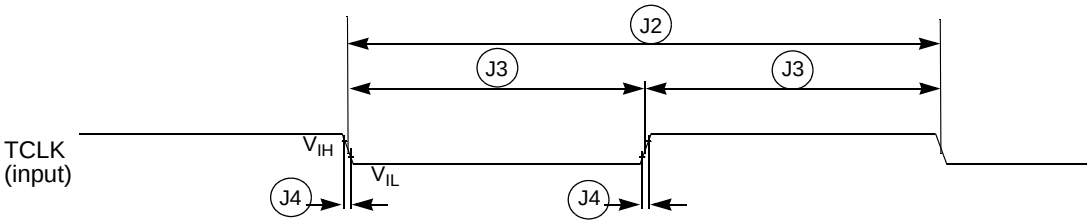


Figure 24. Test Clock Input Timing

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