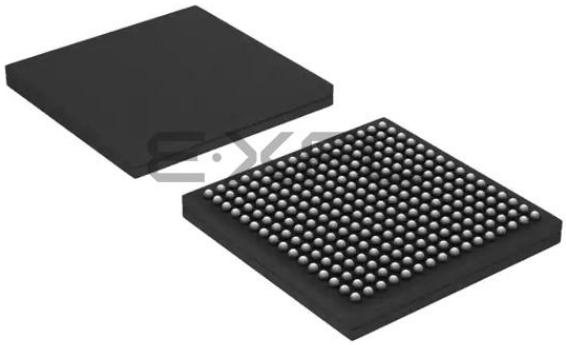


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, SPI, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 61 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.4V ~ 1.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-MAPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5233cvm100 |

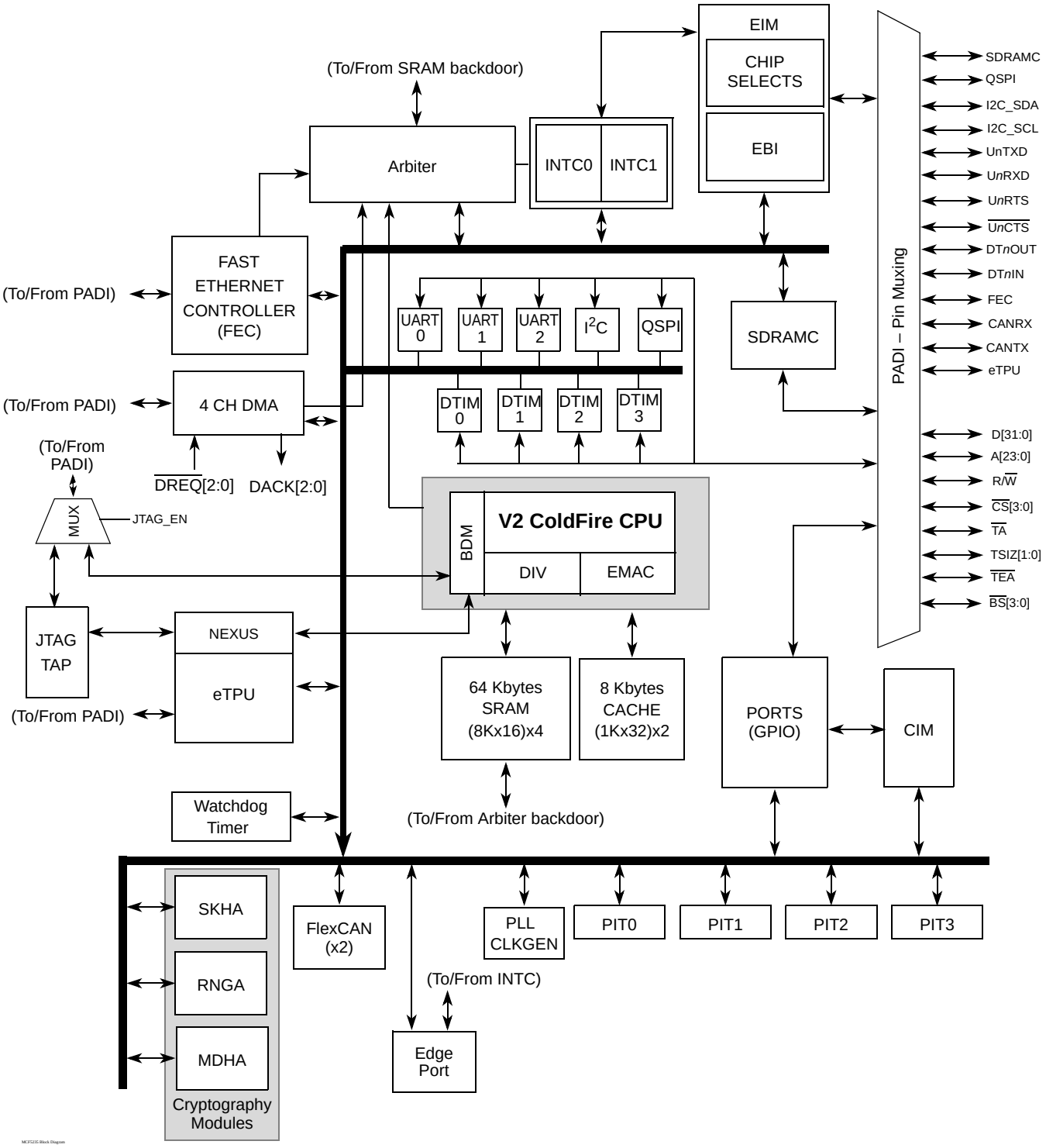
# 1 MCF523*x* Family Configurations

**Table 1. MCF523*x* Family Configurations**

| Module | MCF5232 | MCF5233 | MCF5234 | MCF5235 |
|---|---|---|---|---|
| ColdFire V2 Core with EMAC (Enhanced Multiply-Accumulate Unit) | x | x | x | x |
| Enhanced Time Processor Unit with memory (eTPU) | 16-ch 6K | 32-ch 6K | 16-ch 6K | 32-ch 6K |
| System Clock | up to 150 MHz | | | |
| Performance (Dhrystone/2.1 MIPS) | up to 144 | | | |
| Instruction/Data Cache | 8 Kbytes | | | |
| Static RAM (SRAM) | 64 Kbytes | | | |
| Interrupt Controllers (INTC) | 2 | 2 | 2 | 2 |
| Edge Port Module (EPORT) | x | x | x | x |
| External Interface Module (EIM) | x | x | x | x |
| 4-channel Direct-Memory Access (DMA) | x | x | x | x |
| SDRAM Controller | x | x | x | x |
| Fast Ethernet Controller (FEC) | — | — | x | x |
| Cryptography - Security module for data packets processing | — | — | — | x |
| Watchdog Timer (WDT) | x | x | x | x |
| Four Periodic Interrupt Timers (PIT) | x | x | x | x |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 |
| QSPI | x | x | x | x |
| UART(s) | 3 | 3 | 3 | 3 |
| $I^2C$ | x | x | x | x |
| FlexCAN 2.0B - Controller-Area Network communication module | 1 | 2 | 1 | 2 |
| General Purpose I/O Module (GPIO) | x | x | x | x |
| JTAG - IEEE 1149.1 Test Access Port | x | x | x | x |
| Package | 160 QFP 196 MAPBGA | 256 MAPBGA | 256 MAPBGA | 256 MAPBGA |

# 2 Block Diagram

The superset device in the MCF523*x* family comes in a 256 mold array process ball grid array (MAPBGA) package. Figure  shows a top-level block diagram of the MCF5235, the superset device.




# 3 Features

For a detailed feature list see the MCF5235 Reference Manual (MCF5235RM).

**Table 2. MCF523x Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | MCF5232 160 QFP | MCF5232 196 MAPBGA | MCF5233 256 MAPBGA | MCF5234 256 MAPBGA | MCF5235 256 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **Test** | | | | | | | | | |
| TEST | — | — | — | I | 18 | F5 | J4 | J4 | J4 |
| PLL_TEST | — | — | — | I | — | | R14 | R14 | R14 |
| **Power Supplies** | | | | | | | | | |
| VDDPLL | — | — | — | I | 87 | M13 | P15 | | |
| VSSPLL | — | — | — | I | 84 | L14 | R15 | | |
| OVDD | — | — | — | I | 1, 9, 17, 32, 41, 55, 62, 69, 81, 90, 95, 105, 114, 128, 132, 138, 146 | E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8 | E6:11, F5, F7:10, F12, G5, G6, G11, G12, H5, H6, H11, H12, J5, J6, J11, J12, K5, K6, K11, K12, L5, L7:10, L12, M6:M11 | | |
| VSS | — | — | — | I | 8, 16, 25, 31, 40, 54, 61, 67, 80, 88, 94, 104, 113, 127, 131, 137, 145, 153, 160 | A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14 | A1, A16, E5, E12, F6, F11, F16, G7:10, H7: 10, J1, J7:10, K7:10, L6, L11, M5, M12, N16, T1, T6, T16 | | |
| VDD | — | — | — | I | 15, 53, 103, 144 | D6, F11, G4, L4 | A8, G16, H1, T5 | | |

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

# 5 Design Recommendations

## 5.1 Layout

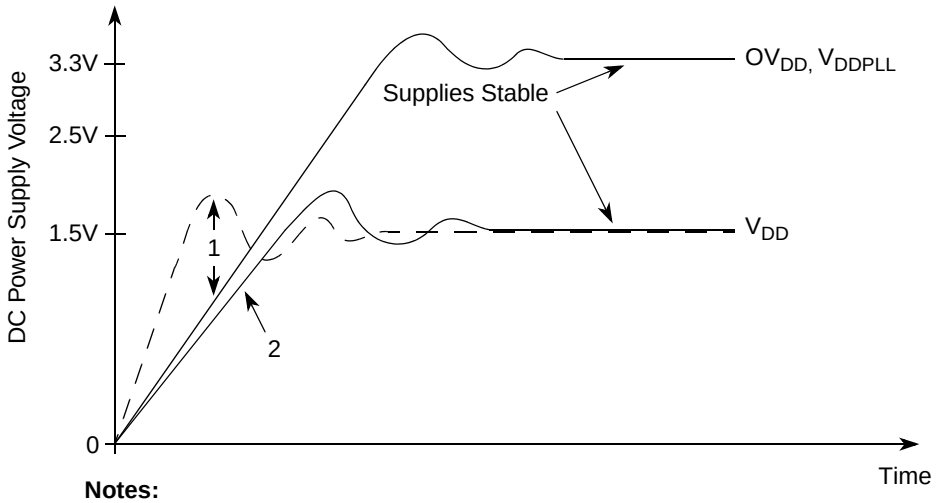
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF523*x*.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

## 5.2 Power Supply

- 33 μF, 0.1 μF, and 0.01 μF across each power supply

### 5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 1 shows situations in sequencing the I/O $V_{DD}$ ($OV_{DD}$), PLL $V_{DD}$ ($V_{DDPLL}$), and Core $V_{DD}$ ($V_{DD}$). $OV_{DD}$ is specified relative to $V_{DD}$.




**Notes:**
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

**Figure 1. Supply Voltage Sequencing and Separation Cautions**

#### 5.2.1.1 Power Up Sequence

If $OV_{DD}$ is powered up with $V_{DD}$ at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the $OV_{DD}$ to be in a high impedance state. There is no limit on how long after $OV_{DD}$ powers up before $V_{DD}$ must power up. $V_{DD}$ should not lead the $OV_{DD}$ or $V_{DDPLL}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. $V_{DD}$ and $OV_{DD}$/$V_{DDPLL}$ should track up to 0.9 V, then separate for the completion of ramps with $OV_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

#### 5.2.1.2 Power Down Sequence

If $V_{DD}$ is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after $V_{DD}$ powers down before $OV_{DD}/V_{DDPLL}$ must power down. $V_{DD}$ should not lag $OV_{DD}$ or $V_{DDPLL}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $V_{DD}$ to 0 V.
2. Drop $OV_{DD}/V_{DDPLL}$ supplies.

## 5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 μF and 0.01 μF at each supply input

## 5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, “Electrical Characteristics.”

## 5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

## 5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

# 5.7 Interface Recommendations

## 5.7.1 SDRAM Controller

### 5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

**Table 3. Synchronous DRAM Signal Connections**

| Signal | Description |
|---|---|
| $\overline{\text{SD\_SRAS}}$ | Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals. |
| $\overline{\text{SD\_SCAS}}$ | Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM. |
| $\overline{\text{DRAMW}}$ | DRAM read/write. Asserted for write operations and negated for read operations. |
| $\overline{\text{SD\_CS}}$[1:0] | Row address strobe. Select each memory block of SDRAMs connected to the MCF523*x*. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals. |
| SD_CKE | Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality. |
| $\overline{\text{BS}}$[3:0] | Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs. |
| CLKOUT | Bus clock output. Connects to the CLK input of SDRAMs. |

### 5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5235 Reference Manual* for details on address multiplexing.

## 5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

**Table 4. MII Mode**

| Signal Description | MCF523*x* Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[3:0] |

**Table 4. MII Mode (continued)**

| Signal Description | MCF523*x* Pin |
|---|---|
| Transmit error | ETXER |
| Collision | ECOL |
| Carrier sense | ECRS |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[3:0] |
| Receive error | ERXER |
| Management channel clock | EMDC |
| Management channel serial data | EMDIO |

The serial mode interface operates in what is generally referred to as AMD mode. The MCF523*x* configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

**Table 5. Seven-Wire Mode Configuration**

| Signal Description | MCF523*x* Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[0] |
| Collision | ECOL |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[0] |
| Unused, configure as PB14 | ERXER |
| Unused input, tie to ground | ECRS |
| Unused, configure as PB[13:11] | ERXD[3:1] |
| Unused output, ignore | ETXER |
| Unused, configure as PB[10:8] | ETXD[3:1] |
| Unused, configure as PB15 | EMDC |
| Input after reset, connect to ground | EMDIO |

Refer to the M523*x*EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5235 site by navigating to: http://www.freescale.com/coldfire.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | TPUCH6 | TPUCH4 | TPUCH2 | TPUCH17/ ETXD1 | TPUCH1 | TPUCH0 | VDD | $\overline{BS1}$ | $\overline{BS0}$ | U1RXD/ CAN0RX | U1TXD/ CAN0TX | $\overline{CS6}$ | $\overline{CS4}$ | A21 | VSS | A |
| B | TPUCH8 | TPUCH7 | TPUCH5 | TPUCH3 | TPUCH18/ ETXD2 | TPUCH19/ ETXD3 | TPUCH16/ ETXD0 | QSPI_ CLK | $\overline{BS2}$ | QSPI_ CS1 | $\overline{U1RTS}$ | $\overline{CS3}$ | $\overline{CS1}$ | A23 | A20 | A19 | B |
| C | TPUCH10 | TPUCH9 | TPUCH25/ ERXD1 | TPUCH24/ ERXD0 | TPUCH22/ ETXCLK | TPUCH20/ ETXER | I2C_SDA/ U2RXD/ EMDIO | QSPI_ DIN | $\overline{BS3}$ | SD_CKE | $\overline{U1CTS}$ | $\overline{CS7}$ | $\overline{CS5}$ | A22 | A18 | A17 | C |
| D | TPUCH12 | TPUCH11 | TPUCH27/ ERXD3 | TPUCH26/ ERXD2 | TPUCH23/ ERXER | TPUCH21/ ETXEN | I2C_SCL/ U2TXD/ EMDC | QSPI_ DOUT | QSPI_ CS0 | U2RXD/ CAN1RX | U2TXD/ CAN1TX | $\overline{CS2}$ | $\overline{CS0}$ | A14 | A15 | A16 | D |
| E | TPUCH14 | TPUCH13 | TPUCH29/ ERXCLK | TPUCH2/ ERXDV | VSS | OVDD | OVDD | OVDD | OVDD | OVDD | OVDD | VSS | A10 | A11 | A12 | A13 | E |
| F | TCRCLK | TPUCH15 | TPUCH31/ ECOL | TPUCH30/ ECRS | OVDD | VSS | OVDD | OVDD | OVDD | OVDD | VSS | OVDD | A7 | A8 | A9 | VSS | F |
| G | $\overline{U0CTS}$ | U0RXD | DT0OUT | DT0IN | OVDD | OVDD | VSS | VSS | VSS | VSS | OVDD | OVDD | A4 | A5 | A6 | VDD | G |
| H | VDD | U0TXD | $\overline{U0RTS}$ | NC | OVDD | OVDD | VSS | VSS | VSS | VSS | OVDD | OVDD | A0 | A1 | A2 | A3 | H |
| J | VSS | CLK MOD0 | CLK MOD1 | TEST | OVDD | OVDD | VSS | VSS | VSS | VSS | OVDD | OVDD | UTPU ODIS | LTPU ODIS | DT3IN | DT3OUT | J |
| K | D28 | D29 | D30 | D31 | OVDD | OVDD | VSS | VSS | VSS | VSS | OVDD | OVDD | $\overline{TEA}$ | $\overline{TA}$ | $\overline{TIP}$ | $\overline{TS}$ | K |
| L | D24 | D25 | D26 | D27 | OVDD | VSS | OVDD | OVDD | OVDD | OVDD | VSS | OVDD | $\overline{SD\_WE}$ | I2C_SCL/ CAN0TX | I2C_SDA/ CAN0RX | R/$\overline{W}$ | L |
| M | D21 | D22 | D23 | eTPU/ $\overline{EthENB}$ | VSS | OVDD | OVDD | OVDD | OVDD | OVDD | OVDD | VSS | $\overline{SD\_CS0}$ | $\overline{SD\_SRAS}$ | $\overline{SD\_SCAS}$ | CLKOUT | M |
| N | D19 | D20 | D13 | D9 | NC | D3 | D0 | TSIZ1 | $\overline{IRQ5}$ | $\overline{IRQ1}$ | $\overline{TRST}$/ DSCLK | PST0 | JTAG_ EN | DDATA3 | $\overline{SD\_CS1}$ | VSS | N |
| P | D17 | D18 | D12 | D8 | D5 | D2 | DT1IN | TSIZ0 | $\overline{IRQ4}$ | DT2IN | TMS/ $\overline{BKPT}$ | PST1 | $\overline{RCON}$ | DDATA2 | VDDPLL | EXTAL | P |
| R | D16 | D15 | D11 | D7 | D4 | D1 | DT1OUT | $\overline{IRQ7}$ | $\overline{IRQ3}$ | DT2OUT | TDO/ DSO | PST2 | DDATA0 | PLL_ TEST | VSSPLL | XTAL | R |
| T | VSS | D14 | D10 | D6 | VDD | VSS | $\overline{OE}$ | $\overline{IRQ6}$ | $\overline{IRQ2}$ | TCLK/ PSTCLK | TDI/DSI | PST3 | DDATA1 | $\overline{RSTOUT}$ | $\overline{RESET}$ | VSS | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

**Figure 6. MCF5235CVMxxx Pinout (256 MAPBGA)**

**Table 9. DC Electrical Specifications[1] (continued)**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance [3]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | — | <br>7<br>7 | pF |
| Load Capacitance[4]<br>Low drive strength<br>High drive strength | $C_L$ | | <br>—<br>— | <br>25<br>50 | <br>pF<br>pF |
| Core Operating Supply Current [5]<br>Master Mode | $I_{DD}$ | <br>— | <br>135 | <br>150 | <br>mA |
| Pad Operating Supply Current<br>Master Mode<br>Low Power Modes | $OI_{DD}$ | <br>—<br>— | <br>100<br>TBD | <br>—<br>— | <br>mA<br>μA |
| DC Injection Current [3, 6, 7, 8]<br>$V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$<br>Single Pin Limit<br>Total processor Limit, Includes sum of all stressed pins | $I_{IC}$ | <br><br>–1.0<br>–10 | | <br><br>1.0<br>10 | <br><br>mA<br>mA |

1 Refer to Table 10 for additional PLL specifications.

2 Refer to the MCF5235 signals section for pins having weak internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.

5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

6 All functional non-supply pins are internally clamped to $V_{SS}$ and their respective $V_{DD}$.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Insure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

Timings listed in Table 11 are shown in Figure 10.

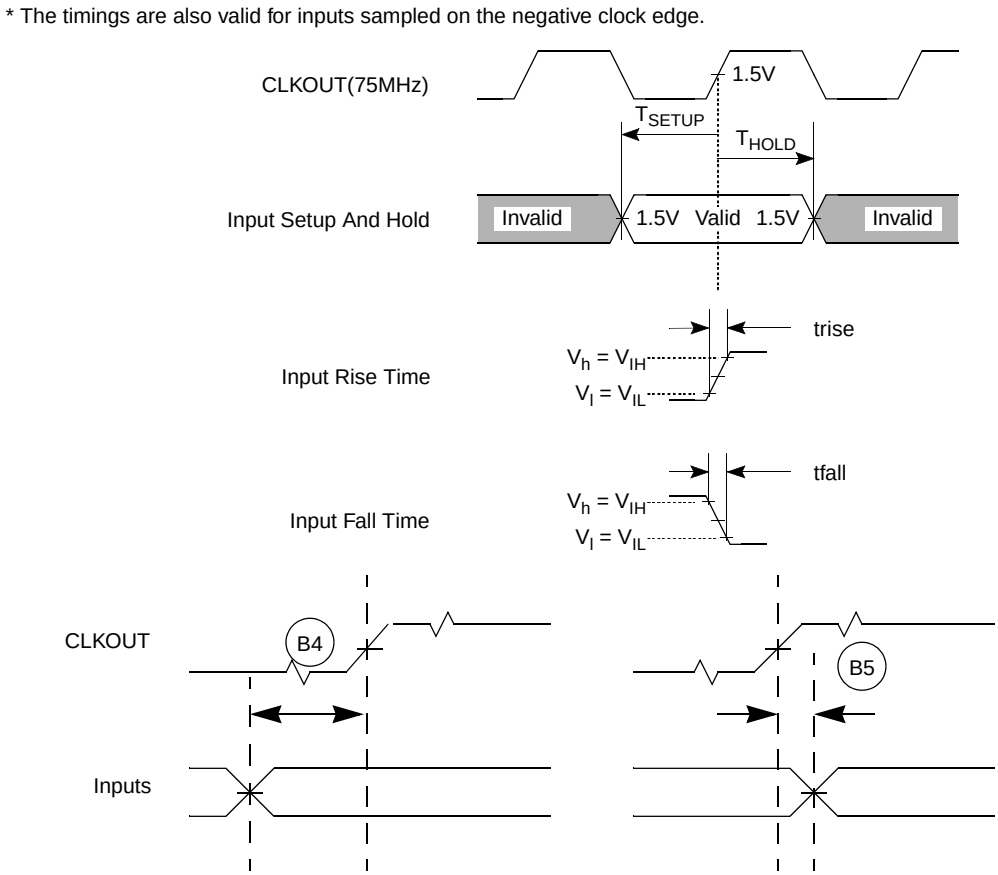



**Figure 10. General Input Timing Requirements**

## 7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

**Table 12. External Bus Output Timing Specifications**

| Name | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **Control Outputs** | | | | | |
| B6a | CLKOUT high to chip selects valid [1] | $t_{CHCV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B6b | CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2] | $t_{CHBV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B6c | CLKOUT high to output enable ($\overline{OE}$) valid[3] | $t_{CHOV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B7 | CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid | $t_{CHCOI}$ | $0.5t_{CYC}$+1.5 | — | ns |
| B7a | CLKOUT high to chip selects invalid | $t_{CHCI}$ | $0.5t_{CYC}$+1.5 | — | ns |

**Table 12. External Bus Output Timing Specifications (continued)**

| Name | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **Address and Attribute Outputs** | | | | | |
| B8 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid | $t_{CHAV}$ | — | 9 | ns |
| B9 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid | $t_{CHAI}$ | 1.5 | — | ns |
| **Data Outputs** | | | | | |
| B11 | CLKOUT high to data output (D[31:0]) valid | $t_{CHDOV}$ | — | 9 | ns |
| B12 | CLKOUT high to data output (D[31:0]) invalid | $t_{CHDOI}$ | 1.5 | — | ns |
| B13 | CLKOUT high to data output (D[31:0]) high impedance | $t_{CHDOZ}$ | — | 9 | ns |

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 12 are shown in Figure 11, Figure 12, and Figure 13.

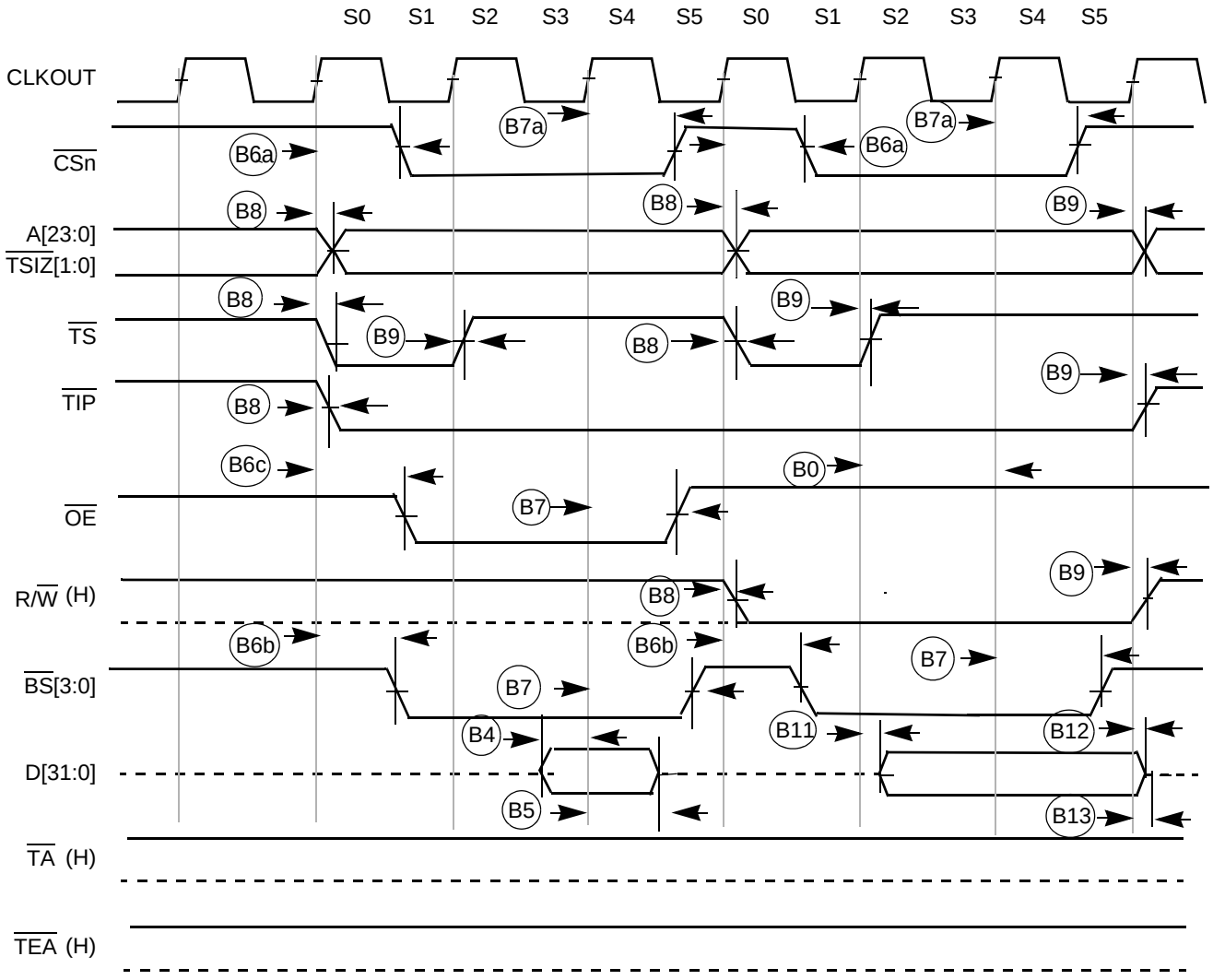



**Figure 11. Read/Write (Internally Terminated) SRAM Bus Timing**

Figure 13 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

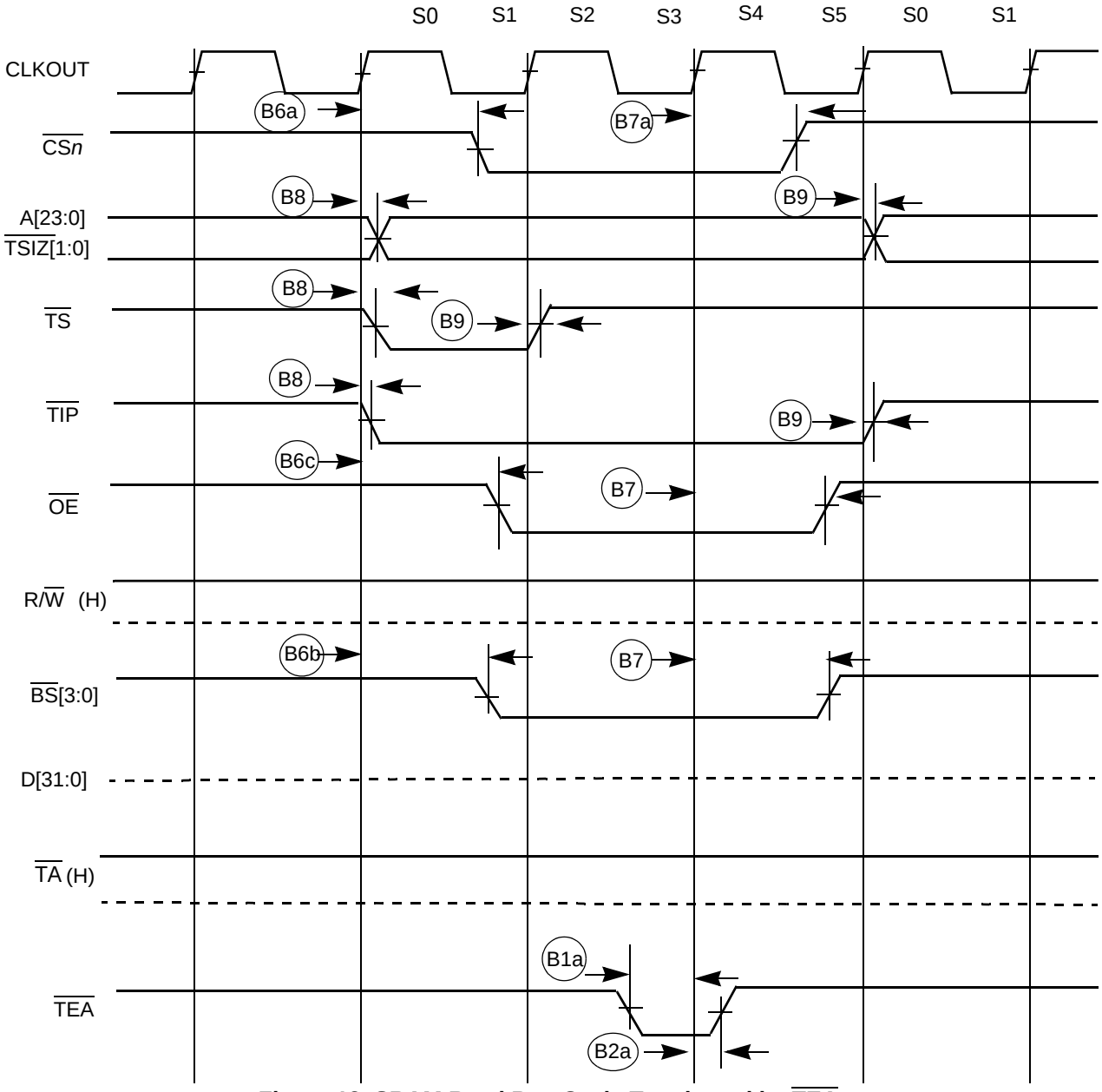
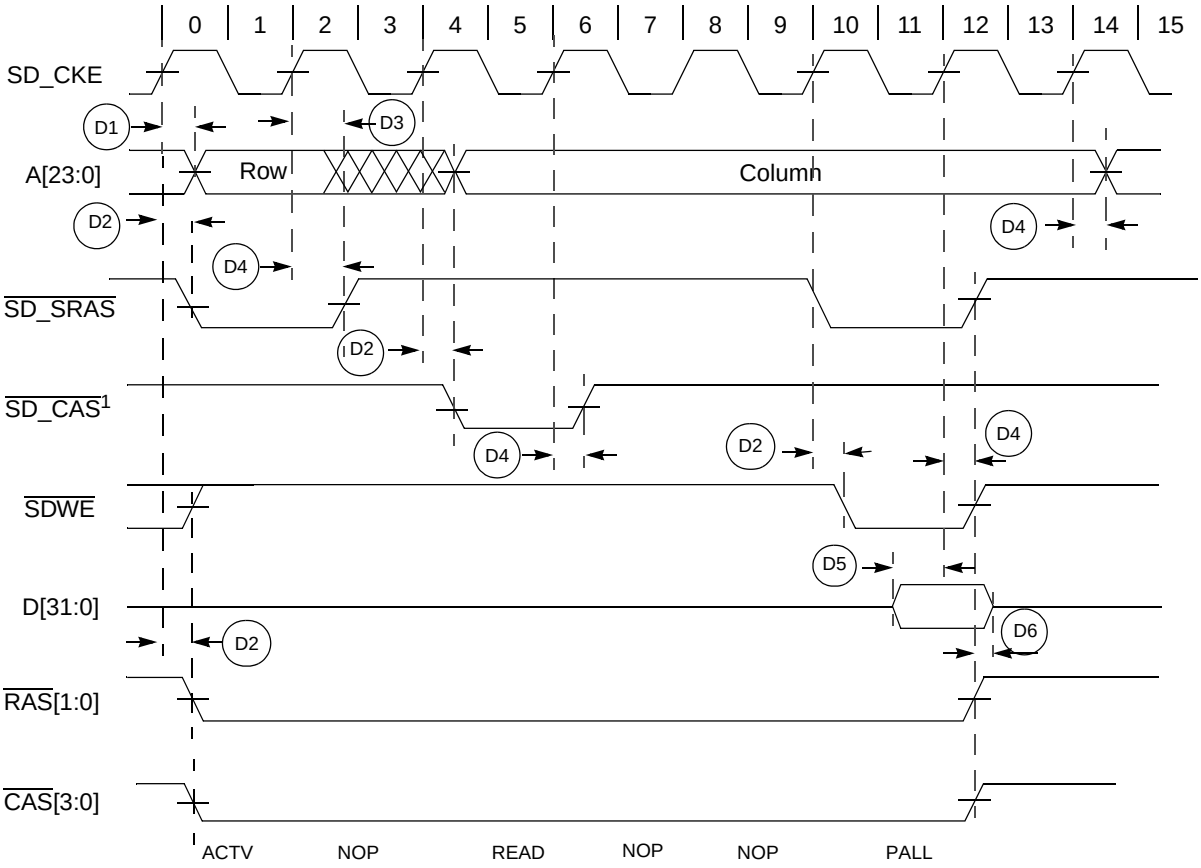



**Figure 13. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$**

Figure 14 shows an SDRAM read cycle.




1 DACR[CASL] = 2

**Figure 14. SDRAM Read Cycle**

**Table 13. SDRAM Timing**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| D1 | CLKOUT high to SDRAM address valid | $t_{CHDAV}$ | — | 9 | ns |
| D2 | CLKOUT high to SDRAM control valid | $t_{CHDCV}$ | — | 9 | ns |
| D3 | CLKOUT high to SDRAM address invalid | $t_{CHDAI}$ | 1.5 | — | ns |
| D4 | CLKOUT high to SDRAM control invalid | $t_{CHDCI}$ | 1.5 | — | ns |
| D5 | SDRAM data valid to CLKOUT high | $t_{DDVCH}$ | 4 | — | ns |
| D6 | CLKOUT high to SDRAM data invalid | $t_{CHDDI}$ | 1.5 | — | ns |
| D7[1] | CLKOUT high to SDRAM data valid | $t_{CHDDVW}$ | — | 9 | ns |
| D8[1] | CLKOUT high to SDRAM data invalid | $t_{CHDDIW}$ | 1.5 | — | ns |

1 D7 and D8 are for write cycles only.

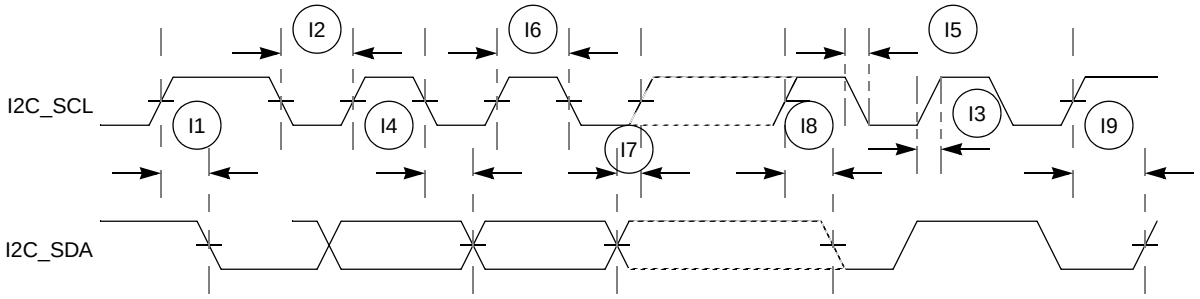



**Figure 18. I²C Input/Output Timings**

## 7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

### 7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

**Table 18. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | ERXD[3:0], ERXDV, ERXER to ERXCLK setup | 5 | — | ns |
| M2 | ERXCLK to ERXD[3:0], ERXDV, ERXER hold | 5 | — | ns |
| M3 | ERXCLK pulse width high | 35% | 65% | ERXCLK period |
| M4 | ERXCLK pulse width low | 35% | 65% | ERXCLK period |

Figure 19 shows MII receive signal timings listed in Table 18.

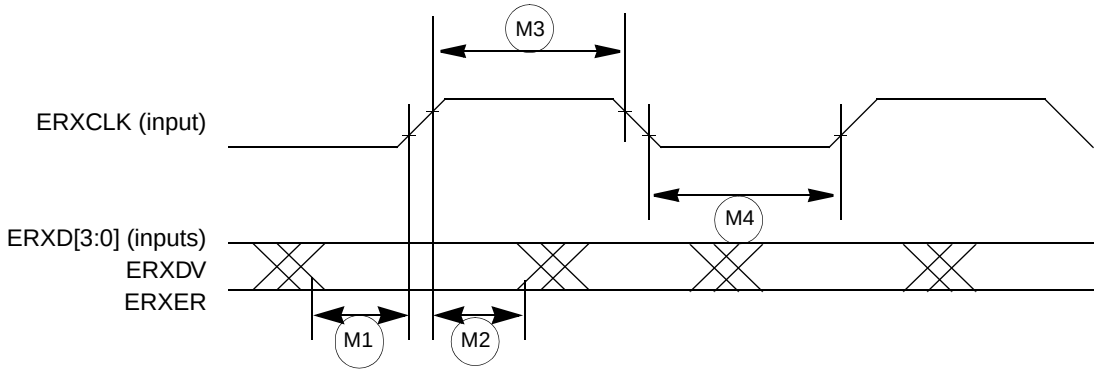



**Figure 19. MII Receive Signal Timing Diagram**

## 7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

**Table 19. MII Transmit Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | ETXCLK to ETXD[3:0], ETXEN, ETXER invalid | 5 | — | ns |
| M6 | ETXCLK to ETXD[3:0], ETXEN, ETXER valid | — | 25 | ns |
| M7 | ETXCLK pulse width high | 35% | 65% | ETXCLK period |
| M8 | ETXCLK pulse width low | 35% | 65% | ETXCLK period |

Figure 20 shows MII transmit signal timings listed in Table 19.

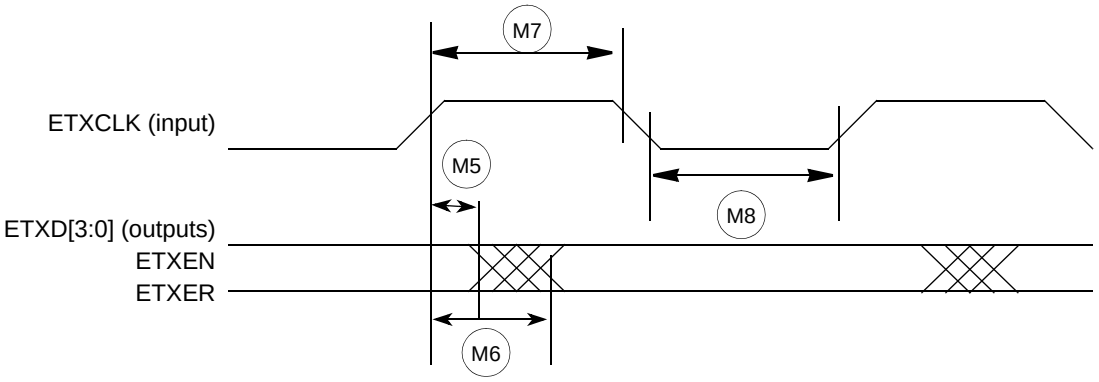



**Figure 20. MII Transmit Signal Timing Diagram**

## 7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

**Table 20. MII Async Inputs Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | ECRS, ECOL minimum pulse width | 1.5 | — | ETXCLK period |

Figure 21 shows MII asynchronous input timings listed in Table 20.


**Figure 21. MII Async Inputs Timing Diagram**

## 7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

**Table 22. Timer Module AC Timing Specifications**

| Name | Characteristic | 0–66 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| T1 | DT0IN / DT1IN / DT2IN / DT3IN cycle time | 3 | — | $t_{CYC}$ |
| T2 | DT0IN / DT1IN / DT2IN / DT3IN pulse width | 1 | — | $t_{CYC}$ |

## 7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

**Table 23. QSPI Modules AC Timing Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| QS1 | QSPI_CS[1:0] to QSPI_CLK | 1 | 510 | tcyc |
| QS2 | QSPI_CLK high to QSPI_DOUT valid. | — | 10 | ns |
| QS3 | QSPI_CLK high to QSPI_DOUT invalid. (Output hold) | 2 | — | ns |
| QS4 | QSPI_DIN to QSPI_CLK (Input setup) | 9 | — | ns |
| QS5 | QSPI_DIN to QSPI_CLK (Input hold) | 9 | — | ns |

The values in Table 23 correspond to Figure 23.

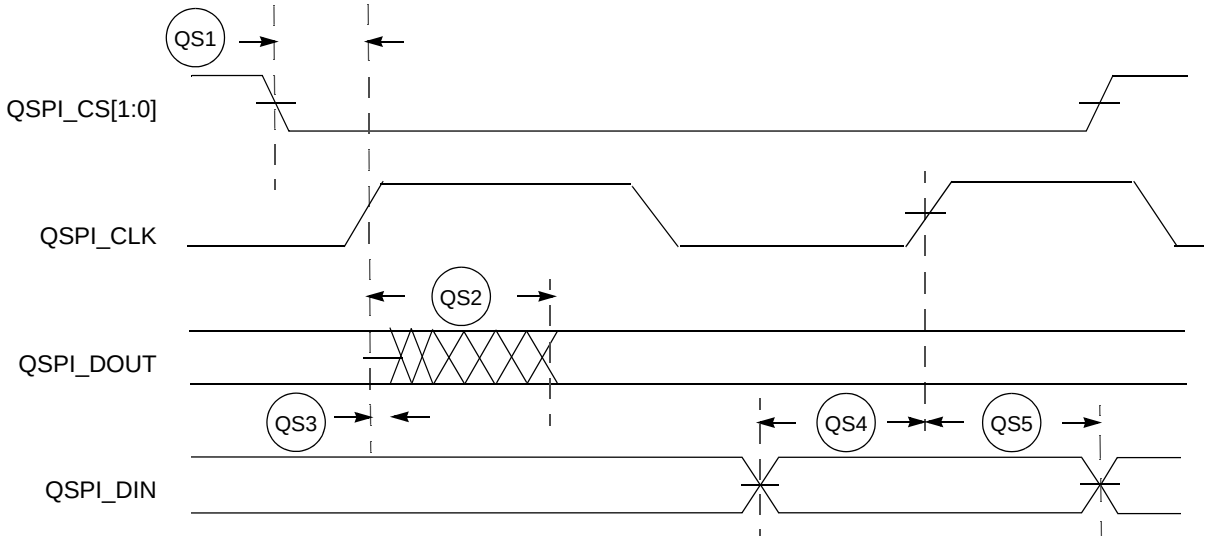



**Figure 23. QSPI Timing**

## 7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 29.

**Table 25. Debug AC Timing Specification**

| Num | Characteristic | 150 MHz | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| DE0 | PSTCLK cycle time | — | 0.5 | $t_{cyc}$ |
| DE1 | PST valid to PSTCLK high | 4 | — | ns |
| DE2 | PSTCLK high to PST invalid | 1.5 | — | ns |
| DE3 | DSCLK cycle time | 5 | — | $t_{cyc}$ |
| DE4 | DSI valid to DSCLK high | 1 | — | $t_{cyc}$ |
| DE5[1] | DSCLK high to DSO invalid | 4 | — | $t_{cyc}$ |
| DE6 | $\overline{\text{BKPT}}$ input data setup time to CLKOUT rise | 4 | — | ns |
| DE7 | CLKOUT high to $\overline{\text{BKPT}}$ high Z | 0 | 10 | ns |

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 25.

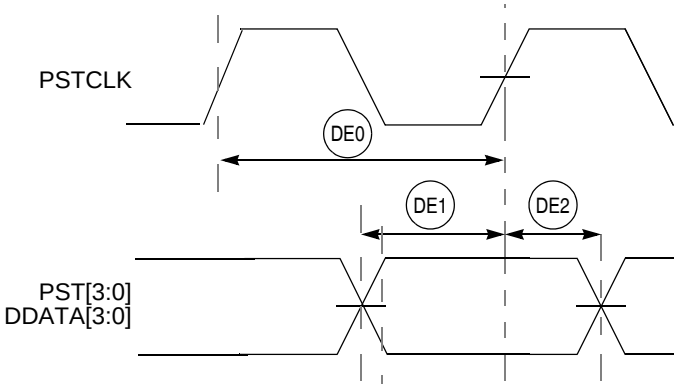



**Figure 28. Real-Time Trace AC Timing**

Figure 29 shows BDM serial port AC timing for the values in Table 25.

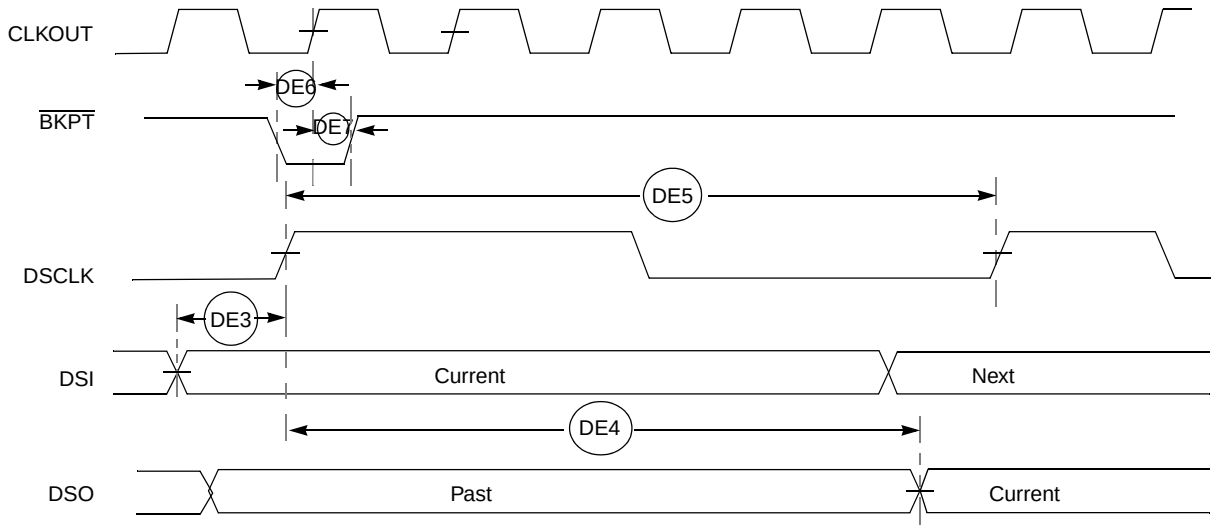



**Figure 29. BDM Serial Port AC Timing**

# 8 Documentation

Documentation regarding the MCF523*x* and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

# 9 Document Revision History

The below table provides a revision history for this document.

**Table 26. MCF5235EC Revision History**

| Rev. No. | Substantive Change(s) |
|---|---|
| 0 | Preliminary release. |
| 1 | • Updated Signal List table |
| 1.1 | • Removed duplicate information in the module description sections. The information is all in the Signals Description Table. |
| 1.2 | • Corrected Figure 8 pin 81. VDD instead of VSS<br>• Changed instances of Motorola to Freescale |
| 1.3 | • Removed detailed signal description section. This information can be found in the MCF5235RM Chapter 2.<br>• Removed detailed feature list. This information can be found in the MCF5235RM Chapter 1.<br>• Corrected Figure 2 pin F10. VSS instead of VDD. Change made in Table 2 as well.<br>• Corrected Figure 8 pin 81. OVDD instead of VDD. Change made in Table 2 as well.<br>• Cleaned up many inconsistencies within the pinout figure signal names<br>• Corrected document IDs in Documentation Table |
| 1.4 | • Added values for ‘Maximum operating junction temperature’ in Table 8.<br>• Added typical values for ‘Core operating supply current (master mode)’ in Table 9.<br>• Added typical values for ‘Pad operating supply current (master mode)’ in Table 9.<br>• Removed unnecessary PLL specifications, #6-9, in Table 10. |

**Table 26. MCF5235EC Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 1.5 | • Removed Overview, Features, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5235 Reference Manual.<br>• Removed list of documentation table in Section 8, "Documentation.". An up-to-date list is always available on our web site. |
| 1.6 | • Table 9: Changed core supply voltage ($V_{DD}$) from 1.35-1.65 to 1.4-1.6. |
| 1.7 | • Table 10: Changed max $f_{ICO}$ frequency from "75 MHz" to "150 MHz". |
| 1.8 | • Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions."<br>• Updated 196MAPBGA package dimensions, Figure 3. |
| 2 | • Table 2: Changed SD_CKE pin location from 139 to "—" for the 160QFP device. Changed QSPI_CS1 pin location from "—" to 139 for the 160QFP device.<br>• Figure 8: Changed pin 139 label from "SD_CKE/QSPI_CS1" to "QSPI_CS1/SD_CKE".<br>• Removed second sentence from Section 7.10.1, "MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)," and Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," regarding no minimum frequency requirement for TXCLK.<br>• Removed third and fourth paragraphs from Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," as this feature is not supported on this device. |
| 3 | • Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" changed $PLLV_{DD}$ to $V_{DDPLL}$ to match rest of document.<br>• Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" Changed $V_{DDPLL}$ voltage level from 1.5V to 3.3V throughout section.<br>• Section 5.2.1.1, "Power Up Sequence" first bullet, changed "Use 1 µs" to "Use 1 ms".<br>• Corrected position of spec D5 in Figure 14.<br>• Table 14: Added $\overline{DACKn}$ and $\overline{DREQn}$ to footnote.<br>• Table 9, added PLL supply voltage row |
| 4 | • Added part number MCF5235CVF150 in Table 6 |