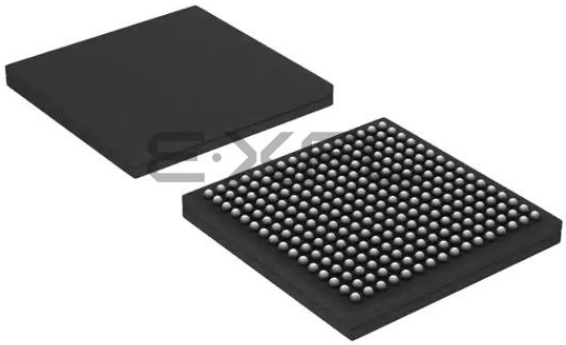

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5234cvm150

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
$\overline{\text{SD\_WE}}$	PSDRAM5	—	—	O	93	K13	L13	L13	L13
$\overline{\text{SD\_SCAS}}$	PSDRAM4	—	—	O	92	K12	M15	M15	M15
$\overline{\text{SD\_SRAS}}$	PSDRAM3	—	—	O	91	K11	M14	M14	M14
$\overline{\text{SD\_CKE}}$	PSDRAM2	—	—	O	—	E8	C10	C10	C10
$\overline{\text{SD\_CS}}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13	N15, M13	N15, M13	N15, M13
External Interrupts Port									
$\overline{\text{IRQ}}$[7:3]	PIRQ[7:3]	—	—	I	IRQ7=64 IRQ4=65	N7, M7, L7, P8, N8	R8, T8, N9, P9, R9	R8, T8, N9, P9, R9	R8, T8, N9, P9, R9
$\overline{\text{IRQ2}}$	PIRQ2	$\overline{\text{DREQ2}}$	—	I	—	M8	T9	T9	T9
$\overline{\text{IRQ1}}$	PIRQ1	—	—	I	66	L8	N10	N10	N10
eTPU									
TPUCH31	—	ECOL	—		—	—	F3	—	F3
TPUCH30	—	ECRS	—		—	—	F4	—	F4
TPUCH29	—	ERXCLK	—		—	—	E3	—	E3
TPUCH28	—	ERXDV	—		—	—	E4	—	E4
TPUCH[27:24]	—	ERXD[3:0]	—		—	—	D3, D4, C3, C4	—	D3, D4, C3, C4
TPUCH23	—	ERXER	—		—	—	D5	—	D5
TPUCH22	—	ETXCLK	—		—	—	C5	—	C5
TPUCH21	—	ETXEN	—		—	—	D6	—	D6
TPUCH20	—	ETXER	—		—	—	C6	—	C6
TPUCH[19:16]	—	ETXD[3:0]	—		—	—	B6,B5, A5, B7	—	B6,B5, A5, B7
TPUCH[15:0]	—	—	—		11, 10, 7:2, 159:154, 152, 151	E2, E1, D1 D2, D3, C1, C2, B1, B2, A2, C3, B3, A3, A4, C4, BR	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7
TCRCLK	PETPU2	—	—		12	E3	F1	F1	F1
UTPUODIS	PETPU1	—	—		—	H10	J13	J13	J13
LTPUODIS	PETPU0	—	—		—	G10	J14	J14	J14
FEC									
EMDIO	PFECI2C2	I2C_SDA	U2RXD	I/O	—	—	—	C7	C7
EMDC	PFECI2C3	I2C_SCL	U2TXD	O	—	—	—	D7	D7
ECOL	—	—	—	I	—	—	—	F3	F3

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
ECRS	—	—	—	I	—	—	—	F4	F4
ERXCLK	—	—	—	I	—	—	—	E3	E3
ERXDV	—	—	—	I	—	—	—	E4	E4
ERXD[3:0]	—	—	—	I	—	—	—	D3, D4, C3, C4	D3, D4, C3, C4
ERXER	—	—	—	I	—	—	—	D5	D5
ETXCLK	—	—	—	I	—	—	—	C5	C5
ETXEN	—	—	—	O	—	—	—	D6	D6
ETXER	—	—	—	O	—	—	—	C6	C6
ETXD[3:0]	—	—	—	O	—	—	—	B6, B5, A5, B7	B6, B5, A5, B7
Feature Control									
eTPU/$\overline{\text{EthENB}}$	—	—	—	I	—	—	—	—	M4
I^2C									
I2C_SDA	PFECI2C1	CAN0RX	—	I/O	—	J12	L15	L15	L15
I2C_SCL	PFECI2C0	CAN0TX	—	I/O	—	J11	L14	L14	L14
DMA									
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, TSIZ1and DT1OUT for $\overline{\text{DACK1}}$, TSIZ0 and DT0OUT for $\overline{\text{DACK0}}$, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and DT1IN for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—	—	—	—
QSPI									
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7	B10	B10	B10
QSPI_CS0	PQSPI3	—	—	O	147	A6	D9	D9	D9
QSPI_CLK	PQSPI2	I2C_SCL	—	O	148	C5	B8	B8	B8
QSPI_DIN	PQSPI1	I2C_SDA	—	I	149	B5	C8	C8	C8
QSPI_DOUT	PQSPI0	—	—	O	150	A5	D8	D8	D8
UARTs									
U2TXD	PUARTH1	CAN1TX	—	O	—	A8	D11	D11	D11
U2RXD	PUARTH0	CAN1RX	—	I	—	A7	D10	D10	D10
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	—	B8	C11	C11	C11
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	—	C8	B11	B11	B11
U1TXD	PUARTL5	CAN0TX	—	O	135	D9	A12	A12	A12

Table 2. MCF523x Signal Information and Muxing (continued)

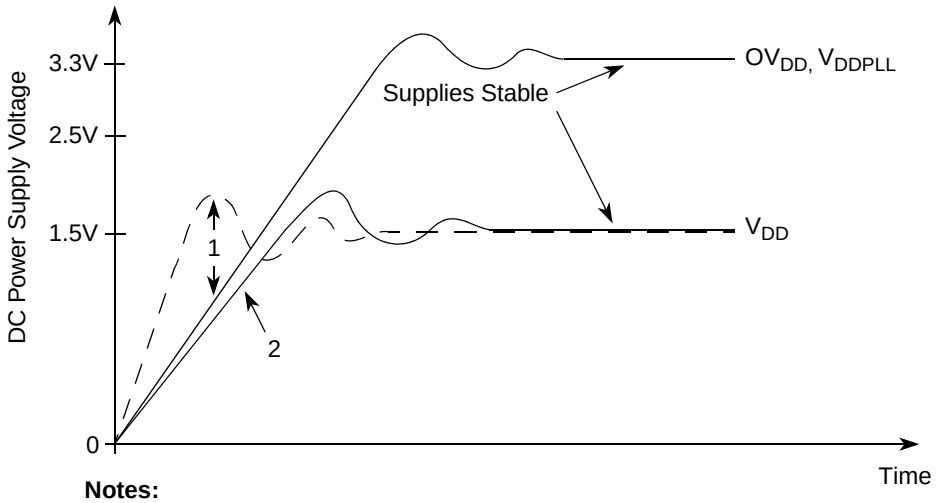
Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
U1RXD	PUARTL4	CAN0RX	—	I	136	D8	A11	A11	A11
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	—	F3	G1	G1	G1
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	—	G3	H3	H3	H3
U0TXD	PUARTL1	—	—	O	14	F1	H2	H2	H2
U0RXD	PUARTL0	—	—	I	13	F2	G2	G2	G2
DMA Timers									
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14	J15	J15	J15
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14	J16	J16	J16
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	—	M9	P10	P10	P10
DT2OUT	PTIMER4	DACK2	—	O	—	L9	R10	R10	R10
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	—	L6	P7	P7	P7
DT1OUT	PTIMER2	DACK1	—	O	—	M6	R7	R7	R7
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	—	E4	G4	G4	G4
DT0OUT	PTIMER0	DACK0	—	O	—	F4	G3	G3	G3
BDM/JTAG[2]									
DSCLK	—	TRST	—	I	70	N9	N11	N11	N11
PSTCLK	—	TCLK	—	O	68	P9	T10	T10	T10
$\overline{\text{BKPT}}$	—	TMS	—	I	71	P10	P11	P11	P11
DSI	—	TDI	—	I	73	M10	T11	T11	T11
DSO	—	TDO	—	O	72	N10	R11	R11	R11
JTAG_EN	—	—	—	I	78	K9	N13	N13	N13
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11	N14, P14, T13, R13	N14, P14, T13, R13	N14, P14, T13, R13
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10	T12, R12, P12, N12	T12, R12, P12, N12	T12, R12, P12, N12

5.2 Power Supply

- 33 μF, 0.1 μF, and 0.01 μF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 1 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 1. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

Table 4. MII Mode (continued)

Signal Description	MCF523*x* Pin
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]
Receive error	ERXER
Management channel clock	EMDC
Management channel serial data	EMDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF523*x* configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

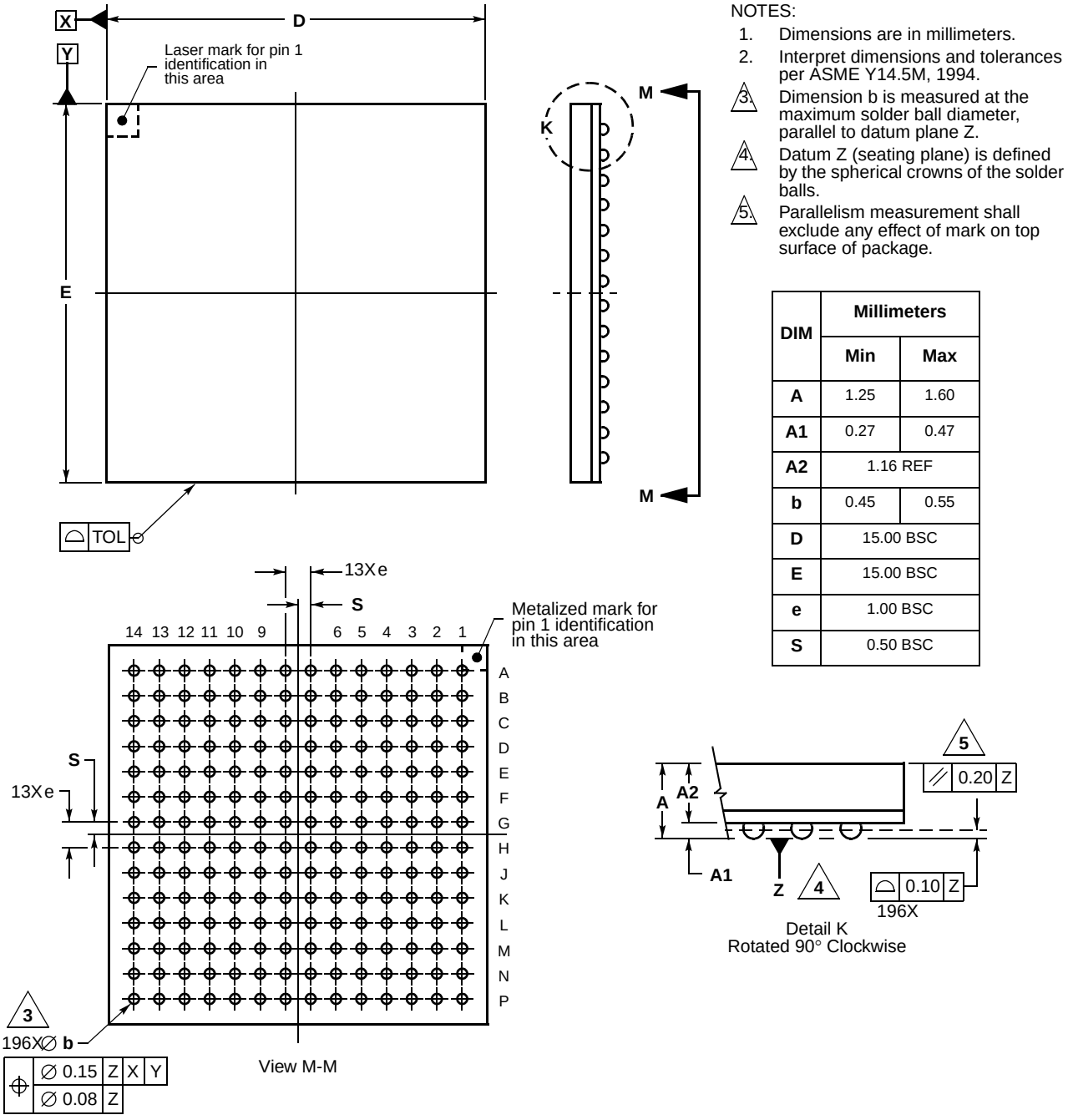
Table 5. Seven-Wire Mode Configuration

Signal Description	MCF523*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[0]
Collision	ECOL
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[0]
Unused, configure as PB14	ERXER
Unused input, tie to ground	ECRS
Unused, configure as PB[13:11]	ERXD[3:1]
Unused output, ignore	ETXER
Unused, configure as PB[10:8]	ETXD[3:1]
Unused, configure as PB15	EMDC
Input after reset, connect to ground	EMDIO

Refer to the M523*x*EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5235 site by navigating to: http://www.freescale.com/coldfire.

6.2 Package Dimensions—196 MAPBGA

Figure 3 shows MCF5232CVMxxx package dimensions.



NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

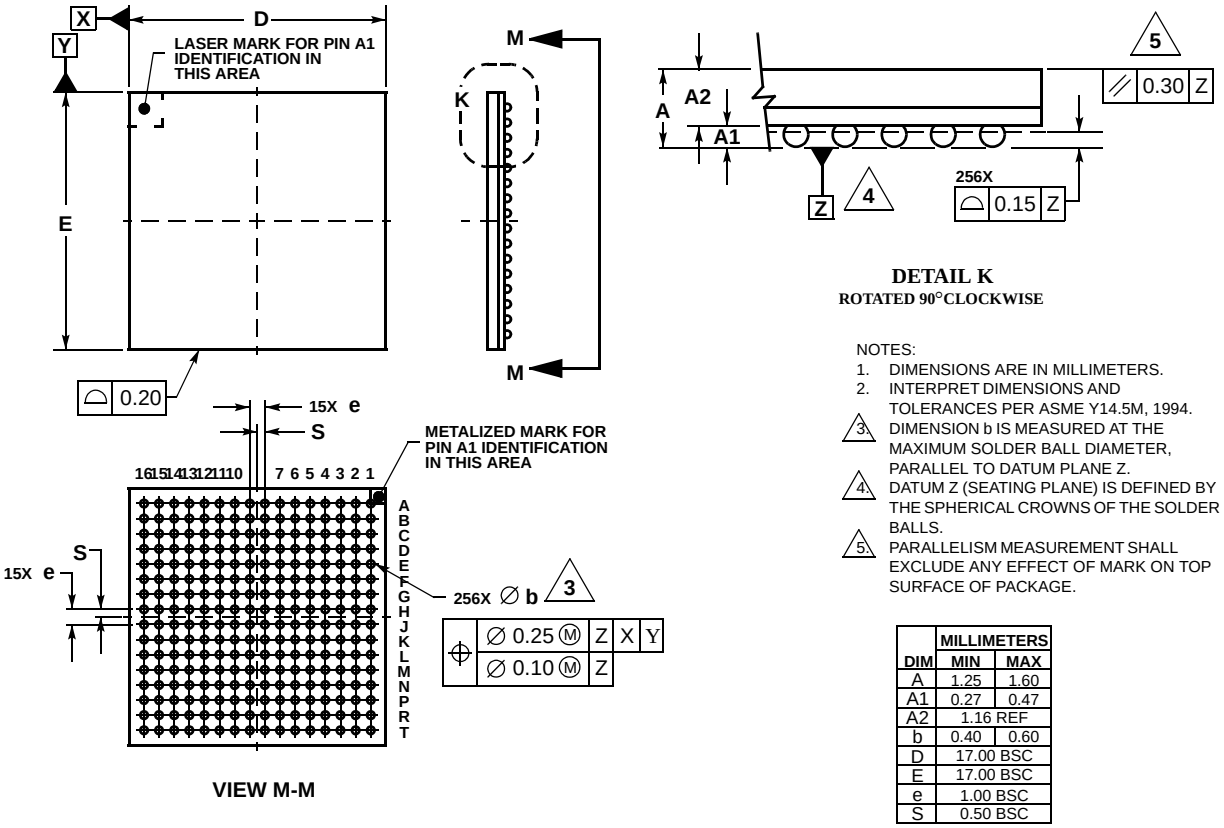
Figure 3. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	TPUCH17/ ETXD1	TPUCH1	TPUCH0	VDD	$\overline{BS1}$	$\overline{BS0}$	U1RXD/ CAN0RX	U1TXD/ CAN0TX	$\overline{CS6}$	$\overline{CS4}$	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	TPUCH18/ ETXD2	TPUCH19/ ETXD3	TPUCH16/ ETXD0	QSPI_ CLK	$\overline{BS2}$	QSPI_ CS1	$\overline{U1RTS}$	$\overline{CS3}$	$\overline{CS1}$	A23	A20	A19	B
C	TPUCH10	TPUCH9	TPUCH25/ ERXD1	TPUCH24/ ERXD0	TPUCH22/ ETXCLK	TPUCH20/ ETXER	I2C_SDA/ U2RXD/ EMDIO	QSPI_ DIN	$\overline{BS3}$	SD_CKE	$\overline{U1CTS}$	$\overline{CS7}$	$\overline{CS5}$	A22	A18	A17	C
D	TPUCH12	TPUCH11	TPUCH27/ ERXD3	TPUCH26/ ERXD2	TPUCH23/ ERXER	TPUCH21/ ETXEN	I2C_SCL/ U2TXD/ EMDC	QSPI_ DOUT	QSPI_ CS0	U2RXD/ CAN1RX	U2TXD/ CAN1TX	$\overline{CS2}$	$\overline{CS0}$	A14	A15	A16	D
E	TPUCH14	TPUCH13	TPUCH29/ ERXCLK	TPUCH2/ ERXDV	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	TPUCH31/ ECOL	TPUCH30/ ECRS	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	$\overline{U0CTS}$	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	$\overline{U0RTS}$	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{TEA}$	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	$\overline{SD\_WE}$	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/$\overline{W}$	L
M	D21	D22	D23	eTPU/ $\overline{EthENB}$	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	$\overline{SD\_CS0}$	$\overline{SD\_SRAS}$	$\overline{SD\_SCAS}$	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	$\overline{IRQ5}$	$\overline{IRQ1}$	$\overline{TRST}$/ DSCLK	PST0	JTAG_ EN	DDATA3	$\overline{SD\_CS1}$	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	$\overline{IRQ4}$	DT2IN	TMS/ $\overline{BKPT}$	PST1	$\overline{RCON}$	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	$\overline{IRQ7}$	$\overline{IRQ3}$	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	$\overline{OE}$	$\overline{IRQ6}$	$\overline{IRQ2}$	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	$\overline{RSTOUT}$	$\overline{RESET}$	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 6. MCF5235CVMxxx Pinout (256 MAPBGA)

6.2.2 Package Dimensions—256 MAPBGA

Figure 7 shows MCF5235CVMxxx, MCF5234CVMxxx, and MCF5233CVMxx package dimensions.



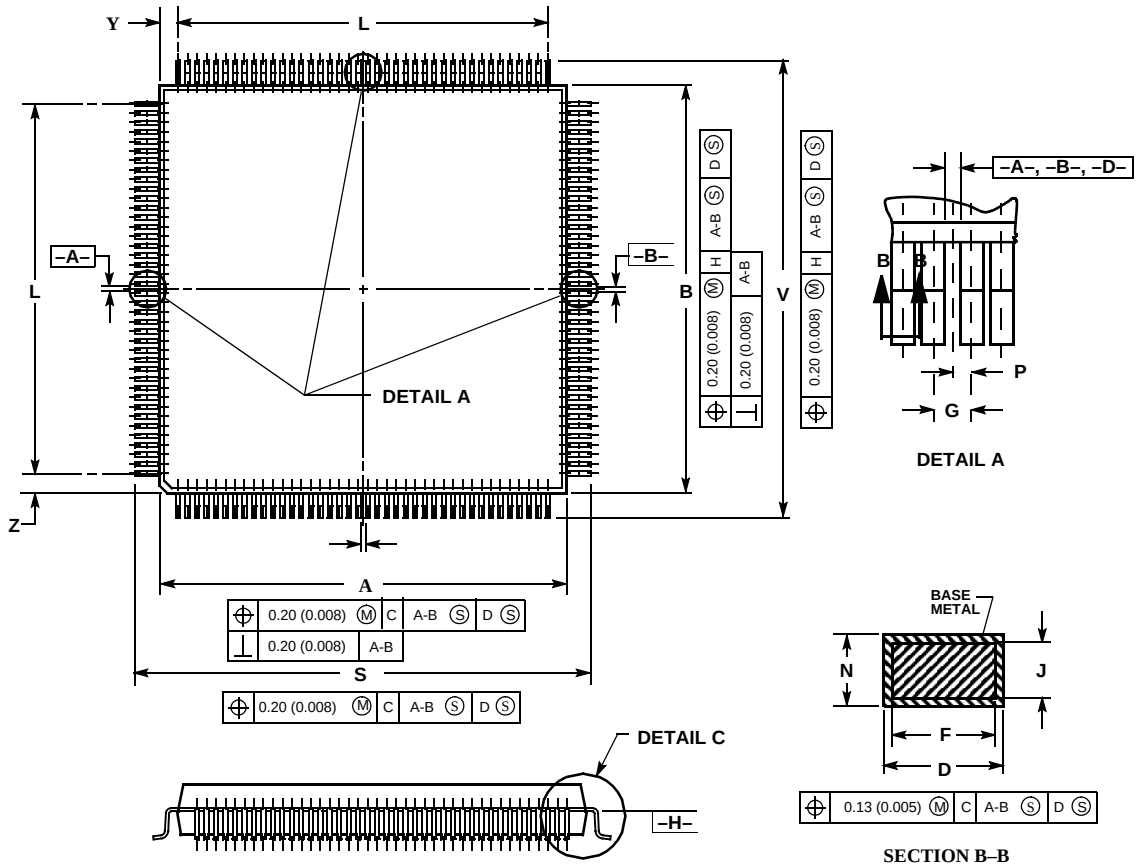
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

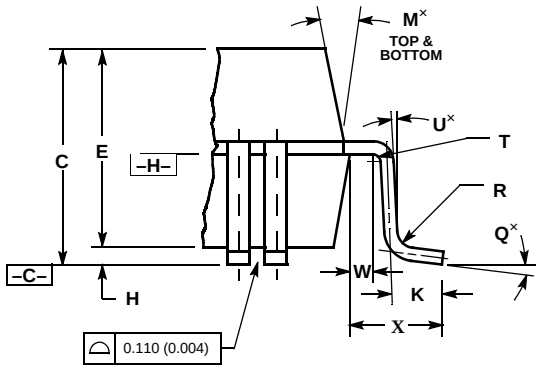
	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 7. 256 MAPBGA Package Outline

6.4 Package Dimensions—160 QFP

Figure 9 shows MCF5232CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 9. 160 QFP Package Dimensions

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5232CAB80	MCF5232 RISC Microprocessor	160 QFP	80MHz	Yes	–40° to +85° C
MCF5232CVM100	MCF5232 RISC Microprocessor	196 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5232CVM150	MCF5232 RISC Microprocessor	196 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5233CVM100	MCF5233 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5233CVM150	MCF5233 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5234CVM100	MCF5234 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5234CVM150	MCF5234 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVM100	MCF5235 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5235CVM150	MCF5235 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVF150	MCF5235 RISC Microprocessor,	256 MAPBGA	150MHz	No	–40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5235 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5235.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D= P_{INT} + $P_{I/O}$

P_{INT}= $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3 DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	—	1.0	μA
High Impedance (Off-State) Leakage Current $V_{in} = V_{DD}$ or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	—	1.0	μA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	–10	—	– 130	μA

7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.

9 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$.

10 PLL is operating in 1:1 PLL mode.

11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

13 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.

14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.

15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..

2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.

3 Refer to figure A-19.

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Figure 12 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

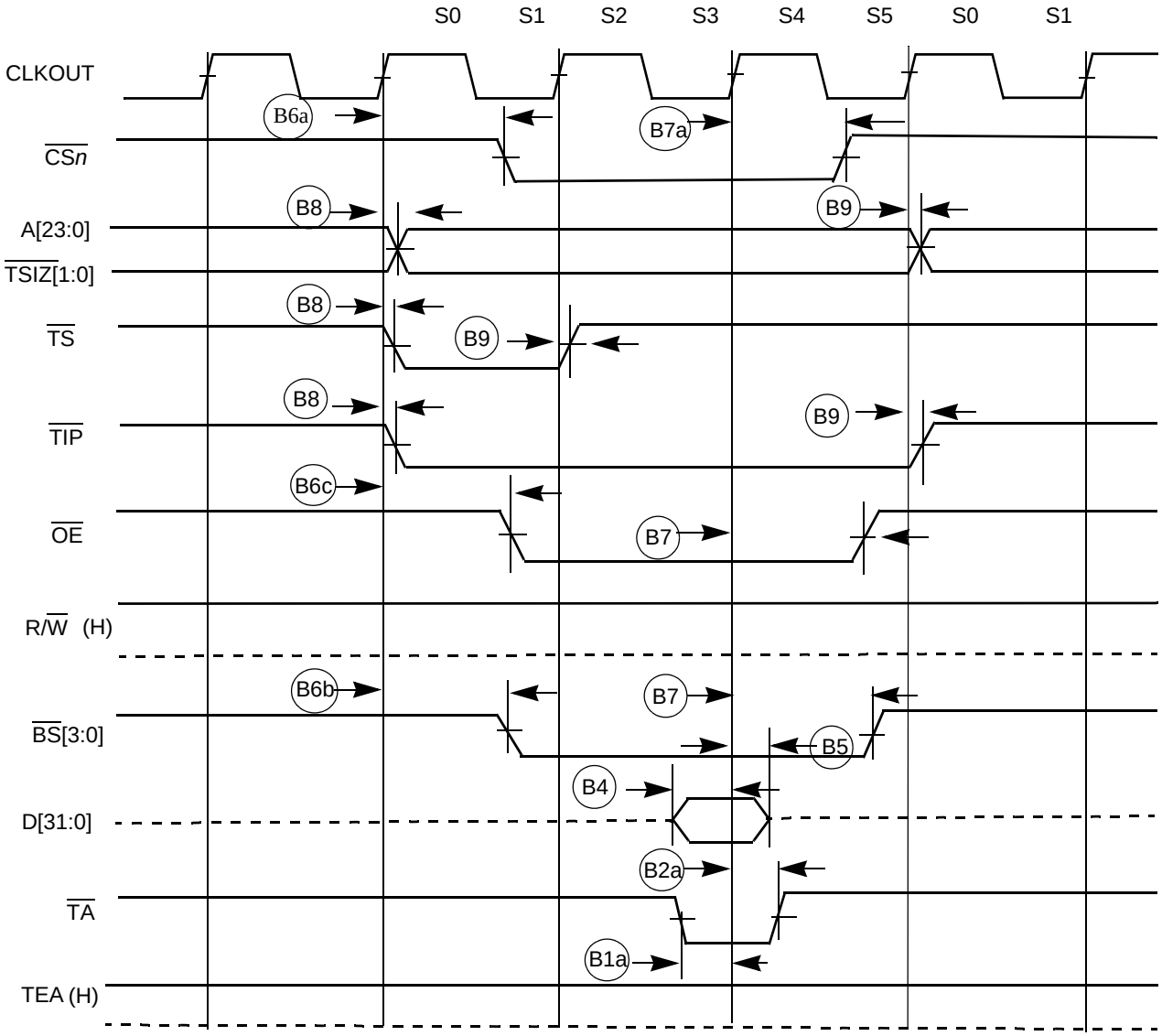


Figure 12. SRAM Read Bus Cycle Terminated by $\overline{TA}$

Figure 13 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

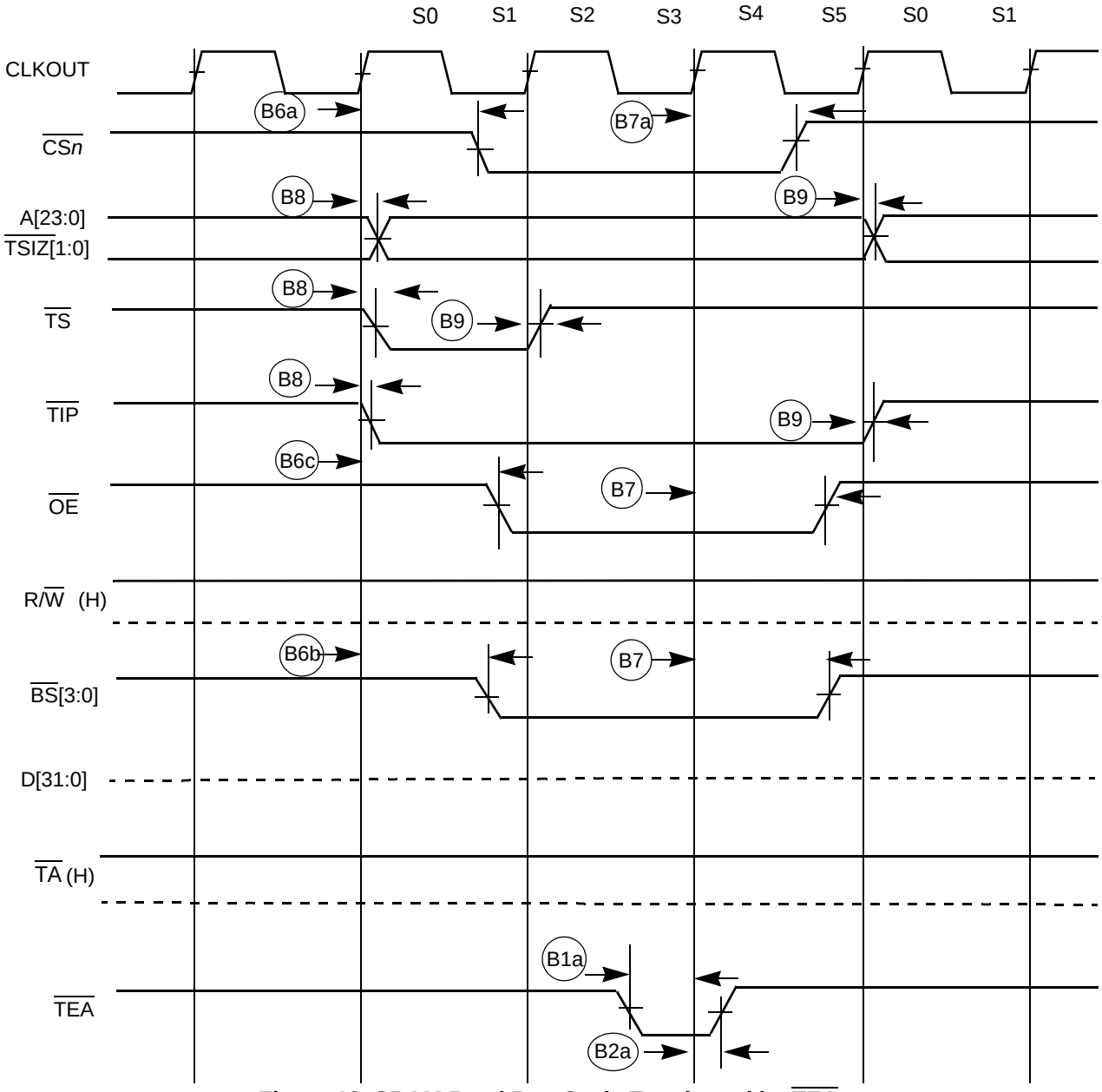
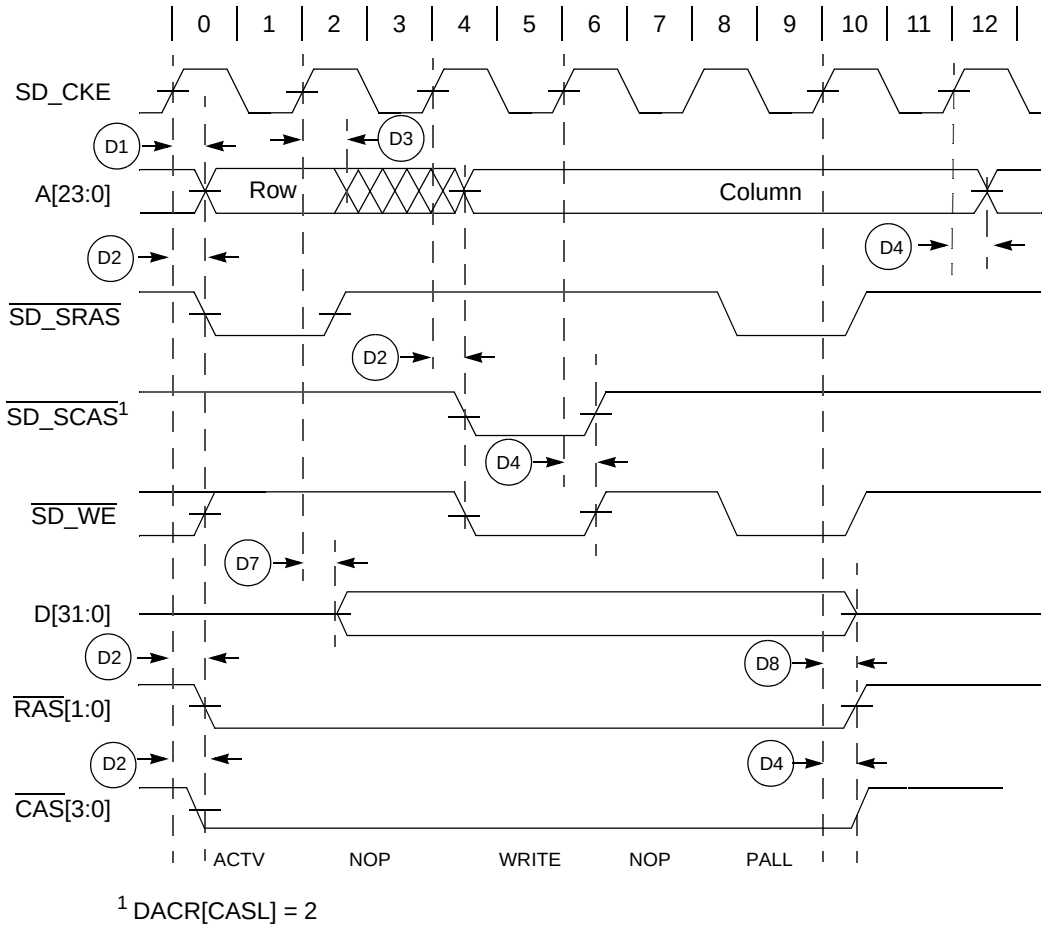


Figure 13. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

Figure 15 shows an SDRAM write cycle.



[1] DACR[CASL] = 2

Figure 15. SDRAM Write Cycle

7.7 General Purpose I/O Timing

Table 14. GPIO Timing[1]

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

[1] GPIO pins include: INT, ETPU, UART, FlexCAN, Timer, $\overline{\text{DREQ}n}$ and $\overline{\text{DACK}n}$ pins.

7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	ETXCLK to ETXD[3:0], ETXEN, ETXER invalid	5	—	ns
M6	ETXCLK to ETXD[3:0], ETXEN, ETXER valid	—	25	ns
M7	ETXCLK pulse width high	35%	65%	ETXCLK period
M8	ETXCLK pulse width low	35%	65%	ETXCLK period

Figure 20 shows MII transmit signal timings listed in Table 19.

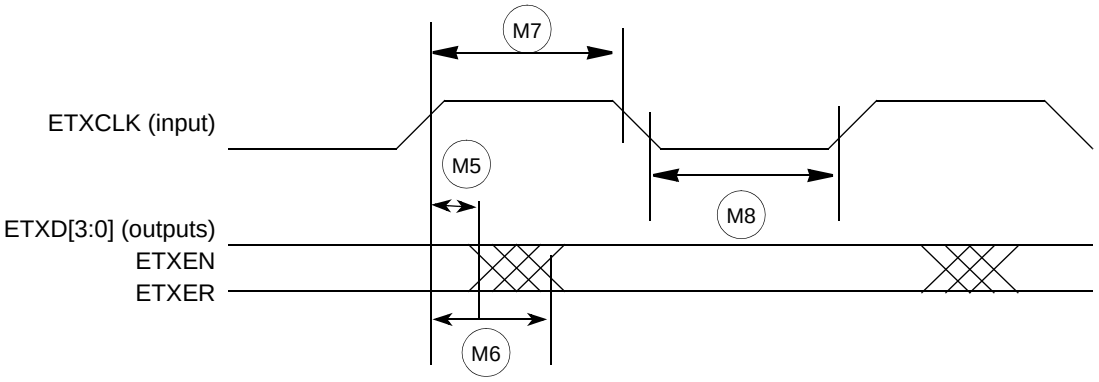


Figure 20. MII Transmit Signal Timing Diagram

7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	ECRS, ECOL minimum pulse width	1.5	—	ETXCLK period

Figure 21 shows MII asynchronous input timings listed in Table 20.

Figure 21. MII Async Inputs Timing Diagram

7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 25.

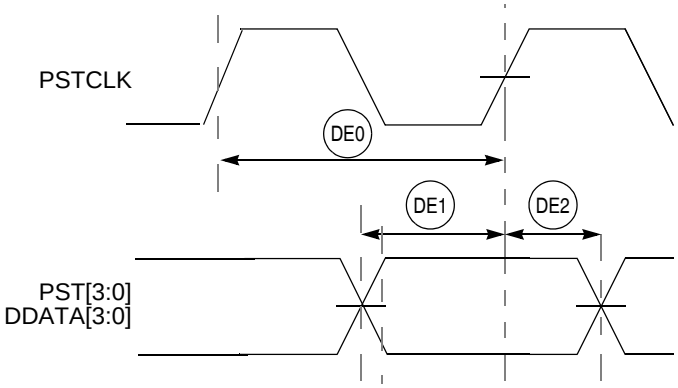


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 25.

Table 26. MCF5235EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.5	• Removed Overview, Features, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5235 Reference Manual. • Removed list of documentation table in Section 8, "Documentation.". An up-to-date list is always available on our web site.
1.6	• Table 9: Changed core supply voltage (V_{DD}) from 1.35-1.65 to 1.4-1.6.
1.7	• Table 10: Changed max f_{ICO} frequency from "75 MHz" to "150 MHz".
1.8	• Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." • Updated 196MAPBGA package dimensions, Figure 3.
2	• Table 2: Changed SD_CKE pin location from 139 to "—" for the 160QFP device. Changed QSPI_CS1 pin location from "—" to 139 for the 160QFP device. • Figure 8: Changed pin 139 label from "SD_CKE/QSPI_CS1" to "QSPI_CS1/SD_CKE". • Removed second sentence from Section 7.10.1, "MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)," and Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," as this feature is not supported on this device.
3	• Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, "Power Up Sequence" first bullet, changed "Use 1 µs" to "Use 1 ms". • Corrected position of spec D5 in Figure 14. • Table 14: Added $\overline{DACKn}$ and $\overline{DREQn}$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5235CVF150 in Table 6