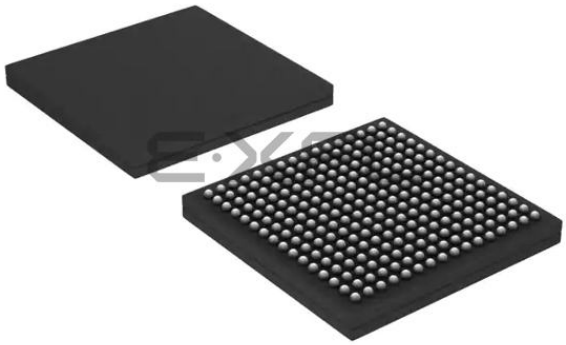

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	113
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5235cvf150

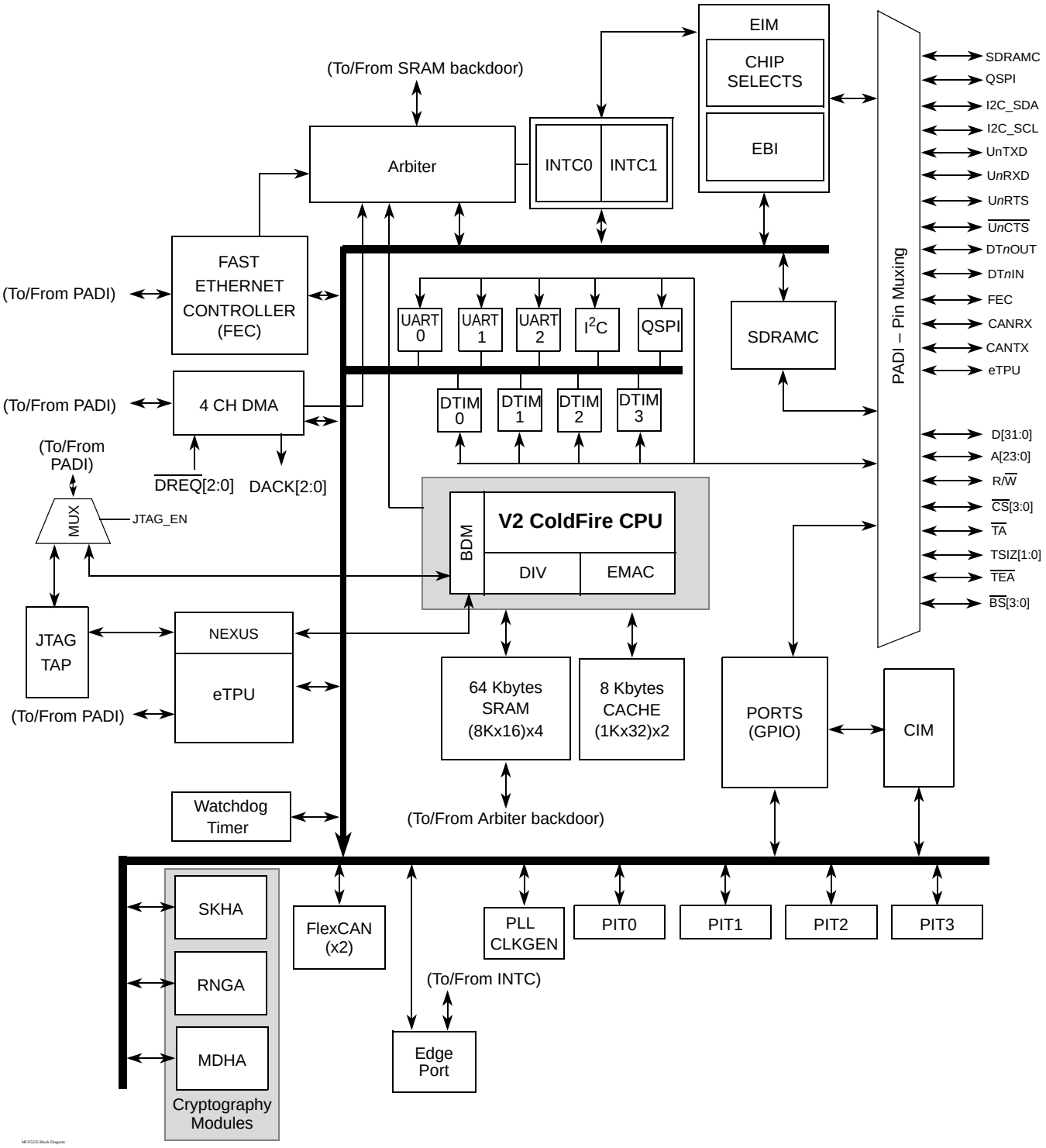
1 MCF523*x* Family Configurations

Table 1. MCF523*x* Family Configurations

Module	MCF5232	MCF5233	MCF5234	MCF5235
ColdFire V2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x	x
Enhanced Time Processor Unit with memory (eTPU)	16-ch 6K	32-ch 6K	16-ch 6K	32-ch 6K
System Clock	up to 150 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 144			
Instruction/Data Cache	8 Kbytes			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	x	x	x	x
External Interface Module (EIM)	x	x	x	x
4-channel Direct-Memory Access (DMA)	x	x	x	x
SDRAM Controller	x	x	x	x
Fast Ethernet Controller (FEC)	—	—	x	x
Cryptography - Security module for data packets processing	—	—	—	x
Watchdog Timer (WDT)	x	x	x	x
Four Periodic Interrupt Timers (PIT)	x	x	x	x
32-bit DMA Timers	4	4	4	4
QSPI	x	x	x	x
UART(s)	3	3	3	3
I^2C	x	x	x	x
FlexCAN 2.0B - Controller-Area Network communication module	1	2	1	2
General Purpose I/O Module (GPIO)	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x	x	x
Package	160 QFP 196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Block Diagram

The superset device in the MCF523*x* family comes in a 256 mold array process ball grid array (MAPBGA) package. Figure shows a top-level block diagram of the MCF5235, the superset device.



3 Features

For a detailed feature list see the MCF5235 Reference Manual (MCF5235RM).

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
A[20:0]	—	—	—	O	123:115, 112:106, 102:98	A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13	B15, B16, C15, C16, D16, D15, D14, E16, E15, E14, E13, F15, F14, F13, G15, G14, G13, H16, H15, H14, H13	B15, B16, C15, C16, D16, D15, D14, E16, E15, E14, E13, F15, F14, F13, G15, G14, G13, H16, H15, H14, H13	B15, B16, C15, C16, D16, D15, D14, E16, E15, E14, E13, F15, F14, F13, G15, G14, G13, H16, H15, H14, H13
D[31:16]	—	—	—	O	21:24, 26:30, 33:39	G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2	K4, K3, K2, K1, L4, L3, L2, L1, M3, M2, M1, N2, N1, P2, P1, R1	K4, K3, K2, K1, L4, L3, L2, L1, M3, M2, M1, N2, N1, P2, P1, R1	K4, K3, K2, K1, L4, L3, L2, L1, M3, M2, M1, N2, N1, P2, P1, R1
D[15:8]	PDATAH[7:0]	—	—	O	42:49,	M1, N1, M2, N2, P2, L3, M3, N3,	R2, T2, N3, P3, R3, T3, N4, P4,	R2, T2, N3, P3, R3, T3, N4, P4,	R2, T2, N3, P3, R3, T3, N4, P4,
D[7:0]	PDATAL[7:0]	—	—	O	50:52, 56:60	P3, M4, N4, P4, L5, M5, N5, P5	R4, T4, P5, R5, N6, P6, R6, N7	R4, T4, P5, R5, N6, P6, R6, N7	R4, T4, P5, R5, N6, P6, R6, N7
$\overline{BS}$[3:0]	PBS[7:4]	$\overline{CAS}$[3:0]	—	O	143:140	B6, C6, D7, C7	C9, B9, A9, A10	C9, B9, A9, A10	C9, B9, A9, A10
$\overline{OE}$	PBUSCTL7	—	—	O	63	N6	T7	T7	T7
$\overline{TA}$	PBUSCTL6	—	—	I	97	H11	K14	K14	K14
$\overline{TEA}$	PBUSCTL5	$\overline{DREQ1}$	—	I	—	J14	K13	K13	K13
R/$\overline{W}$	PBUSCTL4	—	—	O	96	J13	L16	L16	L16
$\overline{TSIZ1}$	PBUSCTL3	DACK1	—	O	—	P6	N8	N8	N8
$\overline{TSIZ0}$	PBUSCTL2	DACK0	—	O	—	P7	P8	P8	P8
$\overline{TS}$	PBUSCTL1	DACK2	—	O	—	H13	K16	K16	K16
$\overline{TIP}$	PBUSCTL0	$\overline{DREQ0}$	—	O	—	H12	K15	K15	K15
Chip Selects									
$\overline{CS}$[7:4]	PCS[7:4]	—	—	O	—	B9, A10, C10, A11	C12, A13, C13, A14	C12, A13, C13, A14	C12, A13, C13, A14
$\overline{CS}$[3:2]	PCS[3:2]	SD_CS[1:0]	—	O	134,133	A9, C9	B12, D12	B12, D12	B12, D12
$\overline{CS1}$	PCS1	—	—	O	130	B10	B13	B13	B13
$\overline{CS0}$	—	—	—	O	129	D10	D13	D13	D13
SDRAM Controller									

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
$\overline{\text{SD\_WE}}$	PSDRAM5	—	—	O	93	K13	L13	L13	L13
$\overline{\text{SD\_SCAS}}$	PSDRAM4	—	—	O	92	K12	M15	M15	M15
$\overline{\text{SD\_SRAS}}$	PSDRAM3	—	—	O	91	K11	M14	M14	M14
$\overline{\text{SD\_CKE}}$	PSDRAM2	—	—	O	—	E8	C10	C10	C10
$\overline{\text{SD\_CS}}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13	N15, M13	N15, M13	N15, M13
External Interrupts Port									
$\overline{\text{IRQ}}$[7:3]	PIRQ[7:3]	—	—	I	IRQ7=64 IRQ4=65	N7, M7, L7, P8, N8	R8, T8, N9, P9, R9	R8, T8, N9, P9, R9	R8, T8, N9, P9, R9
$\overline{\text{IRQ2}}$	PIRQ2	$\overline{\text{DREQ2}}$	—	I	—	M8	T9	T9	T9
$\overline{\text{IRQ1}}$	PIRQ1	—	—	I	66	L8	N10	N10	N10
eTPU									
TPUCH31	—	ECOL	—		—	—	F3	—	F3
TPUCH30	—	ECRS	—		—	—	F4	—	F4
TPUCH29	—	ERXCLK	—		—	—	E3	—	E3
TPUCH28	—	ERXDV	—		—	—	E4	—	E4
TPUCH[27:24]	—	ERXD[3:0]	—		—	—	D3, D4, C3, C4	—	D3, D4, C3, C4
TPUCH23	—	ERXER	—		—	—	D5	—	D5
TPUCH22	—	ETXCLK	—		—	—	C5	—	C5
TPUCH21	—	ETXEN	—		—	—	D6	—	D6
TPUCH20	—	ETXER	—		—	—	C6	—	C6
TPUCH[19:16]	—	ETXD[3:0]	—		—	—	B6,B5, A5, B7	—	B6,B5, A5, B7
TPUCH[15:0]	—	—	—		11, 10, 7:2, 159:154, 152, 151	E2, E1, D1 D2, D3, C1, C2, B1, B2, A2, C3, B3, A3, A4, C4, BR	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7	F2, E1, E2, D1, D2, C1, C2, B1, B2, A2, B3, A3, B4, A4, A6, A7
TCRCLK	PETPU2	—	—		12	E3	F1	F1	F1
UTPUODIS	PETPU1	—	—		—	H10	J13	J13	J13
LTPUODIS	PETPU0	—	—		—	G10	J14	J14	J14
FEC									
EMDIO	PFECI2C2	I2C_SDA	U2RXD	I/O	—	—	—	C7	C7
EMDC	PFECI2C3	I2C_SCL	U2TXD	O	—	—	—	D7	D7
ECOL	—	—	—	I	—	—	—	F3	F3

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
ECRS	—	—	—	I	—	—	—	F4	F4
ERXCLK	—	—	—	I	—	—	—	E3	E3
ERXDV	—	—	—	I	—	—	—	E4	E4
ERXD[3:0]	—	—	—	I	—	—	—	D3, D4, C3, C4	D3, D4, C3, C4
ERXER	—	—	—	I	—	—	—	D5	D5
ETXCLK	—	—	—	I	—	—	—	C5	C5
ETXEN	—	—	—	O	—	—	—	D6	D6
ETXER	—	—	—	O	—	—	—	C6	C6
ETXD[3:0]	—	—	—	O	—	—	—	B6, B5, A5, B7	B6, B5, A5, B7
Feature Control									
eTPU/$\overline{\text{EthENB}}$	—	—	—	I	—	—	—	—	M4
I^2C									
I2C_SDA	PFECI2C1	CAN0RX	—	I/O	—	J12	L15	L15	L15
I2C_SCL	PFECI2C0	CAN0TX	—	I/O	—	J11	L14	L14	L14
DMA									
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, TSIZ1and DT1OUT for $\overline{\text{DACK1}}$, TSIZ0 and DT0OUT for $\overline{\text{DACK0}}$, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and DT1IN for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—	—	—	—
QSPI									
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7	B10	B10	B10
QSPI_CS0	PQSPI3	—	—	O	147	A6	D9	D9	D9
QSPI_CLK	PQSPI2	I2C_SCL	—	O	148	C5	B8	B8	B8
QSPI_DIN	PQSPI1	I2C_SDA	—	I	149	B5	C8	C8	C8
QSPI_DOUT	PQSPI0	—	—	O	150	A5	D8	D8	D8
UARTs									
U2TXD	PUARTH1	CAN1TX	—	O	—	A8	D11	D11	D11
U2RXD	PUARTH0	CAN1RX	—	I	—	A7	D10	D10	D10
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	—	B8	C11	C11	C11
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	—	C8	B11	B11	B11
U1TXD	PUARTL5	CAN0TX	—	O	135	D9	A12	A12	A12

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/V_{DDPLL} supplies.

5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 μF and 0.01 μF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, “Electrical Characteristics.”

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{DRAMW}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF523*x*. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:0]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5235 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

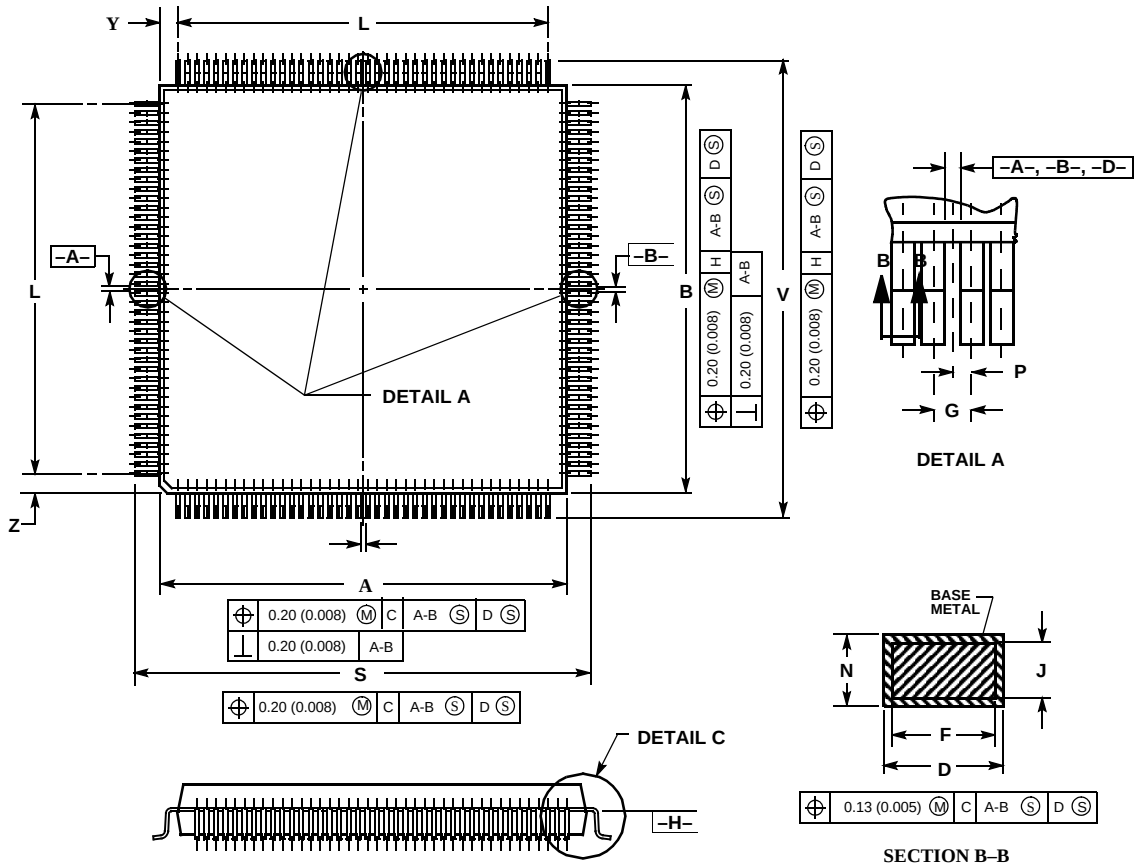
The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

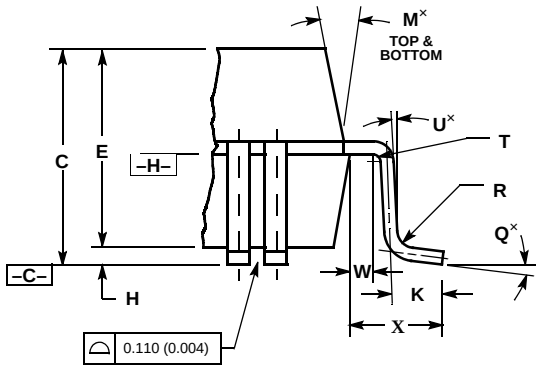
Table 4. MII Mode

Signal Description	MCF523*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]

6.4 Package Dimensions—160 QFP

Figure 9 shows MCF5232CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 9. 160 QFP Package Dimensions

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5232CAB80	MCF5232 RISC Microprocessor	160 QFP	80MHz	Yes	–40° to +85° C
MCF5232CVM100	MCF5232 RISC Microprocessor	196 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5232CVM150	MCF5232 RISC Microprocessor	196 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5233CVM100	MCF5233 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5233CVM150	MCF5233 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5234CVM100	MCF5234 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5234CVM150	MCF5234 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVM100	MCF5235 RISC Microprocessor	256 MAPBGA	100MHz	Yes	–40° to +85° C
MCF5235CVM150	MCF5235 RISC Microprocessor	256 MAPBGA	150MHz	Yes	–40° to +85° C
MCF5235CVF150	MCF5235 RISC Microprocessor,	256 MAPBGA	150MHz	No	–40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5235 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5235.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

Table 9. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	—	 7 7	pF
Load Capacitance[4] Low drive strength High drive strength	C_L		 — —	 25 50	 pF pF
Core Operating Supply Current [5] Master Mode	I_{DD}	 —	 135	 150	 mA
Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 100 TBD	 — —	 mA μA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total processor Limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10		 1.0 10	 mA mA

1 Refer to Table 10 for additional PLL specifications.

2 Refer to the MCF5235 signals section for pins having weak internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.

5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

6 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.

9 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$.

10 PLL is operating in 1:1 PLL mode.

11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

13 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.

14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.

15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..

2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.

3 Refer to figure A-19.

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 12 are shown in Figure 11, Figure 12, and Figure 13.

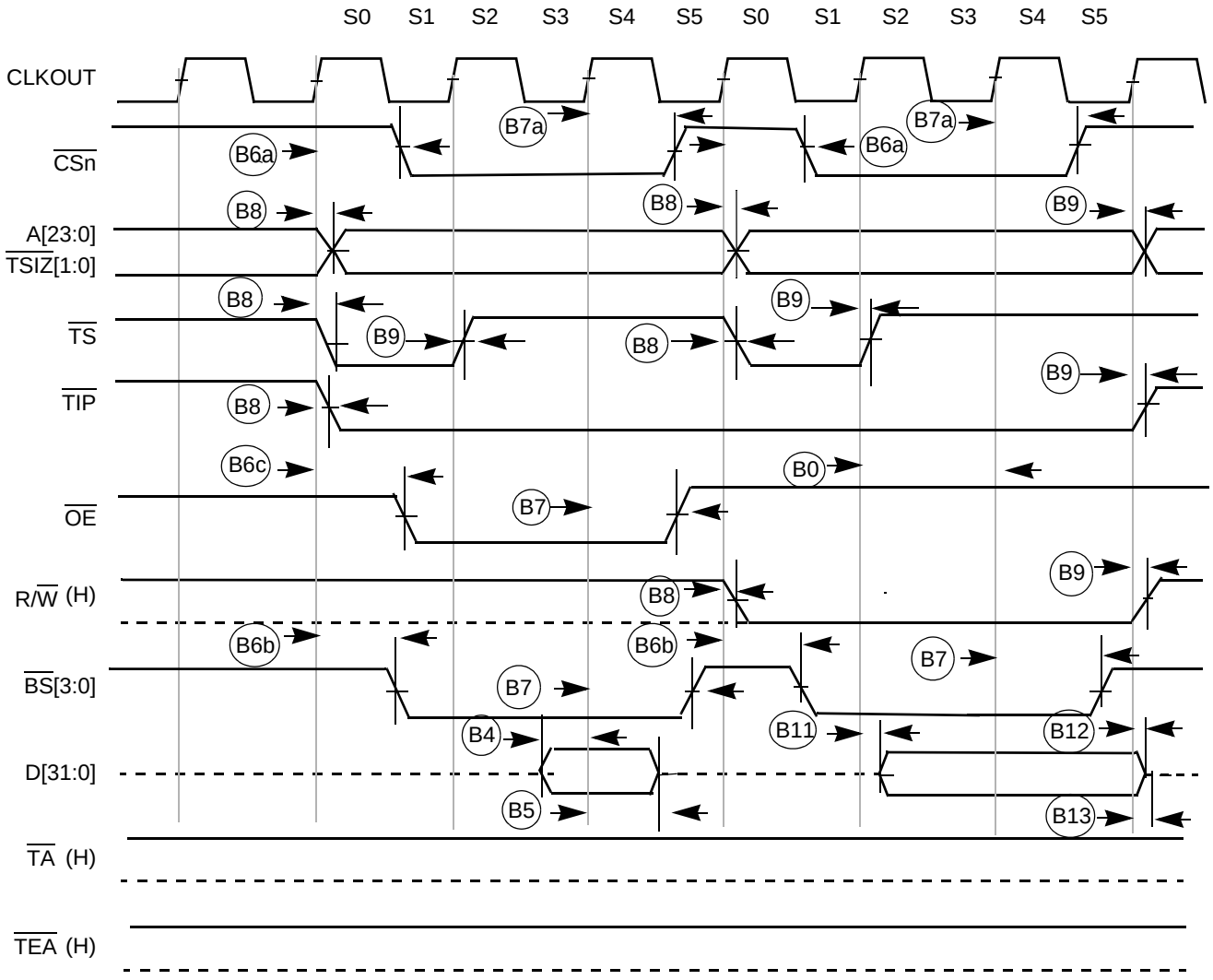
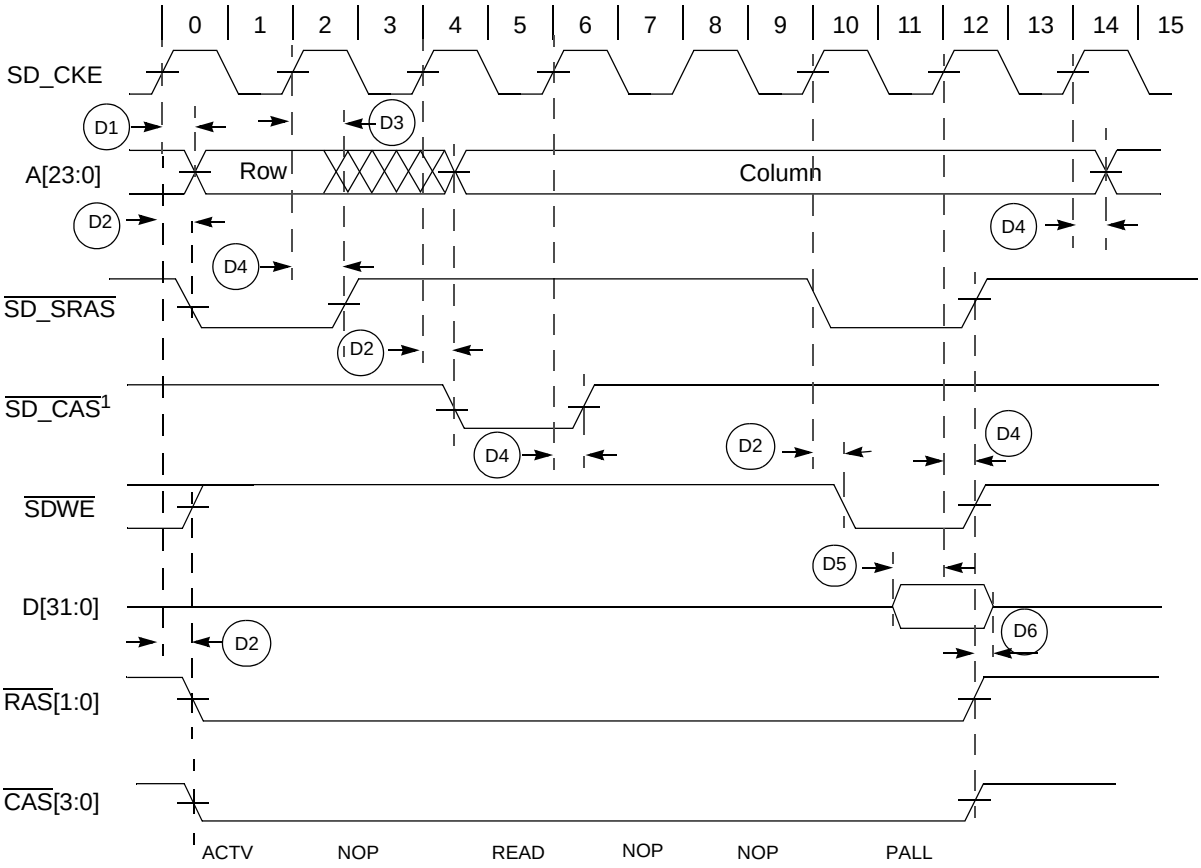


Figure 11. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 14 shows an SDRAM read cycle.



1 DACR[CASL] = 2

Figure 14. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

1 D7 and D8 are for write cycles only.

7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	ETXCLK to ETXD[3:0], ETXEN, ETXER invalid	5	—	ns
M6	ETXCLK to ETXD[3:0], ETXEN, ETXER valid	—	25	ns
M7	ETXCLK pulse width high	35%	65%	ETXCLK period
M8	ETXCLK pulse width low	35%	65%	ETXCLK period

Figure 20 shows MII transmit signal timings listed in Table 19.

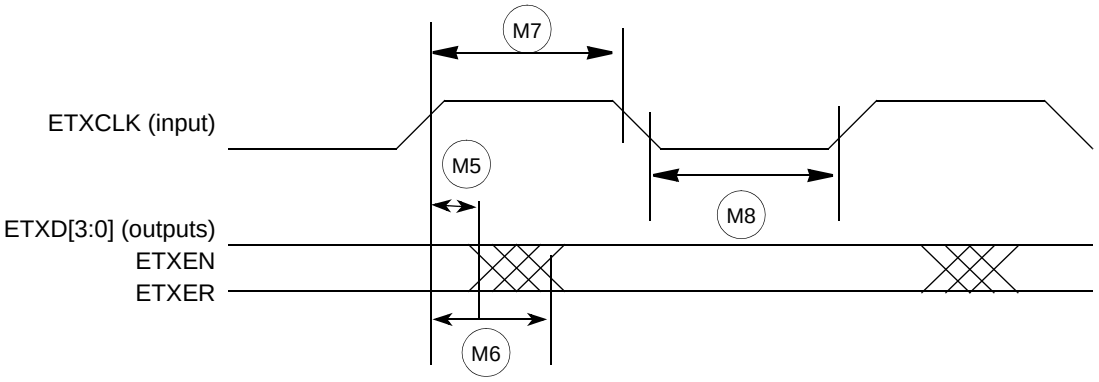


Figure 20. MII Transmit Signal Timing Diagram

7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	ECRS, ECOL minimum pulse width	1.5	—	ETXCLK period

Figure 21 shows MII asynchronous input timings listed in Table 20.

Figure 21. MII Async Inputs Timing Diagram

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

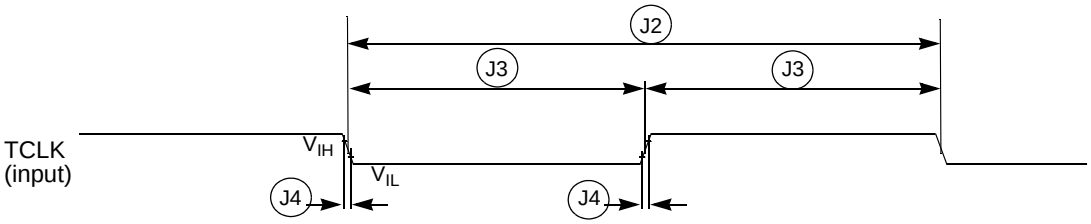


Figure 24. Test Clock Input Timing

7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 25.

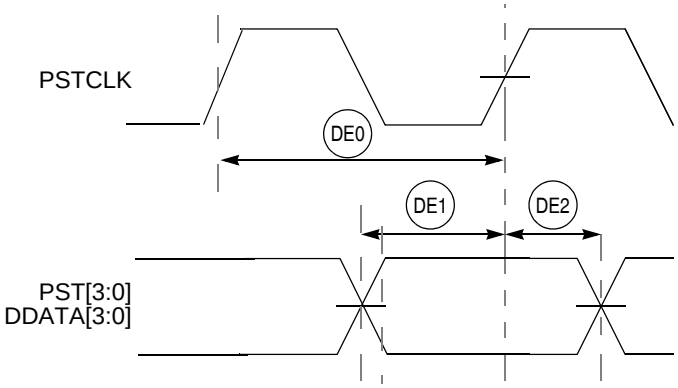


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 25.

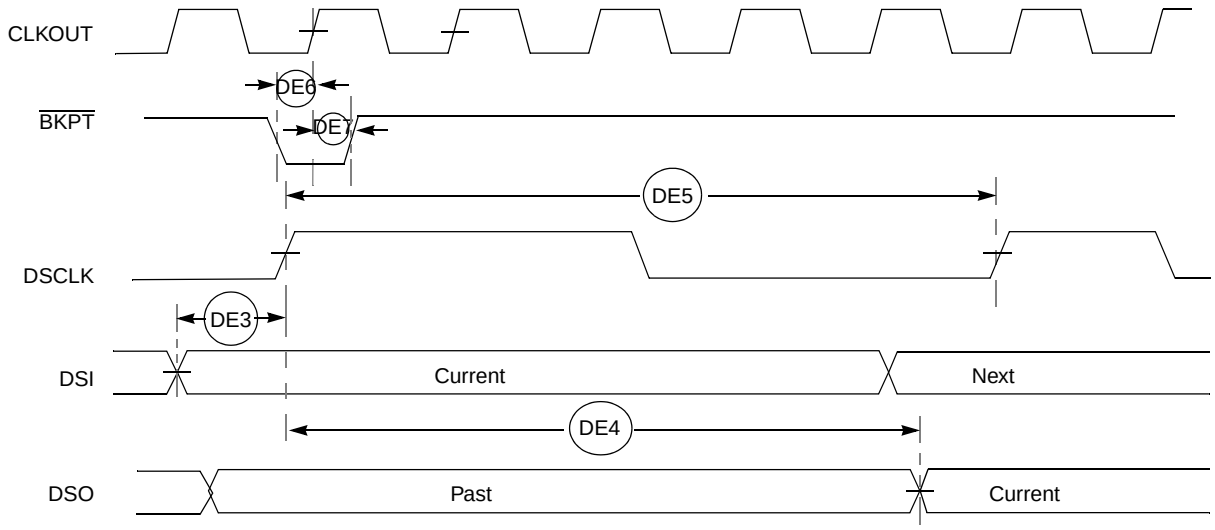


Figure 29. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF523*x* and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5235EC Revision History

Rev. No.	Substantive Change(s)
0	Preliminary release.
1	• Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Corrected Figure 8 pin 81. VDD instead of VSS • Changed instances of Motorola to Freescale
1.3	• Removed detailed signal description section. This information can be found in the MCF5235RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5235RM Chapter 1. • Corrected Figure 2 pin F10. VSS instead of VDD. Change made in Table 2 as well. • Corrected Figure 8 pin 81. OVDD instead of VDD. Change made in Table 2 as well. • Cleaned up many inconsistencies within the pinout figure signal names • Corrected document IDs in Documentation Table
1.4	• Added values for ‘Maximum operating junction temperature’ in Table 8. • Added typical values for ‘Core operating supply current (master mode)’ in Table 9. • Added typical values for ‘Pad operating supply current (master mode)’ in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.

Table 26. MCF5235EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.5	• Removed Overview, Features, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5235 Reference Manual. • Removed list of documentation table in Section 8, "Documentation.". An up-to-date list is always available on our web site.
1.6	• Table 9: Changed core supply voltage (V_{DD}) from 1.35-1.65 to 1.4-1.6.
1.7	• Table 10: Changed max f_{ICO} frequency from "75 MHz" to "150 MHz".
1.8	• Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." • Updated 196MAPBGA package dimensions, Figure 3.
2	• Table 2: Changed SD_CKE pin location from 139 to "—" for the 160QFP device. Changed QSPI_CS1 pin location from "—" to 139 for the 160QFP device. • Figure 8: Changed pin 139 label from "SD_CKE/QSPI_CS1" to "QSPI_CS1/SD_CKE". • Removed second sentence from Section 7.10.1, "MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)," and Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," as this feature is not supported on this device.
3	• Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, "Power Up Sequence" first bullet, changed "Use 1 µs" to "Use 1 ms". • Corrected position of spec D5 in Figure 14. • Table 14: Added $\overline{DACKn}$ and $\overline{DREQn}$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5235CVF150 in Table 6