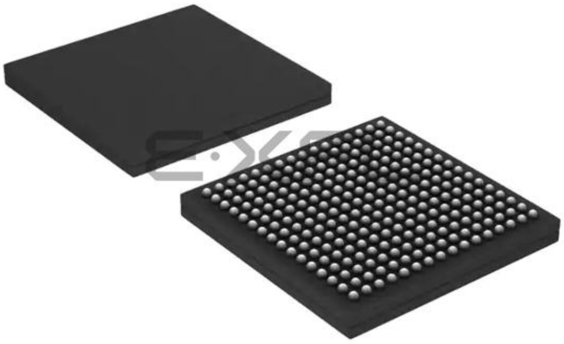
Freescale Semiconductor - MCF5235CVM100J Datasheet



Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	113
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5235cvm100j

1 MCF523*x* Family Configurations

Table 1. MCF523*x* Family Configurations

Module	MCF5232	MCF5233	MCF5234	MCF5235
ColdFire V2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x	x
Enhanced Time Processor Unit with memory (eTPU)	16-ch 6K	32-ch 6K	16-ch 6K	32-ch 6K
System Clock	up to 150 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 144			
Instruction/Data Cache	8 Kbytes			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	x	x	x	x
External Interface Module (EIM)	x	x	x	x
4-channel Direct-Memory Access (DMA)	x	x	x	x
SDRAM Controller	x	x	x	x
Fast Ethernet Controller (FEC)	—	—	x	x
Cryptography - Security module for data packets processing	—	—	—	x
Watchdog Timer (WDT)	x	x	x	x
Four Periodic Interrupt Timers (PIT)	x	x	x	x
32-bit DMA Timers	4	4	4	4
QSPI	x	x	x	x
UART(s)	3	3	3	3
I^2C	x	x	x	x
FlexCAN 2.0B - Controller-Area Network communication module	1	2	1	2
General Purpose I/O Module (GPIO)	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x	x	x
Package	160 QFP 196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Block Diagram

The superset device in the MCF523*x* family comes in a 256 mold array process ball grid array (MAPBGA) package. Figure shows a top-level block diagram of the MCF5235, the superset device.

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
U1RXD	PUARTL4	CAN0RX	—	I	136	D8	A11	A11	A11
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	—	F3	G1	G1	G1
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	—	G3	H3	H3	H3
U0TXD	PUARTL1	—	—	O	14	F1	H2	H2	H2
U0RXD	PUARTL0	—	—	I	13	F2	G2	G2	G2
DMA Timers									
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14	J15	J15	J15
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14	J16	J16	J16
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	—	M9	P10	P10	P10
DT2OUT	PTIMER4	DACK2	—	O	—	L9	R10	R10	R10
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	—	L6	P7	P7	P7
DT1OUT	PTIMER2	DACK1	—	O	—	M6	R7	R7	R7
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	—	E4	G4	G4	G4
DT0OUT	PTIMER0	DACK0	—	O	—	F4	G3	G3	G3
BDM/JTAG[2]									
DSCLK	—	TRST	—	I	70	N9	N11	N11	N11
PSTCLK	—	TCLK	—	O	68	P9	T10	T10	T10
$\overline{\text{BKPT}}$	—	TMS	—	I	71	P10	P11	P11	P11
DSI	—	TDI	—	I	73	M10	T11	T11	T11
DSO	—	TDO	—	O	72	N10	R11	R11	R11
JTAG_EN	—	—	—	I	78	K9	N13	N13	N13
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11	N14, P14, T13, R13	N14, P14, T13, R13	N14, P14, T13, R13
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10	T12, R12, P12, N12	T12, R12, P12, N12	T12, R12, P12, N12

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
Test									
TEST	—	—	—	I	18	F5	J4	J4	J4
PLL_TEST	—	—	—	I	—		R14	R14	R14
Power Supplies									
VDDPLL	—	—	—	I	87	M13	P15		
VSSPLL	—	—	—	I	84	L14	R15		
OVDD	—	—	—	I	1, 9, 17, 32, 41, 55, 62, 69, 81, 90, 95, 105, 114, 128, 132, 138, 146	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8	E6:11, F5, F7:10, F12, G5, G6, G11, G12, H5, H6, H11, H12, J5, J6, J11, J12, K5, K6, K11, K12, L5, L7:10, L12, M6:M11		
VSS	—	—	—	I	8, 16, 25, 31, 40, 54, 61, 67, 80, 88, 94, 104, 113, 127, 131, 137, 145, 153, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14	A1, A16, E5, E12, F6, F11, F16, G7:10, H7: 10, J1, J7:10, K7:10, L6, L11, M5, M12, N16, T1, T6, T16		
VDD	—	—	—	I	15, 53, 103, 144	D6, F11, G4, L4	A8, G16, H1, T5		

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF523*x*.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{DRAMW}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF523*x*. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:0]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5235 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF523*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]

5.7.3 FlexCAN

The FlexCAN module interface to the CAN bus is composed of 2 pins: CANTX and CANRX, which are the serial transmitted data and the serial received data. The use of an external CAN transceiver to interface to the CAN bus is generally required. The transceiver is capable of driving the large current needed for the CAN bus and has current protection, against a defective CAN bus or defective stations.

5.7.4 BDM

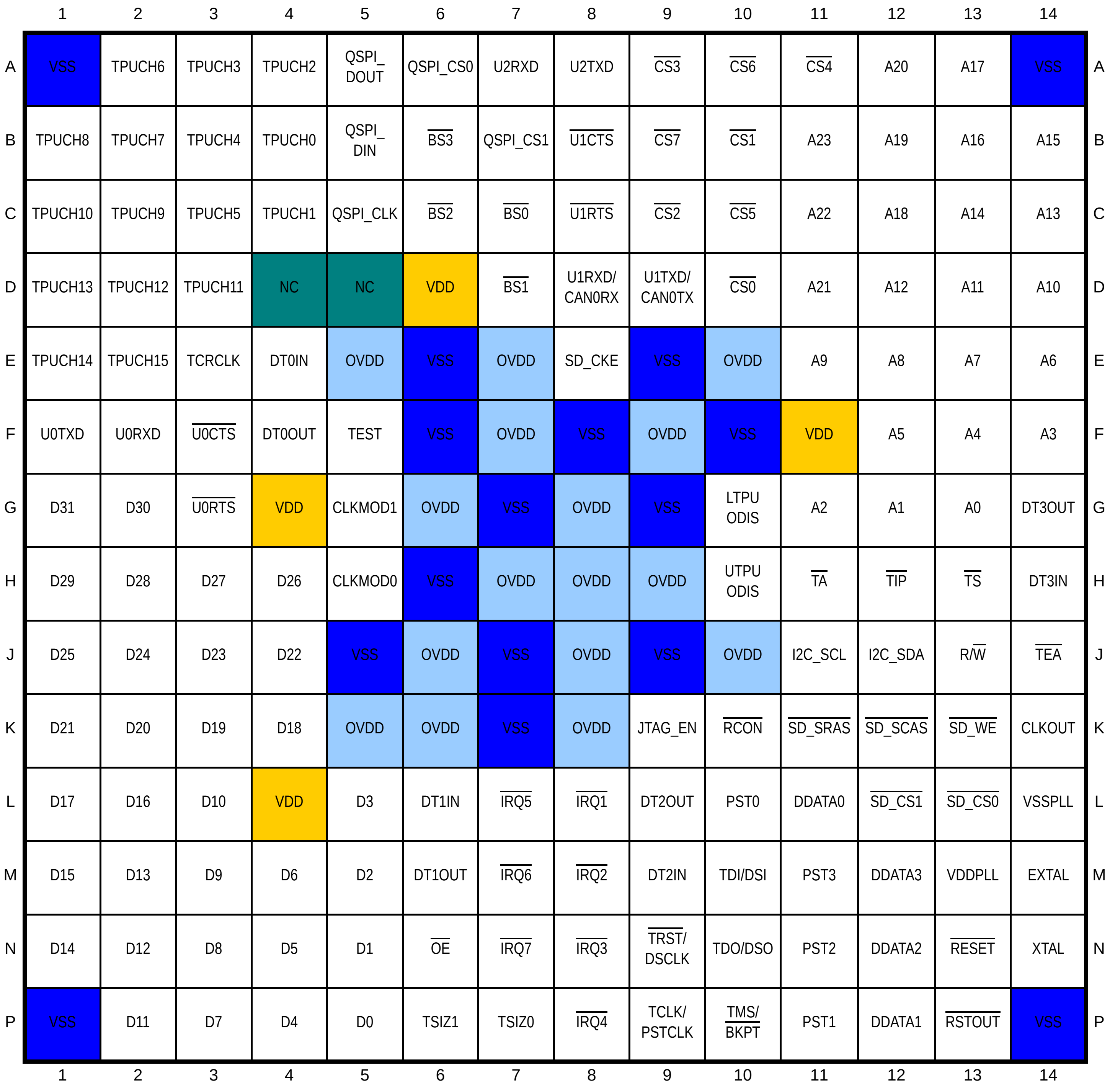
Use the BDM interface as shown in the M523*x*EVB evaluation board user’s manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF523*x* devices. See Table 2 for a list the signal names and pin locations for each device.

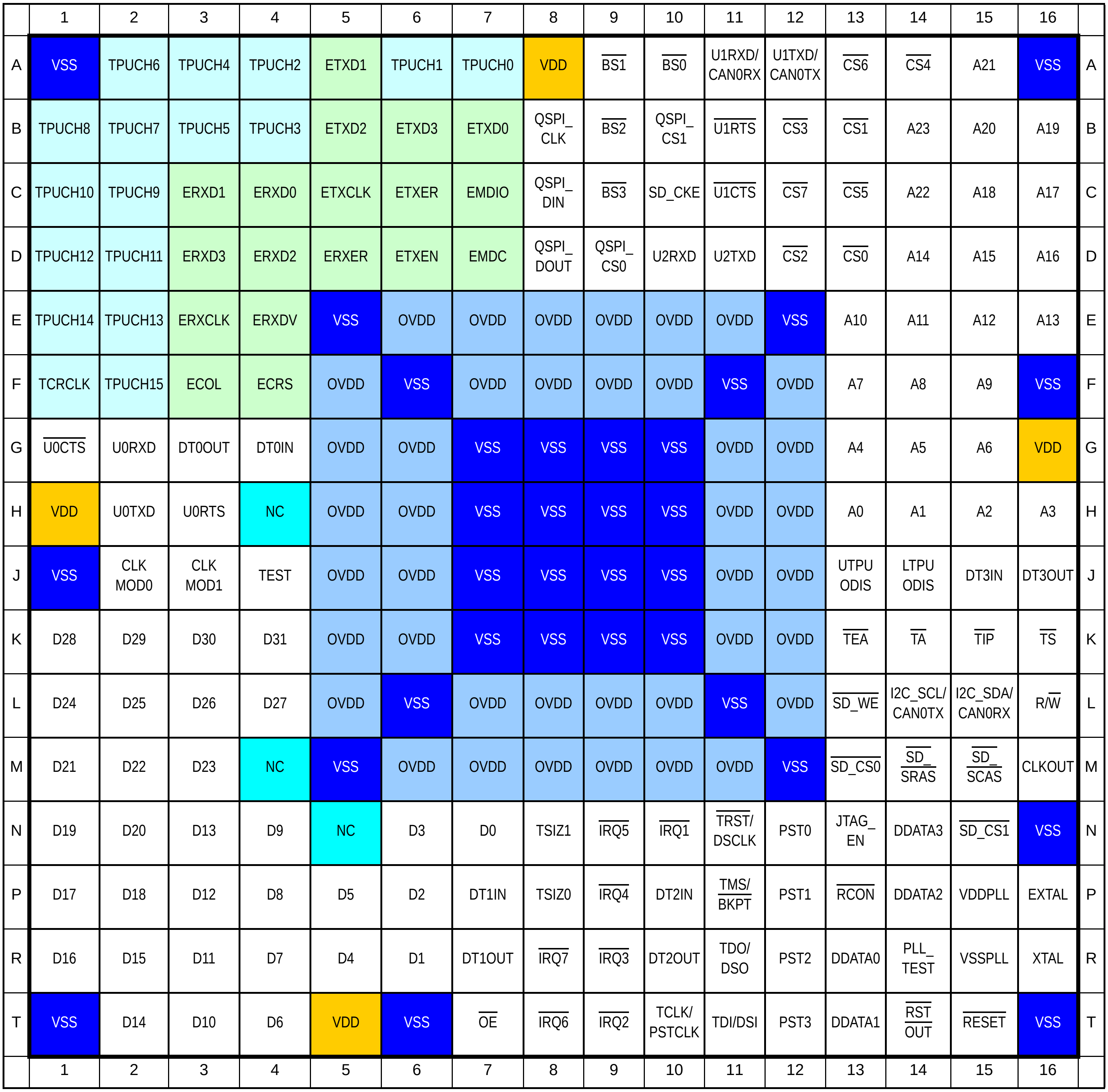
6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5232CVMxxx package.



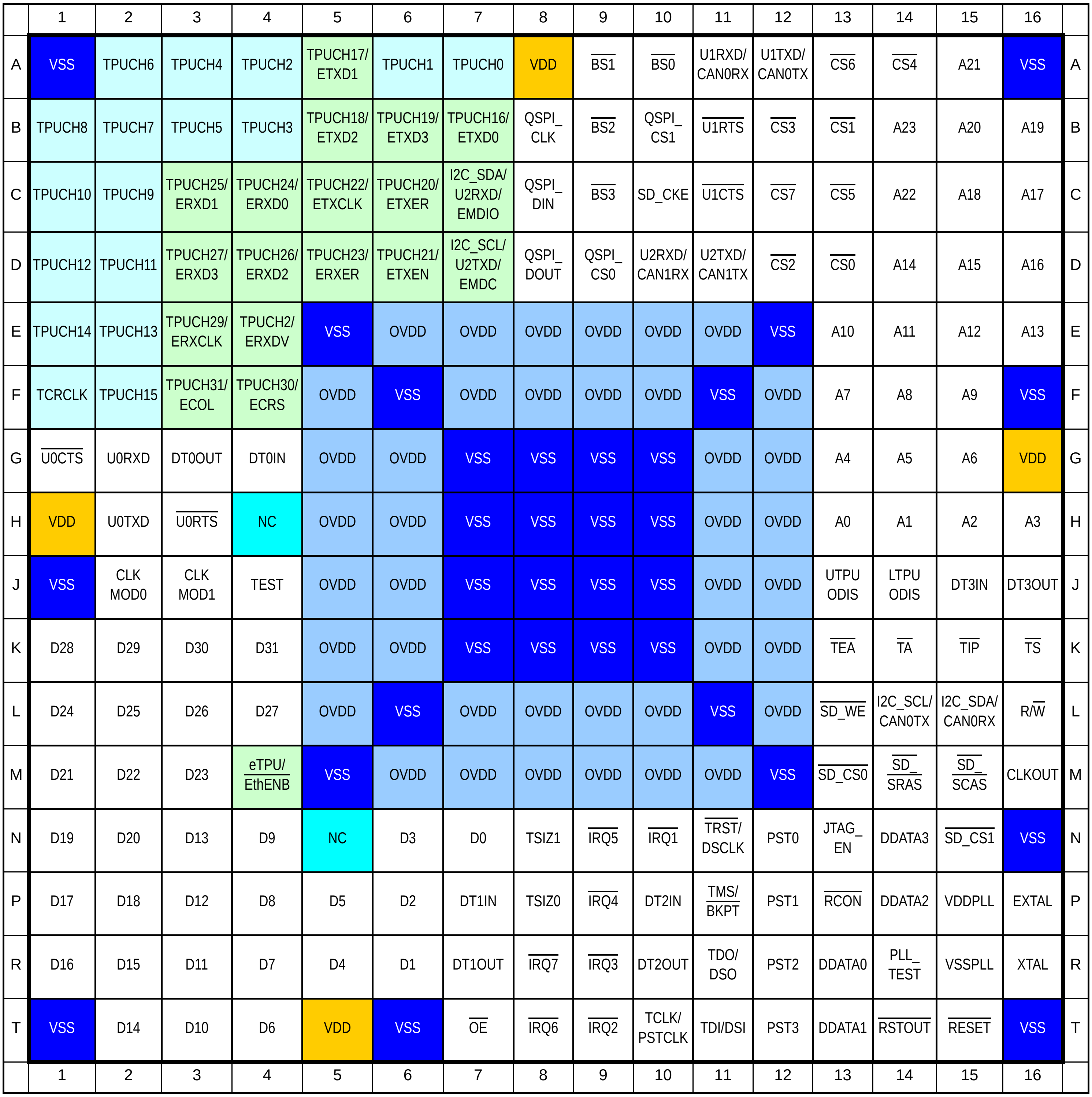
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	TPUCH6	TPUCH3	TPUCH2	QSPI_ DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{\mathrm{CS3}}$	$\overline{\mathrm{CS6}}$	$\overline{\mathrm{CS4}}$	A20	A17	VSS
B	TPUCH8	TPUCH7	TPUCH4	TPUCH0	QSPI_ DIN	$\overline{\mathrm{BS3}}$	QSPI_CS1	$\overline{\mathrm{U1CTS}}$	$\overline{\mathrm{CS7}}$	$\overline{\mathrm{CS1}}$	A23	A19	A16	A15
C	TPUCH10	TPUCH9	TPUCH5	TPUCH1	QSPI_CLK	$\overline{\mathrm{BS2}}$	$\overline{\mathrm{BS0}}$	$\overline{\mathrm{U1RTS}}$	$\overline{\mathrm{CS2}}$	$\overline{\mathrm{CS5}}$	A22	A18	A14	A13
D	TPUCH13	TPUCH12	TPUCH11	NC	NC	VDD	$\overline{\mathrm{BS1}}$	U1RXD/ CAN0RX	U1TXD/ CAN0TX	$\overline{\mathrm{CS0}}$	A21	A12	A11	A10
E	TPUCH14	TPUCH15	TCRCLK	DT0IN	OVDD	VSS	OVDD	SD_CKE	VSS	OVDD	A9	A8	A7	A6
F	U0TXD	U0RXD	$\overline{\mathrm{U0CTS}}$	DT0OUT	TEST	VSS	OVDD	VSS	OVDD	VSS	VDD	A5	A4	A3
G	D31	D30	$\overline{\mathrm{U0RTS}}$	VDD	CLKMOD1	OVDD	VSS	OVDD	VSS	LTPU ODIS	A2	A1	A0	DT3OUT
H	D29	D28	D27	D26	CLKMOD0	VSS	OVDD	OVDD	OVDD	UTPU ODIS	$\overline{\mathrm{TA}}$	$\overline{\mathrm{TIP}}$	$\overline{\mathrm{TS}}$	DT3IN
J	D25	D24	D23	D22	VSS	OVDD	VSS	OVDD	VSS	OVDD	I2C_SCL	I2C_SDA	R/$\overline{\mathrm{W}}$	$\overline{\mathrm{TEA}}$
K	D21	D20	D19	D18	OVDD	OVDD	VSS	OVDD	JTAG_EN	$\overline{\mathrm{RCON}}$	$\overline{\mathrm{SD\_SRAS}}$	$\overline{\mathrm{SD\_SCAS}}$	$\overline{\mathrm{SD\_WE}}$	CLKOUT
L	D17	D16	D10	VDD	D3	DT1IN	$\overline{\mathrm{IRQ5}}$	$\overline{\mathrm{IRQ1}}$	DT2OUT	PST0	DDATA0	$\overline{\mathrm{SD\_CS1}}$	$\overline{\mathrm{SD\_CS0}}$	VSSPLL
M	D15	D13	D9	D6	D2	DT1OUT	$\overline{\mathrm{IRQ6}}$	$\overline{\mathrm{IRQ2}}$	DT2IN	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL
N	D14	D12	D8	D5	D1	$\overline{\mathrm{OE}}$	$\overline{\mathrm{IRQ7}}$	$\overline{\mathrm{IRQ3}}$	$\overline{\mathrm{TRST}}$/ DSCLK	TDO/DSO	PST2	DDATA2	$\overline{\mathrm{RESET}}$	XTAL
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{\mathrm{IRQ4}}$	TCLK/ PSTCLK	TMS/ $\overline{\mathrm{BKPT}}$	PST1	DDATA1	$\overline{\mathrm{RSTOUT}}$	VSS

Figure 2. MCF5232CVMxxx Pinout (196 MAPBGA)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	ETXD1	TPUCH1	TPUCH0	VDD	$\overline{\text{BS1}}$	$\overline{\text{BS0}}$	U1RXD/ CAN0RX	U1TXD/ CAN0TX	$\overline{\text{CS6}}$	$\overline{\text{CS4}}$	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	ETXD2	ETXD3	ETXD0	QSPI_ CLK	$\overline{\text{BS2}}$	QSPI_ CS1	$\overline{\text{U1RTS}}$	$\overline{\text{CS3}}$	$\overline{\text{CS1}}$	A23	A20	A19	B
C	TPUCH10	TPUCH9	ERXD1	ERXD0	ETXCLK	ETXER	EMDIO	QSPI_ DIN	$\overline{\text{BS3}}$	SD_CKE	$\overline{\text{U1CTS}}$	$\overline{\text{CS7}}$	$\overline{\text{CS5}}$	A22	A18	A17	C
D	TPUCH12	TPUCH11	ERXD3	ERXD2	ERXER	ETXEN	EMDC	QSPI_ DOUT	QSPI_ CS0	U2RXD	U2TXD	$\overline{\text{CS2}}$	$\overline{\text{CS0}}$	A14	A15	A16	D
E	TPUCH14	TPUCH13	ERXCLK	ERXDV	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	ECOL	ECRS	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	$\overline{\text{U0CTS}}$	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	U0RTS	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{TEA}}$	$\overline{\text{TA}}$	$\overline{\text{TIP}}$	$\overline{\text{TS}}$	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	$\overline{\text{SD\_WE}}$	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/$\overline{\text{W}}$	L
M	D21	D22	D23	NC	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	$\overline{\text{SD\_CS0}}$	$\overline{\text{SD\_}}$ $\overline{\text{SRAS}}$	$\overline{\text{SD\_}}$ $\overline{\text{SCAS}}$	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ1}}$	$\overline{\text{TRST}}$/ DSCLK	PST0	JTAG_ EN	DDATA3	$\overline{\text{SD\_CS1}}$	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	$\overline{\text{IRQ4}}$	DT2IN	TMS/ $\overline{\text{BKPT}}$	PST1	$\overline{\text{RCON}}$	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ3}}$	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	$\overline{\text{OE}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	$\overline{\text{RST}}$ $\overline{\text{OUT}}$	$\overline{\text{RESET}}$	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 5. MCF5234CVMxxx Pinout (256 MAPBGA)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	TPUCH17/ ETXD1	TPUCH1	TPUCH0	VDD	$\overline{\mathrm{BS1}}$	$\overline{\mathrm{BS0}}$	U1RXD/ CAN0RX	U1TXD/ CAN0TX	$\overline{\mathrm{CS6}}$	$\overline{\mathrm{CS4}}$	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	TPUCH18/ ETXD2	TPUCH19/ ETXD3	TPUCH16/ ETXD0	QSPI_ CLK	$\overline{\mathrm{BS2}}$	QSPI_ CS1	$\overline{\mathrm{U1RTS}}$	$\overline{\mathrm{CS3}}$	$\overline{\mathrm{CS1}}$	A23	A20	A19	B
C	TPUCH10	TPUCH9	TPUCH25/ ERXD1	TPUCH24/ ERXD0	TPUCH22/ ETXCLK	TPUCH20/ ETXER	I2C_SDA/ U2RXD/ EMDIO	QSPI_ DIN	$\overline{\mathrm{BS3}}$	SD_CKE	$\overline{\mathrm{U1CTS}}$	$\overline{\mathrm{CS7}}$	$\overline{\mathrm{CS5}}$	A22	A18	A17	C
D	TPUCH12	TPUCH11	TPUCH27/ ERXD3	TPUCH26/ ERXD2	TPUCH23/ ERXER	TPUCH21/ ETXEN	I2C_SCL/ U2TXD/ EMDC	QSPI_ DOUT	QSPI_ CS0	U2RXD/ CAN1RX	U2TXD/ CAN1TX	$\overline{\mathrm{CS2}}$	$\overline{\mathrm{CS0}}$	A14	A15	A16	D
E	TPUCH14	TPUCH13	TPUCH29/ ERXCLK	TPUCH2/ ERXDV	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	TPUCH31/ ECOL	TPUCH30/ ECRS	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	$\overline{\mathrm{U0CTS}}$	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	$\overline{\mathrm{U0RTS}}$	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\mathrm{TEA}}$	$\overline{\mathrm{TA}}$	$\overline{\mathrm{TIP}}$	$\overline{\mathrm{TS}}$	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	$\overline{\mathrm{SD\_WE}}$	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/$\overline{\mathrm{W}}$	L
M	D21	D22	D23	eTPU/ $\overline{\mathrm{EthENB}}$	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	$\overline{\mathrm{SD\_CS0}}$	SD_ $\overline{\mathrm{SRAS}}$	SD_ $\overline{\mathrm{SCAS}}$	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	$\overline{\mathrm{IRQ5}}$	$\overline{\mathrm{IRQ1}}$	$\overline{\mathrm{TRST}}$/ DSCLK	PST0	JTAG_ EN	DDATA3	$\overline{\mathrm{SD\_CS1}}$	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	$\overline{\mathrm{IRQ4}}$	DT2IN	TMS/ BKPT	PST1	$\overline{\mathrm{RCON}}$	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	$\overline{\mathrm{IRQ7}}$	$\overline{\mathrm{IRQ3}}$	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	$\overline{\mathrm{OE}}$	$\overline{\mathrm{IRQ6}}$	$\overline{\mathrm{IRQ2}}$	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	$\overline{\mathrm{RSTOUT}}$	$\overline{\mathrm{RESET}}$	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 6. MCF5235CVMxxx Pinout (256 MAPBGA)

6.3 Pinout—160 QFP

Figure 8 shows a pinout of the MCF5232CABxxx package.

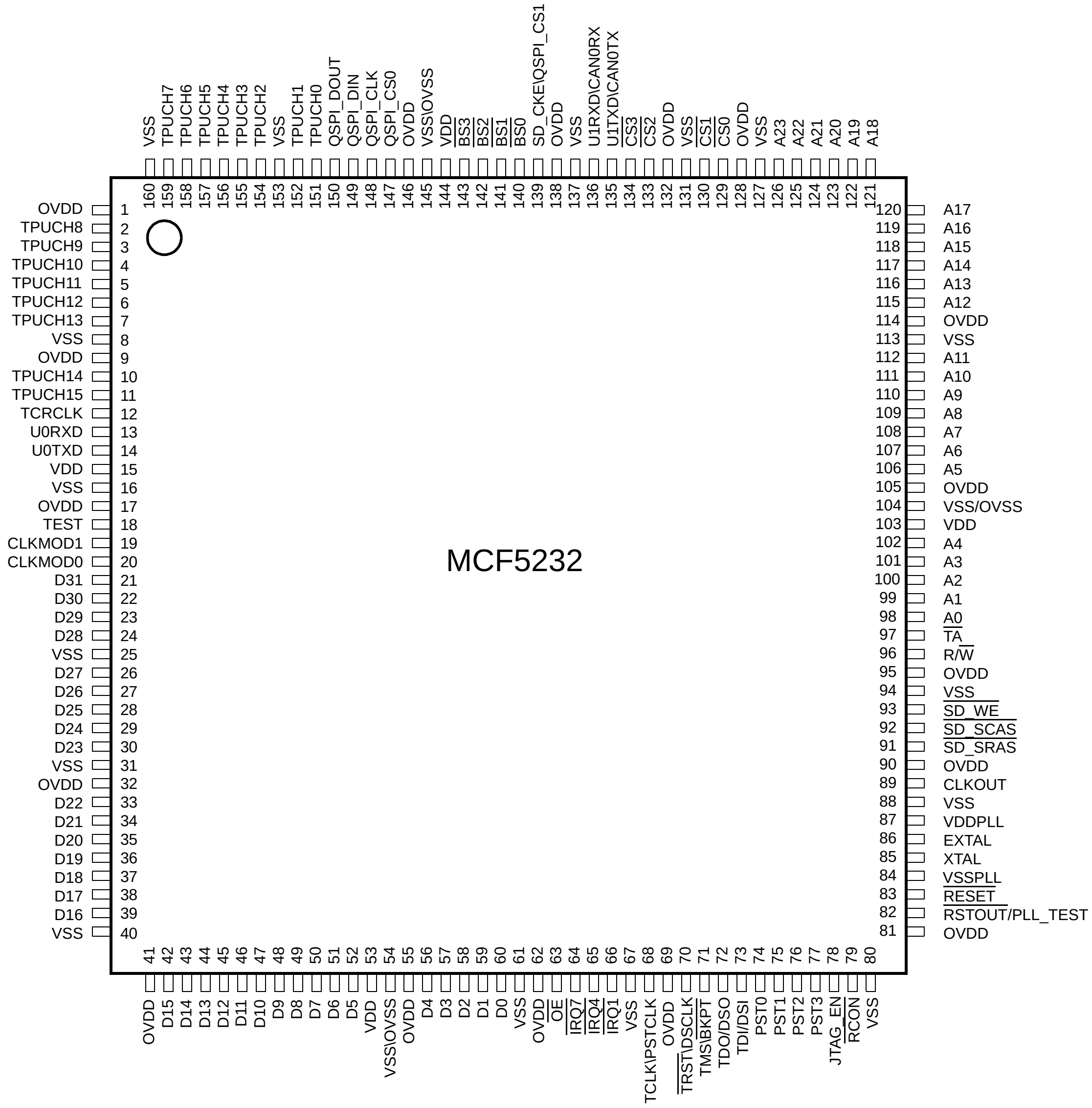
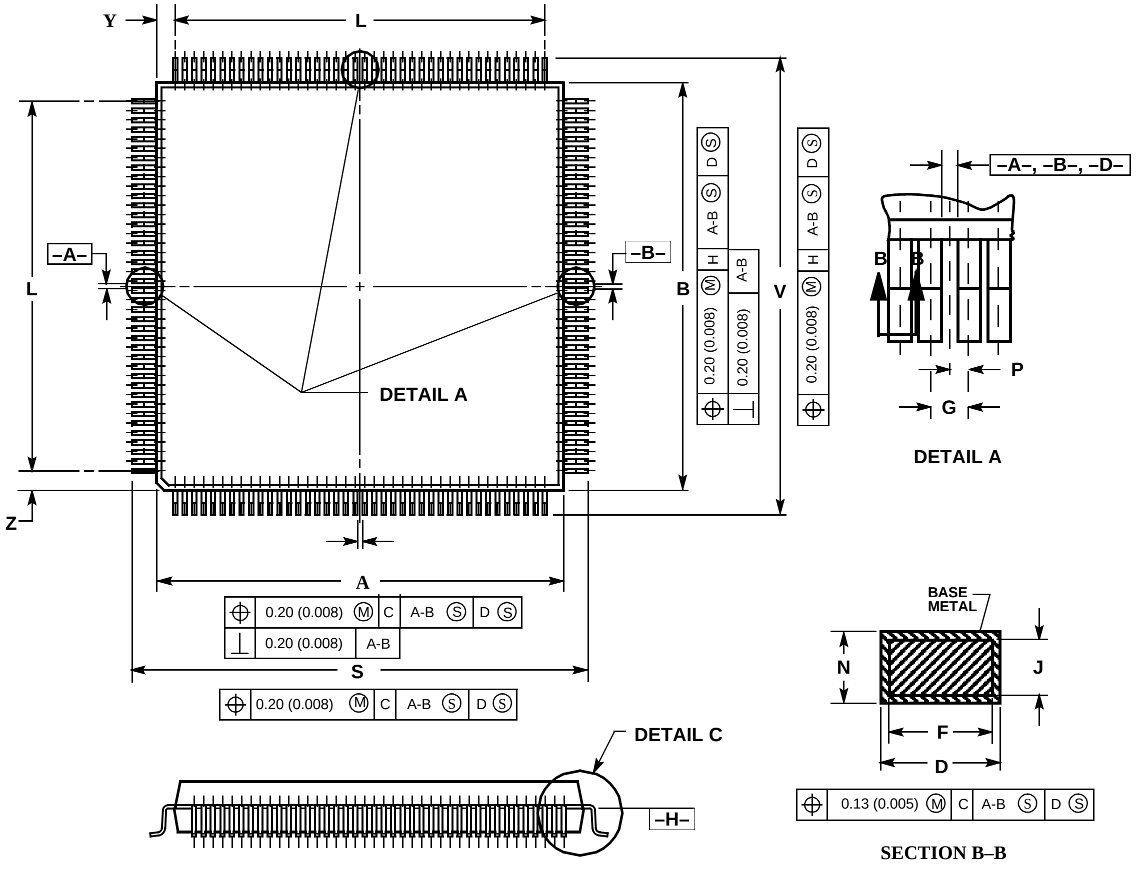
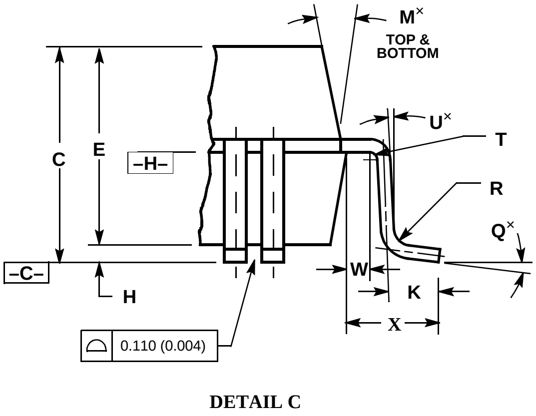


Figure 8. MCF5232CABxxx Pinout (160 QFP)

6.4 Package Dimensions—160 QFP

Figure 9 shows MCF5232CAB80 package dimensions.





NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 9. 160 QFP Package Dimensions

[1] Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

[2] This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

[3] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[4] All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

[5] Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	196 MAPBGA	160 QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	102	104	105[6]	^{o}C

[1] θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

[2] Per JEDEC JESD51-6 with the board horizontal.

[3] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[5] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

[6] At 100MHz.

Table 9. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	—	 7 7	pF
Load Capacitance[4] Low drive strength High drive strength	C_L		 — —	 25 50	 pF pF
Core Operating Supply Current [5] Master Mode	I_{DD}	 —	 135	 150	 mA
Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 100 TBD	 — —	 mA µA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} – 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total processor Limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10		 1.0 10	 mA mA

[1] Refer to Table 10 for additional PLL specifications.

[2] Refer to the MCF5235 signals section for pins having weak internal pull-up devices.

[3] This parameter is characterized before qualification rather than 100% tested.

[4] pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.

[5] Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

[6] All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

[7] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[8] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

7.4 Oscillator and PLLMRFM Electrical Characteristics

Table 10. HiP7 PLLMRFM Electrical Specifications[1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference 1:1 mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 25 25 75	MHz
2	Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{sys} $f_{sys/2}$	 0 $f_{ref} \div 32$	150 75 75	MHz MHz MHz
3	Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
4	Self Clocked Mode Frequency [4, 5]	f_{SCM}	10.25	15.25	MHz
5	Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms
6	XTAL Load Capacitance[5]		5	30	pF
7	PLL Lock Time [5, 7,13]	t_{lpll}	—	750	µs
8	Power-up To Lock Time [5, 6,8] With Crystal Reference (includes 5 time) Without Crystal Reference[9]	t_{lplk}	 — —	 11 750	 ms µs
9	1:1 Mode Clock Skew (between CLKOUT and EXTAL) [10]	t_{skew}	–1	1	ns
10	Duty Cycle of reference [5]	t_{dc}	40	60	%
11	Frequency un-LOCK Range	f_{UL}	–3.8	4.1	% $f_{sys/2}$
12	Frequency LOCK Range	f_{LCK}	–1.7	2.0	% $f_{sys/2}$
13	CLKOUT Period Jitter, [5, 6, 8,11, 12] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5.0 .01	 % $f_{sys/2}$
14	Frequency Modulation Range Limit[13,14] ($f_{sys/2}$ Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/2}$
15	ICO Frequency. $f_{ico} = f_{ref} \times 2 \times (MFD+2)$ [15]	f_{ico}	48	150	MHz

[1] All values given are initial design targets and subject to change.

[2] All internal registers retain data at 0 Hz.

[3] “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

[4] Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

[5] This parameter is guaranteed by characterization before qualification rather than 100% tested.

[6] Proper PC board layout procedures must be followed to achieve specifications.

Timings listed in Table 11 are shown in Figure 10.

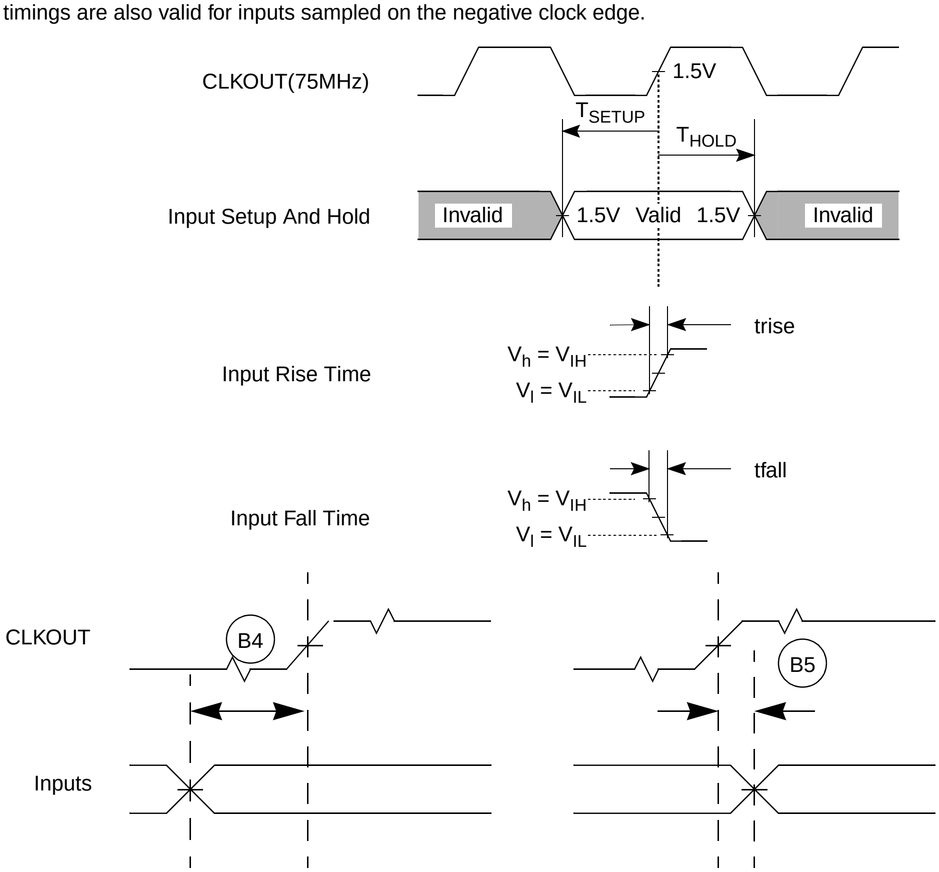


Figure 10. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

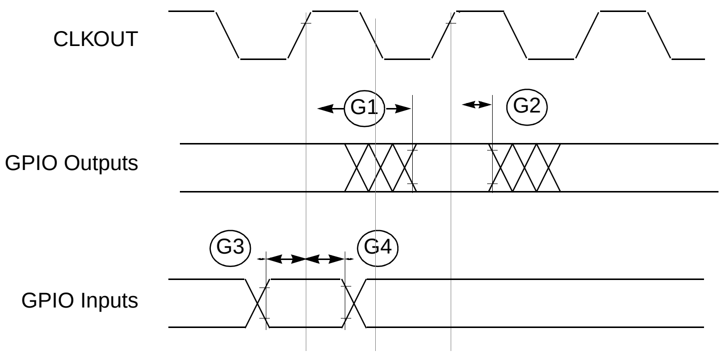


Figure 16. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

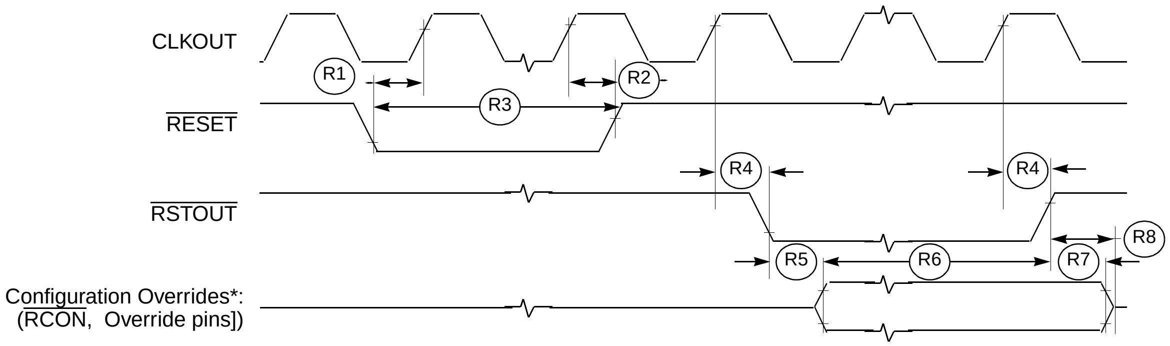


Figure 17. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

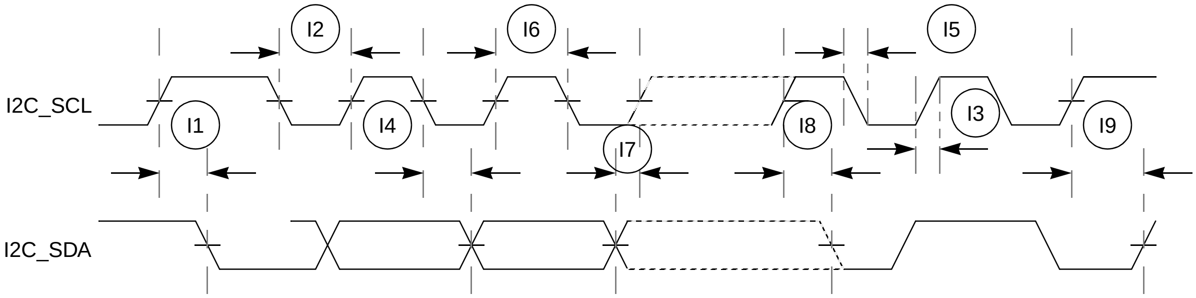


Figure 18. I^{2}C Input/Output Timings

7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	ERXD[3:0], ERXDV, ERXER to ERXCLK setup	5	—	ns
M2	ERXCLK to ERXD[3:0], ERXDV, ERXER hold	5	—	ns
M3	ERXCLK pulse width high	35%	65%	ERXCLK period
M4	ERXCLK pulse width low	35%	65%	ERXCLK period

Figure 19 shows MII receive signal timings listed in Table 18.

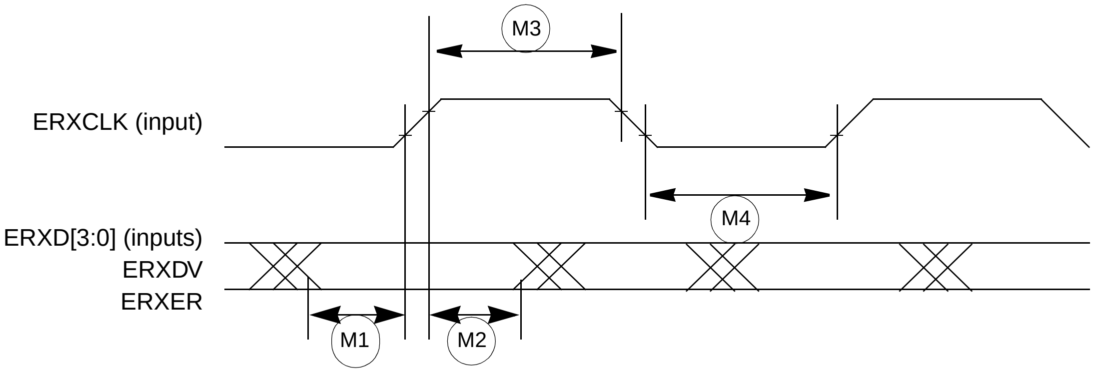


Figure 19. MII Receive Signal Timing Diagram

7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

Figure 22 shows MII serial management channel timings listed in Table 21.

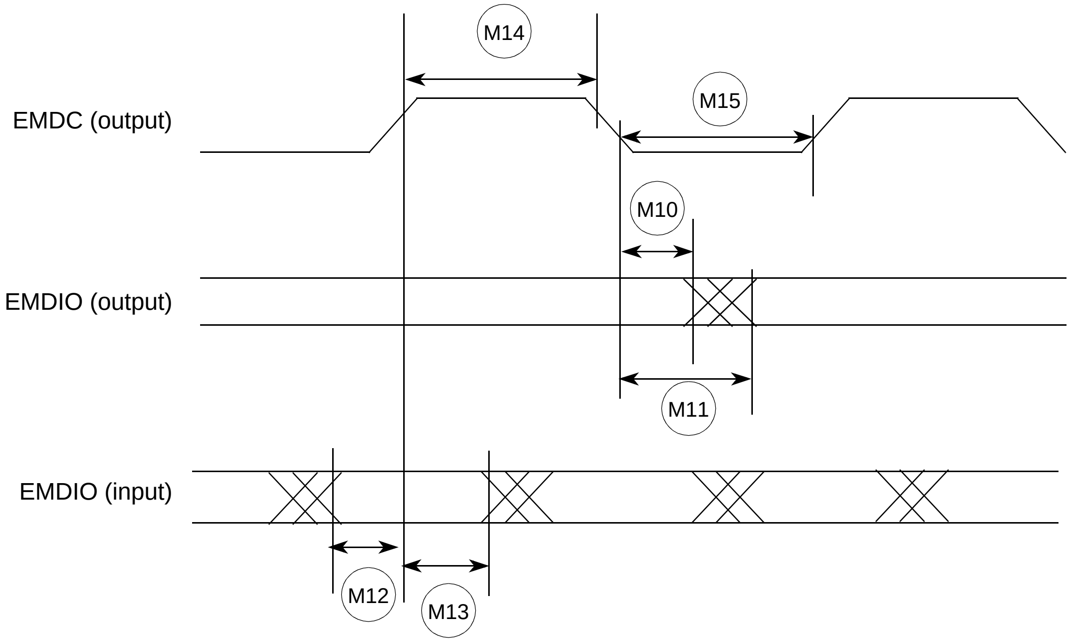


Figure 22. MII Serial Management Channel Timing Diagram

7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 23.

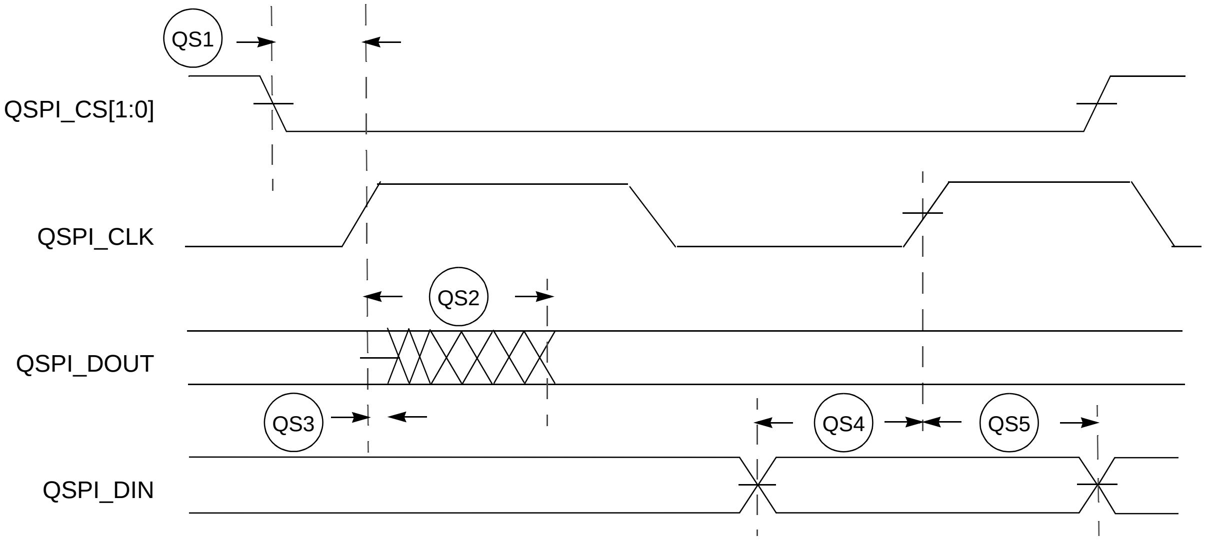


Figure 23. QSPI Timing

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

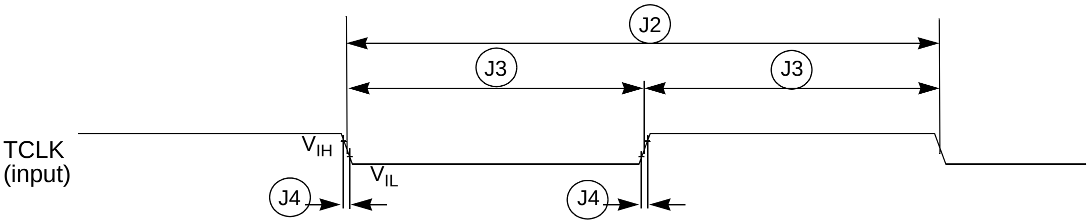


Figure 24. Test Clock Input Timing

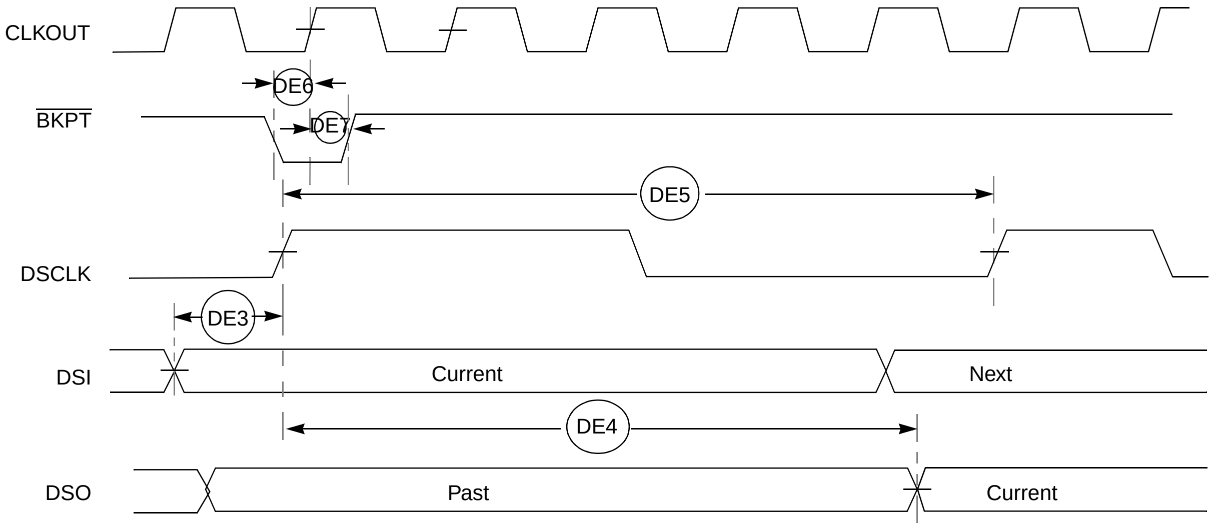


Figure 29. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF523*x* and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5235EC Revision History

Rev. No.	Substantive Change(s)
0	Preliminary release.
1	• Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Corrected Figure 8 pin 81. VDD instead of VSS • Changed instances of Motorola to Freescale
1.3	• Removed detailed signal description section. This information can be found in the MCF5235RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5235RM Chapter 1. • Corrected Figure 2 pin F10. VSS instead of VDD. Change made in Table 2 as well. • Corrected Figure 8 pin 81. OVDD instead of VDD. Change made in Table 2 as well. • Cleaned up many inconsistencies within the pinout figure signal names • Corrected document IDs in Documentation Table
1.4	• Added values for 'Maximum operating junction temperature' in Table 8. • Added typical values for 'Core operating supply current (master mode)' in Table 9. • Added typical values for 'Pad operating supply current (master mode)' in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.