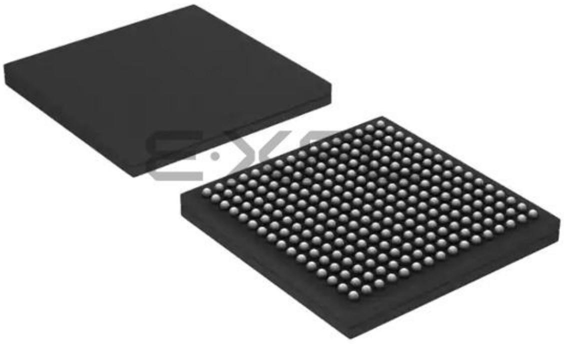


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5235cvm150

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
ECRS	—	—	—	I	—	—	—	F4	F4
ERXCLK	—	—	—	I	—	—	—	E3	E3
ERXDV	—	—	—	I	—	—	—	E4	E4
ERXD[3:0]	—	—	—	I	—	—	—	D3, D4, C3, C4	D3, D4, C3, C4
ERXER	—	—	—	I	—	—	—	D5	D5
ETXCLK	—	—	—	I	—	—	—	C5	C5
ETXEN	—	—	—	O	—	—	—	D6	D6
ETXER	—	—	—	O	—	—	—	C6	C6
ETXD[3:0]	—	—	—	O	—	—	—	B6, B5, A5, B7	B6, B5, A5, B7
Feature Control									
eTPU/$\overline{\text{EthENB}}$	—	—	—	I	—	—	—	—	M4
I^{2}C									
I2C_SDA	PFECI2C1	CAN0RX	—	I/O	—	J12	L15	L15	L15
I2C_SCL	PFECI2C0	CAN0TX	—	I/O	—	J11	L14	L14	L14
DMA									
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, TSIZ1and DT1OUT for DACK1, TSIZ0 and DT0OUT for DACK0, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and DT1IN for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—	—	—	—
QSPI									
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7	B10	B10	B10
QSPI_CS0	PQSPI3	—	—	O	147	A6	D9	D9	D9
QSPI_CLK	PQSPI2	I2C_SCL	—	O	148	C5	B8	B8	B8
QSPI_DIN	PQSPI1	I2C_SDA	—	I	149	B5	C8	C8	C8
QSPI_DOUT	PQSPI0	—	—	O	150	A5	D8	D8	D8
UARTs									
U2TXD	PUARTH1	CAN1TX	—	O	—	A8	D11	D11	D11
U2RXD	PUARTH0	CAN1RX	—	I	—	A7	D10	D10	D10
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	—	B8	C11	C11	C11
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	—	C8	B11	B11	B11
U1TXD	PUARTL5	CAN0TX	—	O	135	D9	A12	A12	A12

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
U1RXD	PUARTL4	CAN0RX	—	I	136	D8	A11	A11	A11
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	—	F3	G1	G1	G1
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	—	G3	H3	H3	H3
U0TXD	PUARTL1	—	—	O	14	F1	H2	H2	H2
U0RXD	PUARTL0	—	—	I	13	F2	G2	G2	G2
DMA Timers									
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14	J15	J15	J15
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14	J16	J16	J16
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	—	M9	P10	P10	P10
DT2OUT	PTIMER4	DACK2	—	O	—	L9	R10	R10	R10
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	—	L6	P7	P7	P7
DT1OUT	PTIMER2	DACK1	—	O	—	M6	R7	R7	R7
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	—	E4	G4	G4	G4
DT0OUT	PTIMER0	DACK0	—	O	—	F4	G3	G3	G3
BDM/JTAG[2]									
DSCLK	—	TRST	—	I	70	N9	N11	N11	N11
PSTCLK	—	TCLK	—	O	68	P9	T10	T10	T10
$\overline{\text{BKPT}}$	—	TMS	—	I	71	P10	P11	P11	P11
DSI	—	TDI	—	I	73	M10	T11	T11	T11
DSO	—	TDO	—	O	72	N10	R11	R11	R11
JTAG_EN	—	—	—	I	78	K9	N13	N13	N13
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11	N14, P14, T13, R13	N14, P14, T13, R13	N14, P14, T13, R13
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10	T12, R12, P12, N12	T12, R12, P12, N12	T12, R12, P12, N12

Table 2. MCF523x Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5232 160 QFP	MCF5232 196 MAPBGA	MCF5233 256 MAPBGA	MCF5234 256 MAPBGA	MCF5235 256 MAPBGA
Test									
TEST	—	—	—	I	18	F5	J4	J4	J4
PLL_TEST	—	—	—	I	—		R14	R14	R14
Power Supplies									
VDDPLL	—	—	—	I	87	M13	P15		
VSSPLL	—	—	—	I	84	L14	R15		
OVDD	—	—	—	I	1, 9, 17, 32, 41, 55, 62, 69, 81, 90, 95, 105, 114, 128, 132, 138, 146	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8	E6:11, F5, F7:10, F12, G5, G6, G11, G12, H5, H6, H11, H12, J5, J6, J11, J12, K5, K6, K11, K12, L5, L7:10, L12, M6:M11		
VSS	—	—	—	I	8, 16, 25, 31, 40, 54, 61, 67, 80, 88, 94, 104, 113, 127, 131, 137, 145, 153, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14	A1, A16, E5, E12, F6, F11, F16, G7:10, H7: 10, J1, J7:10, K7:10, L6, L11, M5, M12, N16, T1, T6, T16		
VDD	—	—	—	I	15, 53, 103, 144	D6, F11, G4, L4	A8, G16, H1, T5		

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

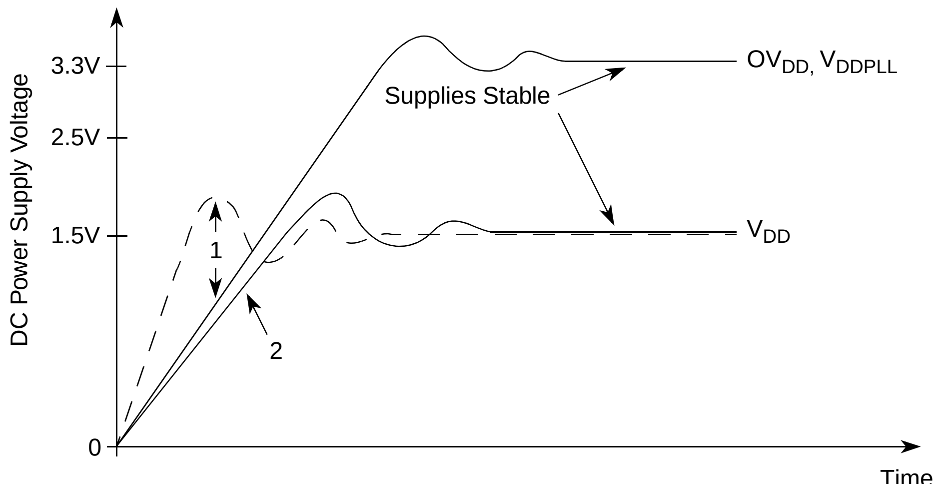
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF523*x*.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 µF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 1 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 1. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/V_{DDPLL} supplies.

5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, "Electrical Characteristics."

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
SD_SRAS	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. SD_SRAS should be connected to the corresponding SDRAM SD_SRAS. Do not confuse SD_SRAS with the DRAM controller's SD_CS[1:0], which should not be interfaced to the SDRAM SD_SRAS signals.
SD_SCAS	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. SD_SCAS should be connected to the corresponding signal labeled SD_SCAS on the SDRAM.
DRAMW	DRAM read/write. Asserted for write operations and negated for read operations.
SD_CS[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF523*x*. One SD_CS signal selects one SDRAM block and connects to the corresponding CS signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
BS[3:0]	Column address strobe. For synchronous operation, BS[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5235 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF523*x* Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]

6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5232CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	TPUCH6	TPUCH3	TPUCH2	QSPI_ DOUT	QSPI_CS0	U2RXD	U2TXD	CS3	CS6	CS4	A20	A17	VSS	A
B	TPUCH8	TPUCH7	TPUCH4	TPUCH0	QSPI_ DIN	BS3	QSPI_CS1	U1CTS	CS7	CS1	A23	A19	A16	A15	B
C	TPUCH10	TPUCH9	TPUCH5	TPUCH1	QSPI_CLK	BS2	BS0	U1RTS	CS2	CS5	A22	A18	A14	A13	C
D	TPUCH13	TPUCH12	TPUCH11	NC	NC	VDD	BS1	U1RXD/ CAN0RX	U1TXD/ CAN0TX	CS0	A21	A12	A11	A10	D
E	TPUCH14	TPUCH15	TCRCLK	DT0IN	OVDD	VSS	OVDD	SD_CKE	VSS	OVDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	U0CTS	DT0OUT	TEST	VSS	OVDD	VSS	OVDD	VSS	VDD	A5	A4	A3	F
G	D31	D30	U0RTS	VDD	CLKMOD1	OVDD	VSS	OVDD	VSS	LTPU ODIS	A2	A1	A0	DT3OUT	G
H	D29	D28	D27	D26	CLKMOD0	VSS	OVDD	OVDD	OVDD	UTPU ODIS	TA	TIP	TS	DT3IN	H
J	D25	D24	D23	D22	VSS	OVDD	VSS	OVDD	VSS	OVDD	I2C_SCL	I2C_SDA	R/W	TEA	J
K	D21	D20	D19	D18	OVDD	OVDD	VSS	OVDD	JTAG_EN	RCON	SD_SRAS	SD_SCAS	SD_WE	CLKOUT	K
L	D17	D16	D10	VDD	D3	DT1IN	IRQ5	IRQ1	DT2OUT	PST0	DDATA0	SD_CS1	SD_CS0	VSSPLL	L
M	D15	D13	D9	D6	D2	DT1OUT	IRQ6	IRQ2	DT2IN	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	OE	IRQ7	IRQ3	TRST/ DSCLK	TDO/DSO	PST2	DDATA2	RESET	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	IRQ4	TCLK/ PSTCLK	TMS/ BKPT	PST1	DDATA1	RSTOUT	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

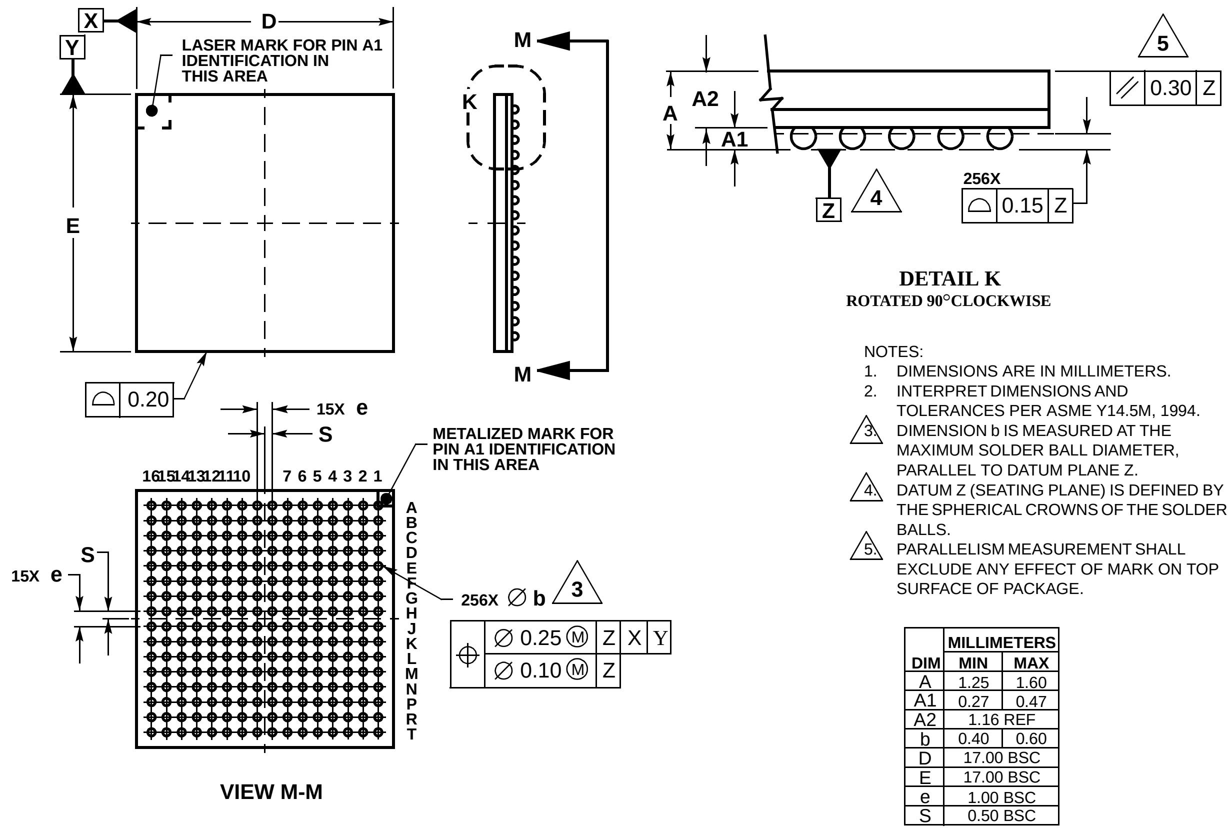
Figure 2. MCF5232CVMxxx Pinout (196 MAPBGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	TPUCH6	TPUCH4	TPUCH2	TPUCH17/ ETXD1	TPUCH1	TPUCH0	VDD	BS1	BS0	U1RXD/ CAN0RX	U1TXD/ CAN0TX	CS6	CS4	A21	VSS	A
B	TPUCH8	TPUCH7	TPUCH5	TPUCH3	TPUCH18/ ETXD2	TPUCH19/ ETXD3	TPUCH16/ ETXD0	QSPI_ CLK	BS2	QSPI_ CS1	U1RTS	CS3	CS1	A23	A20	A19	B
C	TPUCH10	TPUCH9	TPUCH25/ ERXD1	TPUCH24/ ERXD0	TPUCH22/ ETXCLK	TPUCH20/ ETXER	I2C_SDA/ U2RXD/ EMDIO	QSPI_ DIN	BS3	SD_CKE	U1CTS	CS7	CS5	A22	A18	A17	C
D	TPUCH12	TPUCH11	TPUCH27/ ERXD3	TPUCH26/ ERXD2	TPUCH23/ ERXER	TPUCH21/ ETXEN	I2C_SCL/ U2TXD/ EMDC	QSPI_ DOUT	QSPI_ CS0	U2RXD/ CAN1RX	U2TXD/ CAN1TX	CS2	CS0	A14	A15	A16	D
E	TPUCH14	TPUCH13	TPUCH29/ ERXCLK	TPUCH2/ ERXDV	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	A10	A11	A12	A13	E
F	TCRCLK	TPUCH15	TPUCH31/ ECOL	TPUCH30/ ECRS	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	A7	A8	A9	VSS	F
G	U0CTS	U0RXD	DT0OUT	DT0IN	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A4	A5	A6	VDD	G
H	VDD	U0TXD	U0RTS	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	A0	A1	A2	A3	H
J	VSS	CLK MOD0	CLK MOD1	TEST	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	UTPU ODIS	LTPU ODIS	DT3IN	DT3OUT	J
K	D28	D29	D30	D31	OVDD	OVDD	VSS	VSS	VSS	VSS	OVDD	OVDD	TEA	TA	TIP	TS	K
L	D24	D25	D26	D27	OVDD	VSS	OVDD	OVDD	OVDD	OVDD	VSS	OVDD	SD_WE	I2C_SCL/ CAN0TX	I2C_SDA/ CAN0RX	R/W	L
M	D21	D22	D23	eTPU/ EthENB	VSS	OVDD	OVDD	OVDD	OVDD	OVDD	OVDD	VSS	SD_CS0	SD_ SRAS	SD_ SCAS	CLKOUT	M
N	D19	D20	D13	D9	NC	D3	D0	TSIZ1	IRQ5	IRQ1	TRST/ DSCLK	PST0	JTAG_ EN	DDATA3	SD_CS1	VSS	N
P	D17	D18	D12	D8	D5	D2	DT1IN	TSIZ0	IRQ4	DT2IN	TMS/ BKPT	PST1	RCON	DDATA2	VDDPLL	EXTAL	P
R	D16	D15	D11	D7	D4	D1	DT1OUT	IRQ7	IRQ3	DT2OUT	TDO/ DSO	PST2	DDATA0	PLL_ TEST	VSSPLL	XTAL	R
T	VSS	D14	D10	D6	VDD	VSS	OE	IRQ6	IRQ2	TCLK/ PSTCLK	TDI/DSI	PST3	DDATA1	RSTOUT	RESET	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 6. MCF5235CVMxxx Pinout (256 MAPBGA)

6.2.2 Package Dimensions—256 MAPBGA

Figure 7 shows MCF5235CVMxxx, MCF5234CVMxxx, and MCF5233CVMxx package dimensions.



DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 7. 256 MAPBGA Package Outline

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D= $P_{INT} + P_{I/O}$

P_{INT}= $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3 DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} – 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	—	1.0	μA
High Impedance (Off-State) Leakage Current $V_{in} = V_{DD}$ or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	—	1.0	μA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	–10	—	– 130	μA

Read/write bus timings listed in Table 12 are shown in Figure 11, Figure 12, and Figure 13.

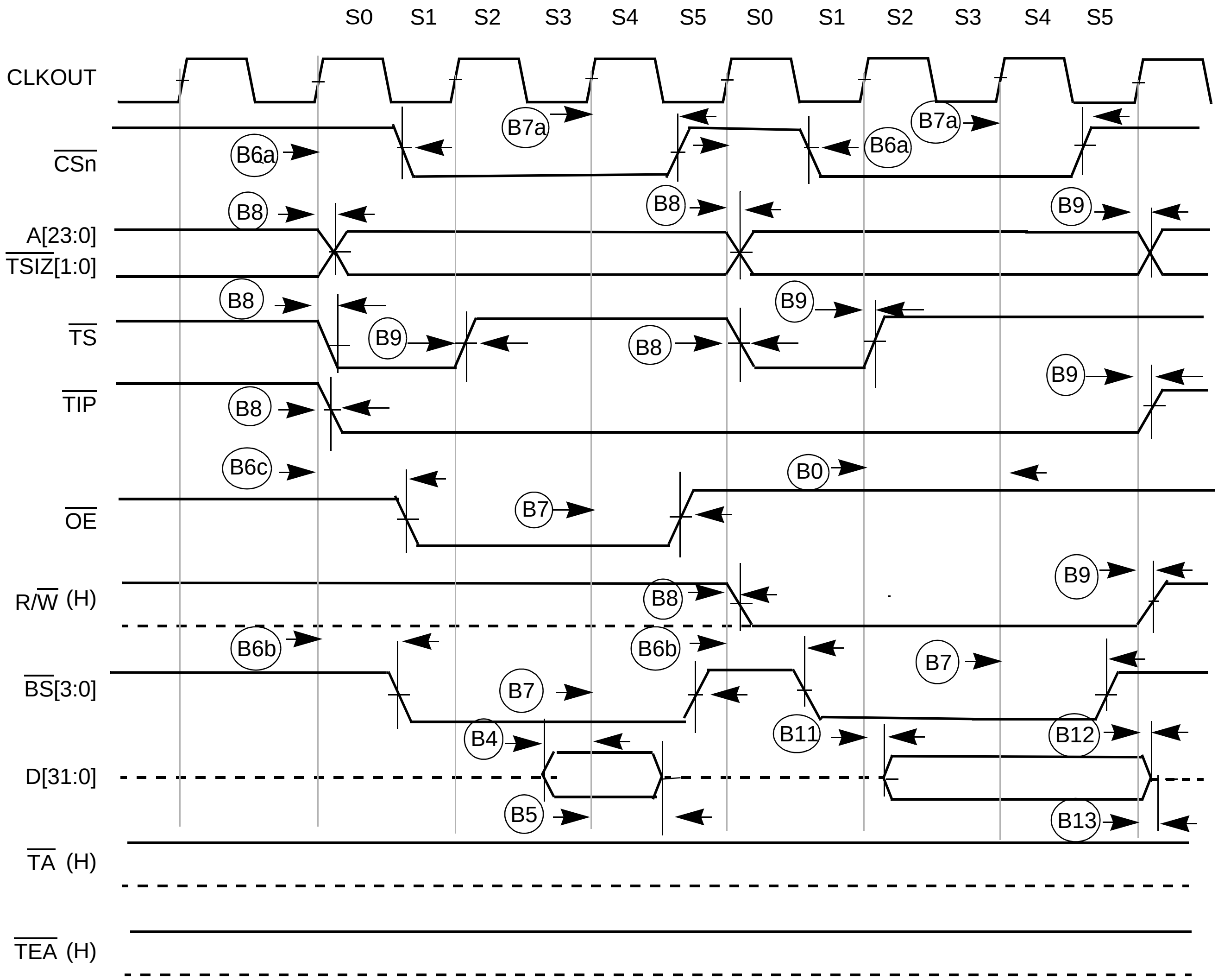


Figure 11. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 12 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

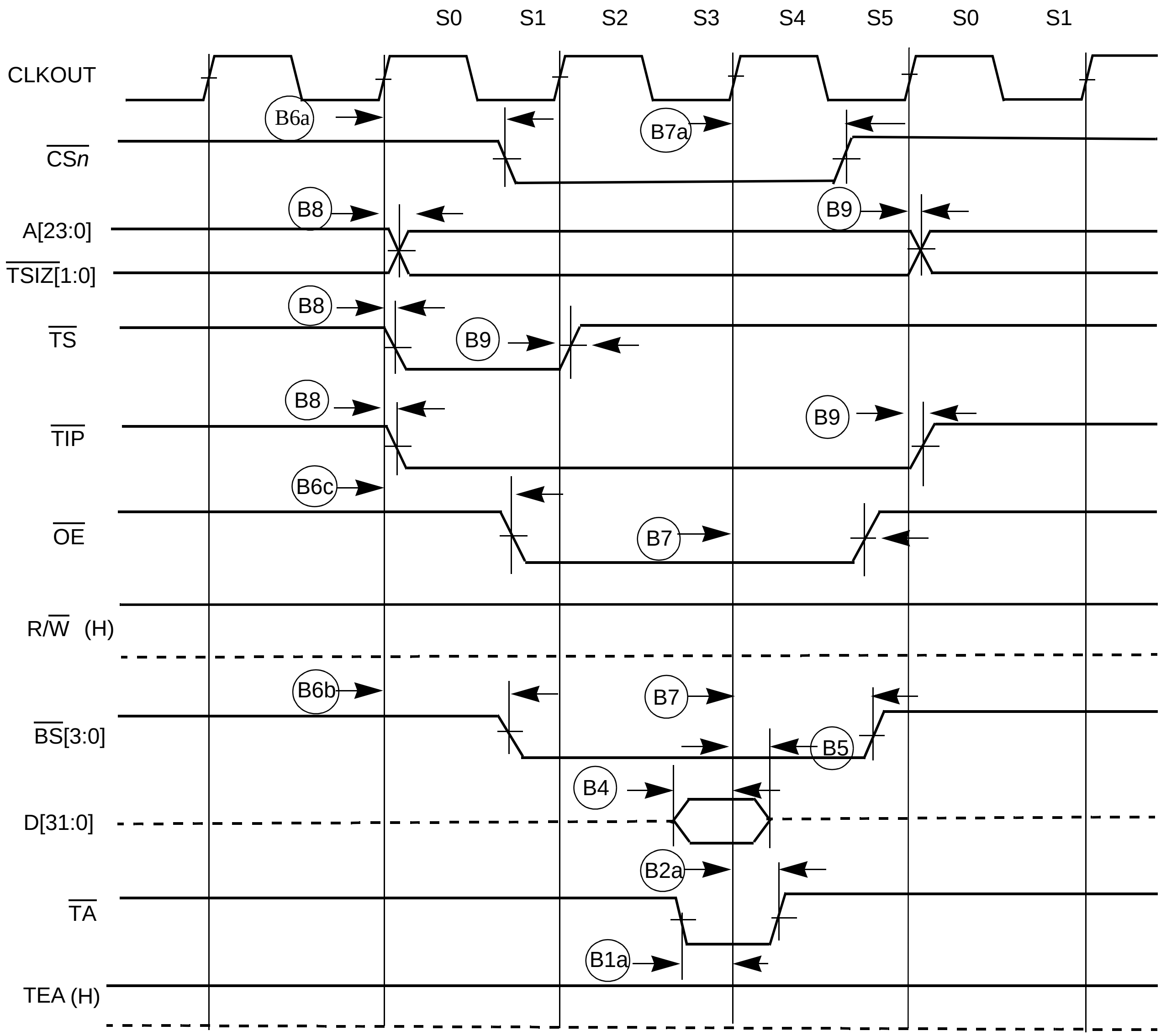


Figure 12. SRAM Read Bus Cycle Terminated by $\overline{TA}$

Figure 13 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

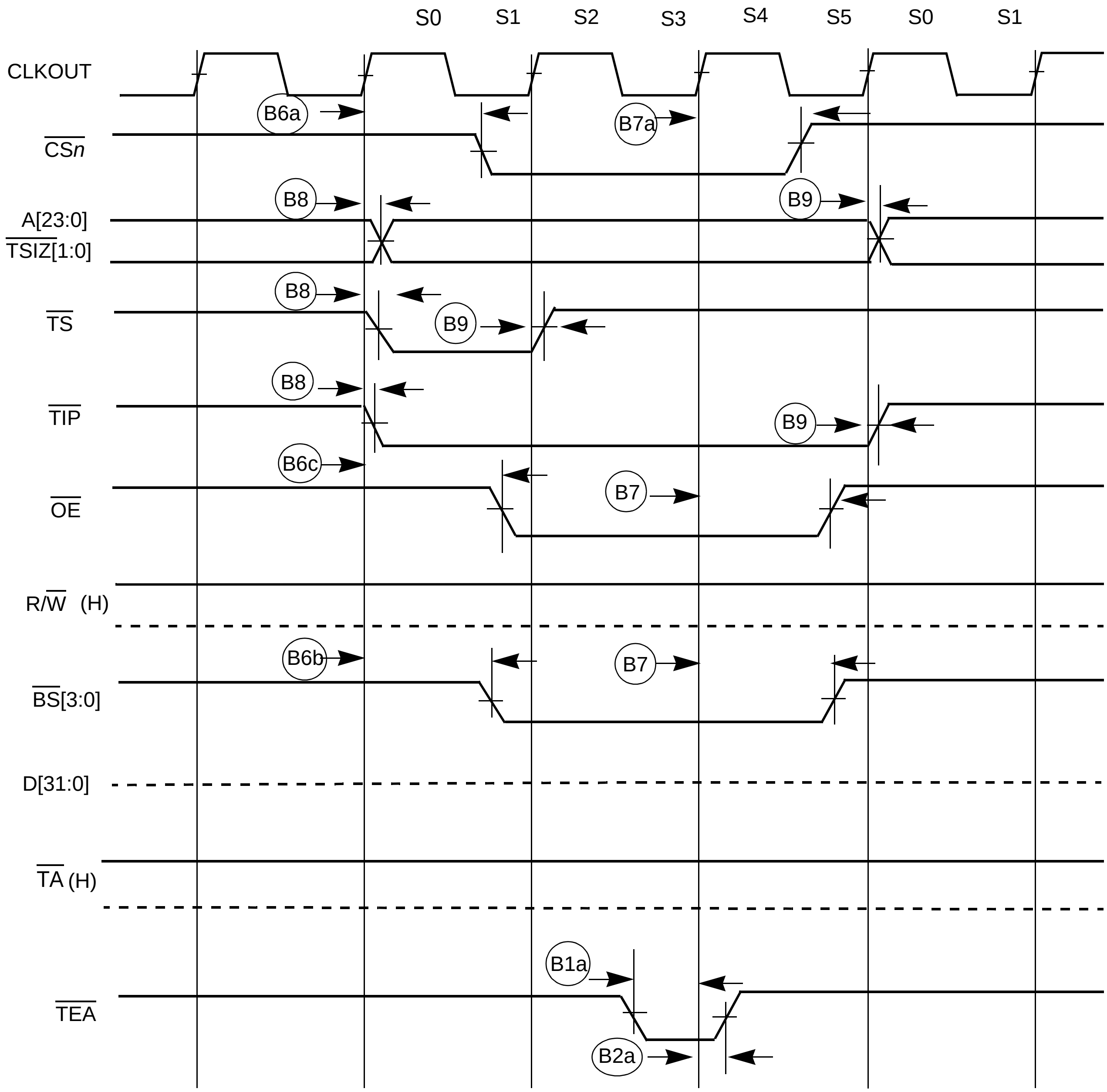


Figure 13. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

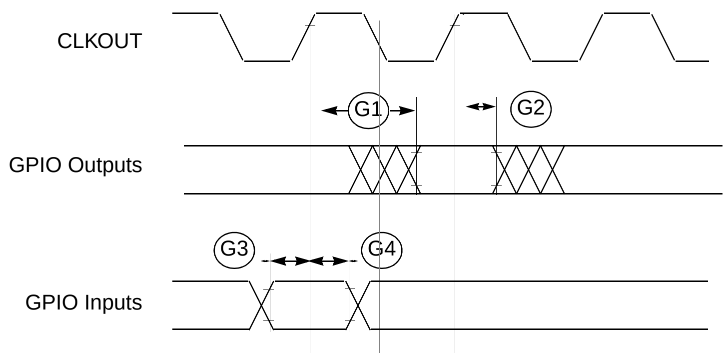


Figure 16. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.
[2] During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

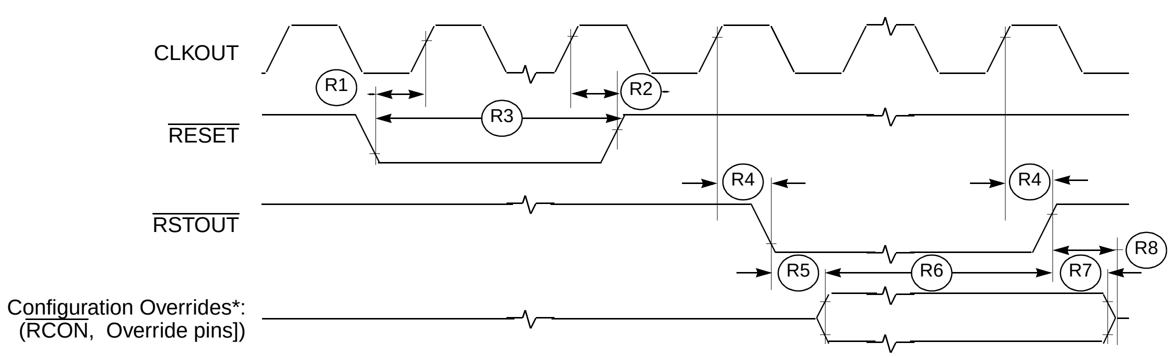


Figure 17. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	ETXCLK to ETXD[3:0], ETXEN, ETXER invalid	5	—	ns
M6	ETXCLK to ETXD[3:0], ETXEN, ETXER valid	—	25	ns
M7	ETXCLK pulse width high	35%	65%	ETXCLK period
M8	ETXCLK pulse width low	35%	65%	ETXCLK period

Figure 20 shows MII transmit signal timings listed in Table 19.

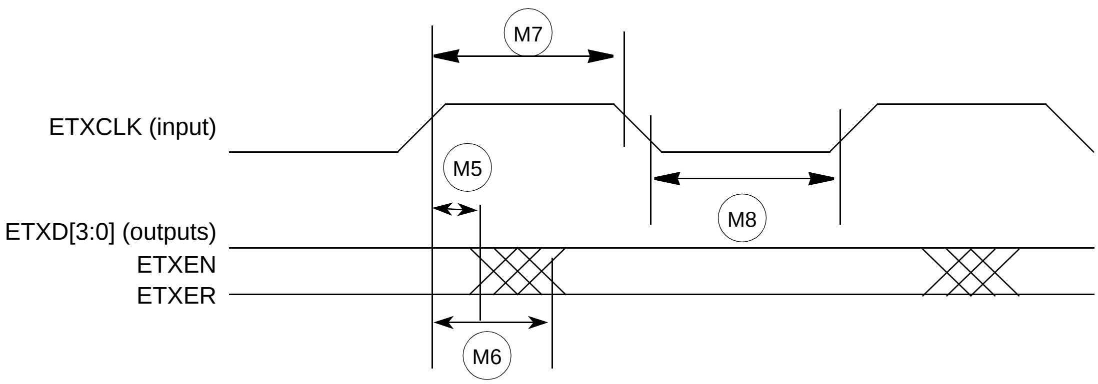


Figure 20. MII Transmit Signal Timing Diagram

7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	ECRS, ECOL minimum pulse width	1.5	—	ETXCLK period

Figure 21 shows MII asynchronous input timings listed in Table 20.

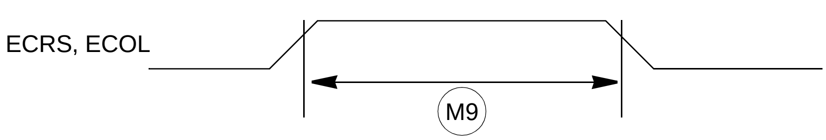


Figure 21. MII Async Inputs Timing Diagram

7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 23.

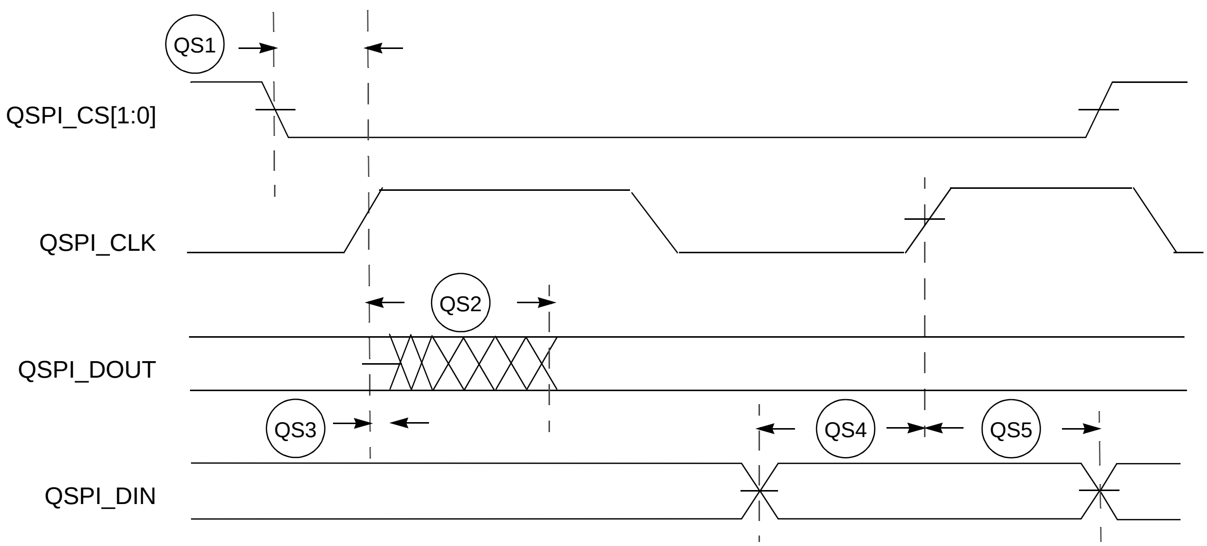


Figure 23. QSPI Timing

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

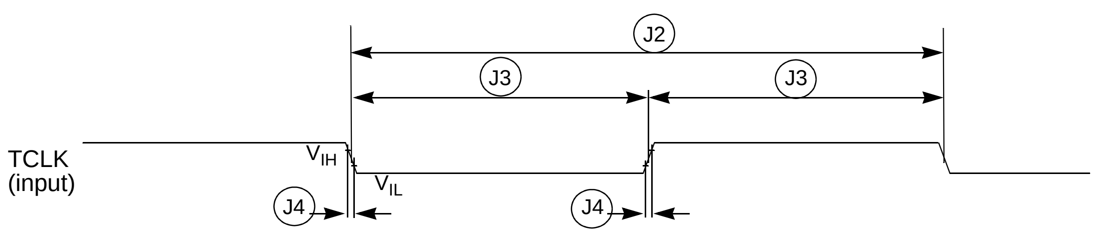


Figure 24. Test Clock Input Timing

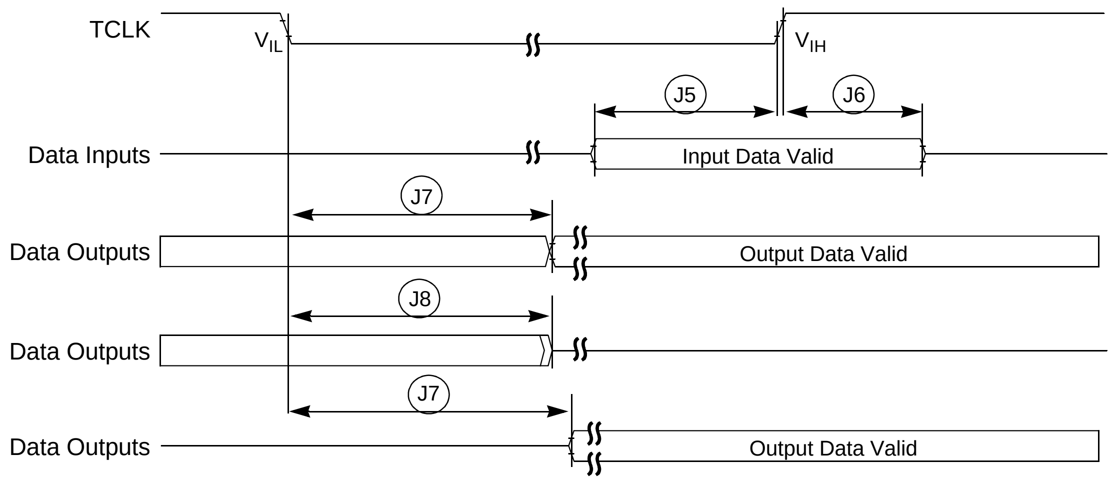


Figure 25. Boundary Scan (JTAG) Timing

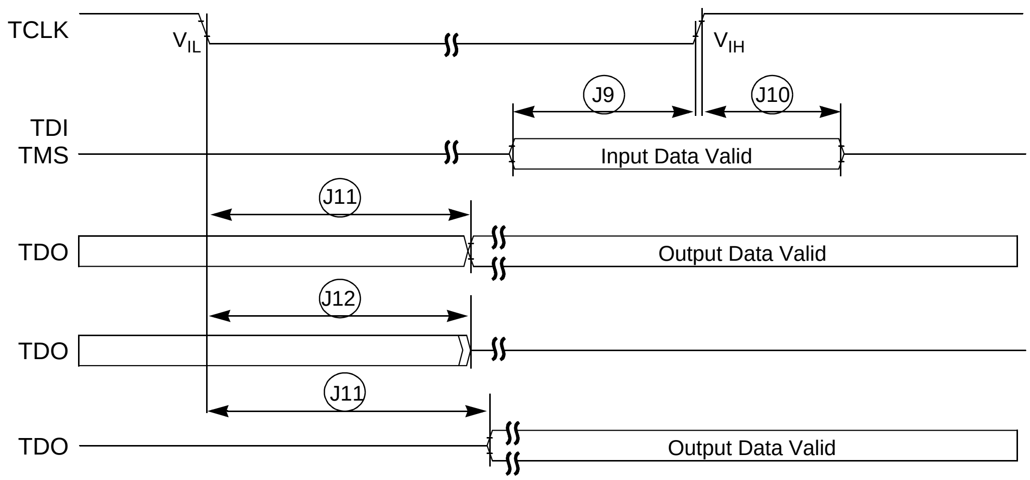


Figure 26. Test Access Port Timing

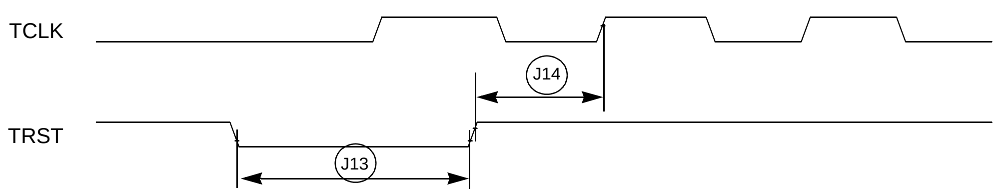


Figure 27. $\overline{\text{TRST}}$ Timing

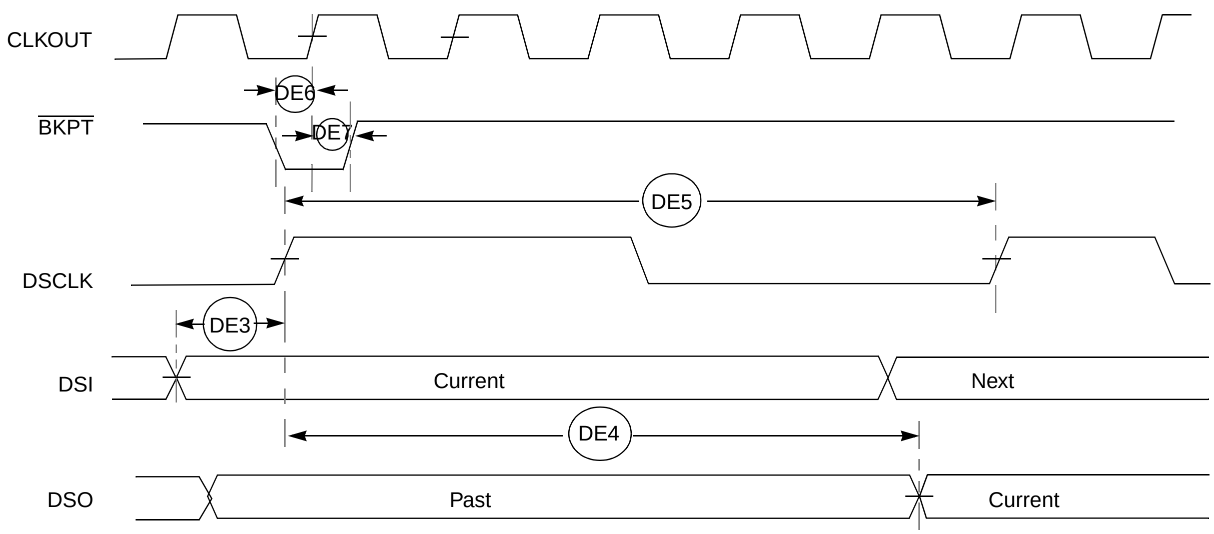


Figure 29. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF523*x* and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5235EC Revision History

Rev. No.	Substantive Change(s)
0	Preliminary release.
1	• Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Corrected Figure 8 pin 81. VDD instead of VSS • Changed instances of Motorola to Freescale
1.3	• Removed detailed signal description section. This information can be found in the MCF5235RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5235RM Chapter 1. • Corrected Figure 2 pin F10. VSS instead of VDD. Change made in Table 2 as well. • Corrected Figure 8 pin 81. OVDD instead of VDD. Change made in Table 2 as well. • Cleaned up many inconsistencies within the pinout figure signal names • Corrected document IDs in Documentation Table
1.4	• Added values for 'Maximum operating junction temperature' in Table 8. • Added typical values for 'Core operating supply current (master mode)' in Table 9. • Added typical values for 'Pad operating supply current (master mode)' in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.

Table 26. MCF5235EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.5	• Removed Overview, Features, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5235 Reference Manual. • Removed list of documentation table in Section 8, "Documentation.". An up-to-date list is always available on our web site.
1.6	• Table 9: Changed core supply voltage (V_{DD}) from 1.35-1.65 to 1.4-1.6.
1.7	• Table 10: Changed max f_{ICO} frequency from "75 MHz" to "150 MHz".
1.8	• Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." • Updated 196MAPBGA package dimensions, Figure 3.
2	• Table 2: Changed SD_CKE pin location from 139 to "—" for the 160QFP device. Changed QSPI_CS1 pin location from "—" to 139 for the 160QFP device. • Figure 8: Changed pin 139 label from "SD_CKE/QSPI_CS1" to "QSPI_CS1/SD_CKE". • Removed second sentence from Section 7.10.1, "MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)," and Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, "MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)," as this feature is not supported on this device.
3	• Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions" Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, "Power Up Sequence" first bullet, changed "Use 1 µs" to "Use 1 ms". • Corrected position of spec D5 in Figure 14. • Table 14: Added $\overline{\text{DACK}n}$ and $\overline{\text{DREQ}n}$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5235CVF150 in Table 6