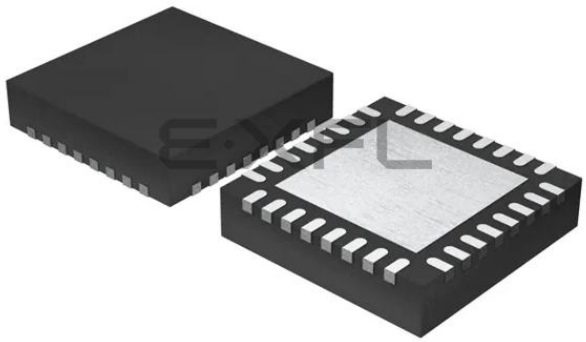

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, FlexIO, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 8x16b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl27z32vfm4 |

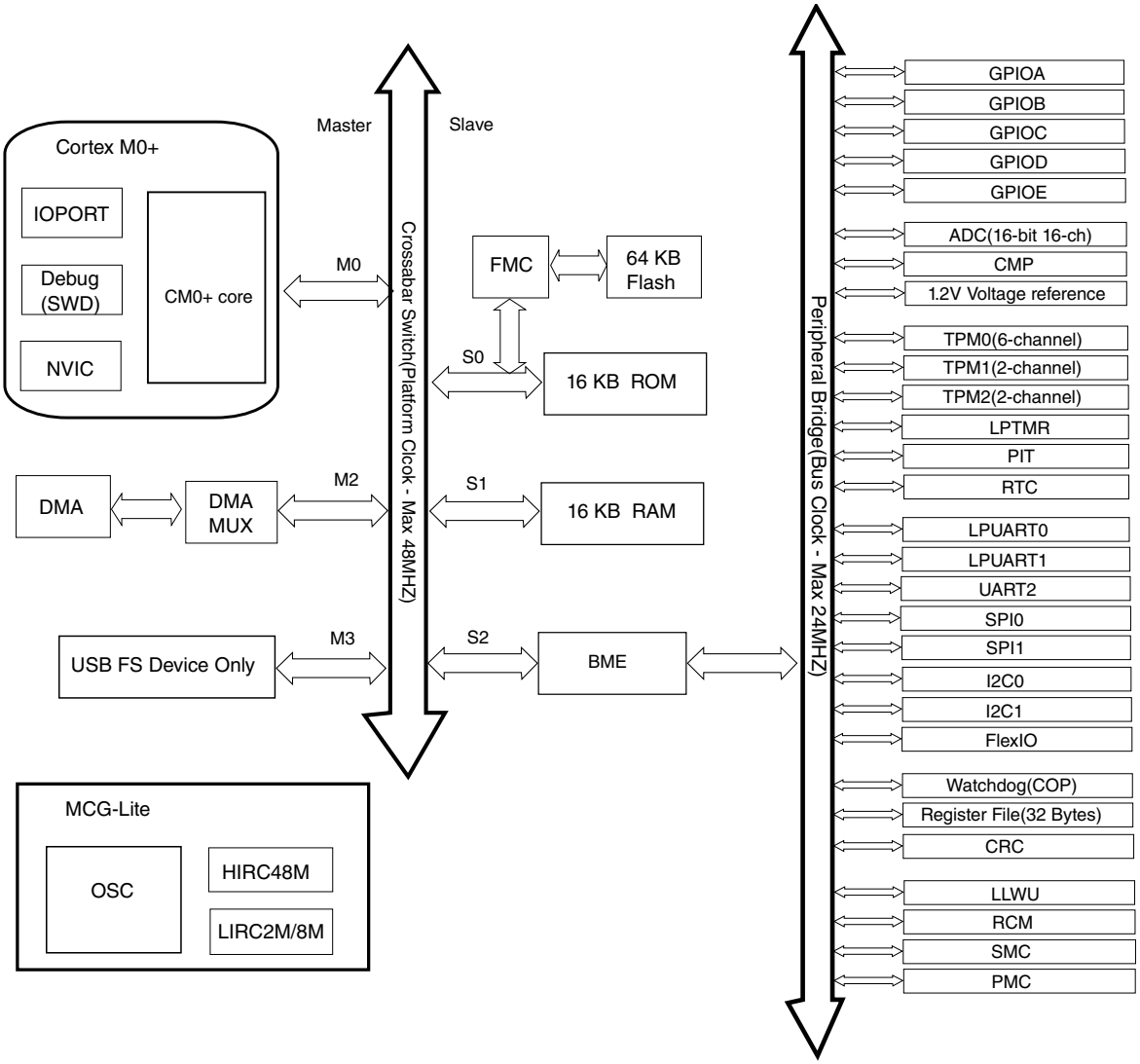



**Figure 1. System diagram**

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

## 2.1 System features

The following sections describe the high-level system features.

**Table 6. Peripherals states in different operational modes (continued)**

| Core mode | Device mode | Descriptions |
|---|---|---|
| Deep sleep | Stop | In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTimer, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt. |
| | Very Low Power Stop | In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, USB, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt. |
| | Low Leakage Stop | In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, CRC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM, UART, USB, and COP are static, but retain their programming. The GPIO, and VREF are static, retain their programming, and continue to drive their previous values. |
| | Very Low Leakage Stop | In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes.<br>In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving.<br>In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving.<br>In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled. |

## 2.1.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 8 external wakeup pin inputs and 4 internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-Calibration mode

#### 2.2.4.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see Table 56 for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031. We recommend to use internal reference voltage as ADC reference with long sample time.

### 2.2.5 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC or CMP.

The VREF supports the following programmable buffer modes:

- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

The VREF voltage output signal, bonded on VREFH for 48 QFN, 64 LQFP and 64 MAPBGA packages and on PTE30 for 32 QFN and 36 XFBGA packages, can be used by both internal and external peripherals in low and high power buffer mode. A 100 nF capacitor must always be connected between this pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

### 2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has two independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

### 2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers
- Support DMA

### 2.2.14 I2C

This device contains two I2C modules, which support up to 1 Mbits/s by dual buffer features, and address match to wake MCU from the low power mode.

I2C modules support DMA transfer, and the interrupt condition can trigger DMA request when DMA function is enabled.

The I2C modules have the following features:

- Support for system management bus (SMBus) Specification, version 2
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

| 64 LQFP | 36 XFBGA | 32 QFN | 48 QFN | 64 MAPBGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 50 | A5 | 26 | 38 | A8 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ ALT2 | | | CMP0_OUT | |
| 51 | B4 | 27 | 39 | A7 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_MOSI | EXTRG_IN | | SPI0_MISO | | |
| 52 | A4 | 28 | 40 | B6 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_MISO | audioUSB_ SOF_OUT | | SPI0_MOSI | | |
| 53 | — | — | — | A6 | PTC8 | CMP0_IN2 | CMP0_IN2 | PTC8 | I2C0_SCL | TPM0_CH4 | | | | |
| 54 | — | — | — | B5 | PTC9 | CMP0_IN3 | CMP0_IN3 | PTC9 | I2C0_SDA | TPM0_CH5 | | | | |
| 55 | — | — | — | B4 | PTC10 | DISABLED | | PTC10 | I2C1_SCL | | | | | |
| 56 | — | — | — | A5 | PTC11 | DISABLED | | PTC11 | I2C1_SDA | | | | | |
| 57 | — | — | 41 | C3 | PTD0 | DISABLED | | PTD0 | SPI0_PCS0 | | TPM0_CH0 | | FXIO0_D0 | |
| 58 | — | — | 42 | A4 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | | TPM0_CH1 | | FXIO0_D1 | |
| 59 | — | — | 43 | C2 | PTD2 | DISABLED | | PTD2 | SPI0_MOSI | UART2_RX | TPM0_CH2 | SPI0_MISO | FXIO0_D2 | |
| 60 | — | — | 44 | B3 | PTD3 | DISABLED | | PTD3 | SPI0_MISO | UART2_TX | TPM0_CH3 | SPI0_MOSI | FXIO0_D3 | |
| 61 | A3 | 29 | 45 | A3 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI1_PCS0 | UART2_RX | TPM0_CH4 | | FXIO0_D4 | |
| 62 | B3 | 30 | 46 | C1 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI1_SCK | UART2_TX | TPM0_CH5 | | FXIO0_D5 | |
| 63 | B2 | 31 | 47 | B2 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI1_MOSI | LPUART0_ RX | I2C1_SDA | SPI1_MISO | FXIO0_D6 | |
| 64 | A2 | 32 | 48 | A2 | PTD7 | DISABLED | | PTD7 | SPI1_MISO | LPUART0_ TX | I2C1_SCL | SPI1_MOSI | FXIO0_D7 | |

## 4.2 Pin properties

The following table lists the pin properties.

| 64 LQFP | 36 XFBGA | 32 QFN | 48 QFN | 64 MAPBGA | Pin name | Driver strength | Default status after POR | Pullup/ pulldown setting after POR | Slew rate after POR | Passive pin filter after POR | Open drain | Pin interrupt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | C1 | — | — | — | PTE17 | ND | HI-Z | — | FS | N | N | Y |
| — | D1 | — | — | — | PTE18 | ND | Hi-Z | — | FS | N | N | Y |

*Table continues on the next page...*

| 64 LQFP | 36 XFBGA | 32 QFN | 48 QFN | 64 MAPBGA | Pin name | Driver strength | Default status after POR | Pullup/ pulldown setting after POR | Slew rate after POR | Passive pin filter after POR | Open drain | Pin interrupt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 27 | — | — | — | F5 | PTA5 | ND | Hi-Z | — | SS | N | N | Y |
| 28 | — | — | — | H6 | PTA12 | ND | Hi-Z | — | SS | N | N | Y |
| 29 | — | — | — | G6 | PTA13 | ND | Hi-Z | — | SS | N | N | Y |
| 30 | C3 | 15 | 22 | G7 | VDD | ND | — | — | — | — | — | — |
| 31 | C4 | 16 | 23 | H7 | VSS | ND | — | — | — | — | — | — |
| 32 | F6 | 17 | 24 | H8 | PTA18 | ND | Hi-Z | — | SS | N | N | Y |
| 33 | E6 | 18 | 25 | G8 | PTA19 | ND | Hi-Z | — | SS | N | N | Y |
| 34 | D5 | 19 | 26 | F8 | PTA20 | ND | H | PU | SS | N | Y | Y |
| 35 | D6 | 20 | 27 | F7 | PTB0/LLWU_P5 | HD | Hi-Z | — | FS | N | N | Y |
| 36 | C6 | 21 | 28 | F6 | PTB1 | HD | Hi-Z | — | FS | N | N | Y |
| 37 | — | — | 29 | E7 | PTB2 | ND | Hi-Z | — | SS | N | N | Y |
| 38 | — | — | 30 | E8 | PTB3 | ND | Hi-Z | — | SS | N | N | Y |
| 39 | — | — | 31 | E6 | PTB16 | ND | Hi-Z | — | FS | N | N | Y |
| 40 | — | — | 32 | D7 | PTB17 | ND | Hi-Z | — | FS | N | N | Y |
| 41 | — | — | — | D6 | PTB18 | ND | Hi-Z | — | SS | N | N | Y |
| 42 | — | — | — | C7 | PTB19 | ND | Hi-Z | — | SS | N | N | Y |
| 43 | — | — | 33 | D8 | PTC0 | ND | Hi-Z | — | SS | N | N | Y |
| 44 | C5 | 22 | 34 | C6 | PTC1/ LLWU_P6/ RTC_CLKIN | ND | Hi-Z | — | SS | N | N | Y |
| 45 | B6 | 23 | 35 | B7 | PTC2 | ND | Hi-Z | — | SS | N | N | Y |
| 46 | B5 | 24 | 36 | C8 | PTC3/ LLWU_P7 | HD | Hi-Z | — | FS | N | N | Y |
| 47 | — | — | — | E3 | VSS | — | — | — | — | — | — | — |
| 48 | — | — | — | E4 | VDD | — | — | — | — | — | — | — |
| 49 | A6 | 25 | 37 | B8 | PTC4/ LLWU_P8 | HD | Hi-Z | — | FS | N | N | Y |
| 50 | A5 | 26 | 38 | A8 | PTC5/ LLWU_P9 | ND | Hi-Z | — | FS | N | N | Y |
| 51 | B4 | 27 | 39 | A7 | PTC6/ LLWU_P10 | ND | Hi-Z | — | FS | N | N | Y |

*Table continues on the next page...*

**Table 40. Low power mode peripheral adders — typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | • IRC8M (8 MHz internal reference clock)<br>• IRC2M (2 MHz internal reference clock) | 31 | 31 | 31 | 31 | 31 | 31 | |
| $I_{TPM}$ | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.<br>• IRC8M (8 MHz internal reference clock)<br>• IRC2M (2 MHz internal reference clock) | <br><br><br><br><br><br>130<br><br>40 | <br><br><br><br><br><br>130<br><br>40 | <br><br><br><br><br><br>130<br><br>40 | <br><br><br><br><br><br>130<br><br>40 | <br><br><br><br><br><br>130<br><br>40 | <br><br><br><br><br><br>130<br><br>40 | µA |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 320 | 320 | 320 | 320 | 320 | 320 | µA |

#### 5.2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems
- KL-QRUG (Kinetis L-series Quick Reference).

#### 5.2.2.7 Capacitance attributes

**Table 41. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | — | 7 | pF |

## 5.2.3 Switching specifications

### 5.2.3.1 Device clock specifications

**Table 42. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| Normal run mode | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 24 | MHz |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz |
| $f_{SYS\_USB}$ | System and core clock when Full Speed USB in operation | 20 | — | MHz |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes[1] | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 1 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 24 | MHz |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| $f_{TPM}$ | TPM asynchronous clock | — | 8 | MHz |
| $f_{UART0}$ | UART0 asynchronous clock | — | 8 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

#### 5.2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 43. General switching specifications**

| Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

### 5.2.4 Thermal specifications

#### 5.2.4.1 Thermal operating requirements

**Table 44. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C | |
| $T_A$ | Ambient temperature | –40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed the maximum. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

#### 5.2.4.2 Thermal attributes

**NOTE**

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

**Table 45. Thermal attributes**

| Board type | Symbol | Description | 32 QFN | 36 XFBGA | 64 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 101 | 81.5 | 71 | °C/W | 1, 2, 3 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 33 | 54.7 | 53 | °C/W | 1, 2, 3,4 |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 84 | 71.3 | 60 | °C/W | 1, 4, 5 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 28 | 50.0 | 47 | °C/W | 1, 4, 5 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 13 | 58.0 | 35 | °C/W | 6 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 1.7 | 45.3 | 21 | °C/W | 7 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 1.2 | 5 | °C/W | 8 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom (natural convection) | - | 44.5 | - | °C/W | 9 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
6. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
7. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
8. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
9. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

## 5.3 Peripheral operating requirements and behaviors

### 5.3.1 Core modules

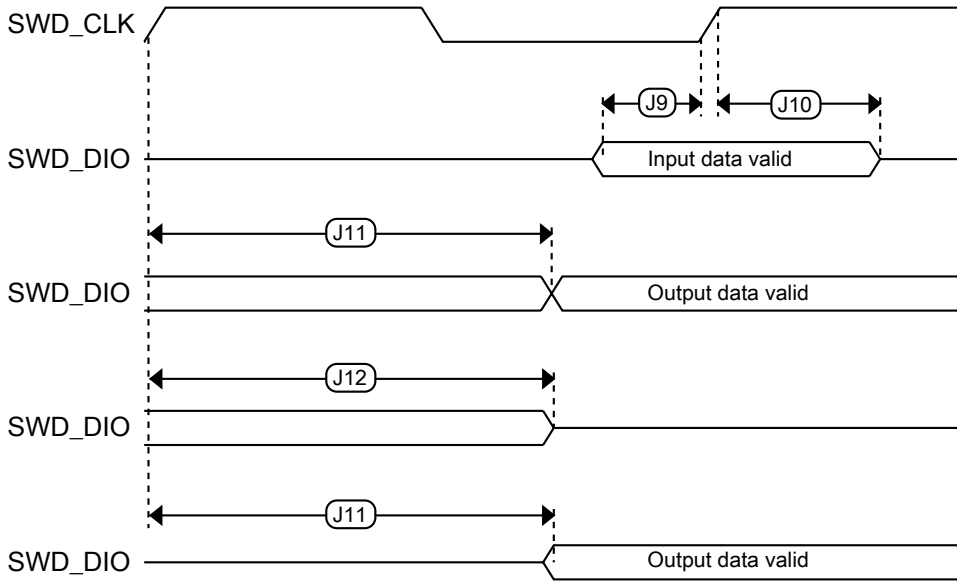



**Figure 23. Serial wire data timing**

## 5.3.2 System modules

There are no specifications necessary for the device's system modules.

## 5.3.3 Clock modules

### 5.3.3.1 MCG-Lite specifications

**Table 47. IRC48M specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD48M}$ | Supply current | — | 400 | 500 | µA | |
| $f_{irc48m}$ | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m\_ol\_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | 1 |
| $\Delta f_{irc48m\_cl}$ | Closed loop total deviation of IRC48M frequency over voltage and temperature | — | — | ± 0.1 | $\%f_{host}$ | 2 |

*Table continues on the next page...*

**Table 47. IRC48M specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $J_{cyc\_irc48m}$ | Period Jitter (RMS) | — | 35 | 150 | ps | |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | µs | 3 |

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean±3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. See reference manual for details.

**Table 48. IRC8M/2M specification**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_2M}$ | Supply current in 2 MHz mode | — | 14 | 17 | µA | — |
| $I_{DD\_8M}$ | Supply current in 8 MHz mode | — | 30 | 35 | µA | — |
| $f_{IRC\_2M}$ | Output frequency | — | 2 | — | MHz | — |
| $f_{IRC\_8M}$ | Output frequency | — | 8 | — | MHz | — |
| $f_{IRC\_T\_2M}$ | Output frequency range (trimmed) | — | — | ±3 | $\%f_{IRC}$ | — |
| $f_{IRC\_T\_8M}$ | Output frequency range (trimmed) | — | — | ±3 | $\%f_{IRC}$ | — |
| $T_{su\_2M}$ | Startup time | — | — | 12.5 | µs | — |
| $T_{su\_8M}$ | Startup time | — | — | 12.5 | µs | — |

## 5.3.3.2 Oscillator electrical specifications

### 5.3.3.2.1 Oscillator DC electrical specifications

**Table 49. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |

*Table continues on the next page...*

**Table 51. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

#### 5.3.4.1.2 Flash timing specifications — commands

**Table 52. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | — |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 0.9 | ms | 1 |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | — |
| $t_{ersall}$ | Erase All Blocks execution time | — | 70 | 575 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |
| $t_{ersallu}$ | Erase All Blocks Unsecure execution time | — | 70 | 575 | ms | 2 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

#### 5.3.4.1.3 Flash high voltage current behaviors

**Table 53. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

#### 5.3.4.1.4 Reliability specifications

**Table 54. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Program Flash | | | | | | |

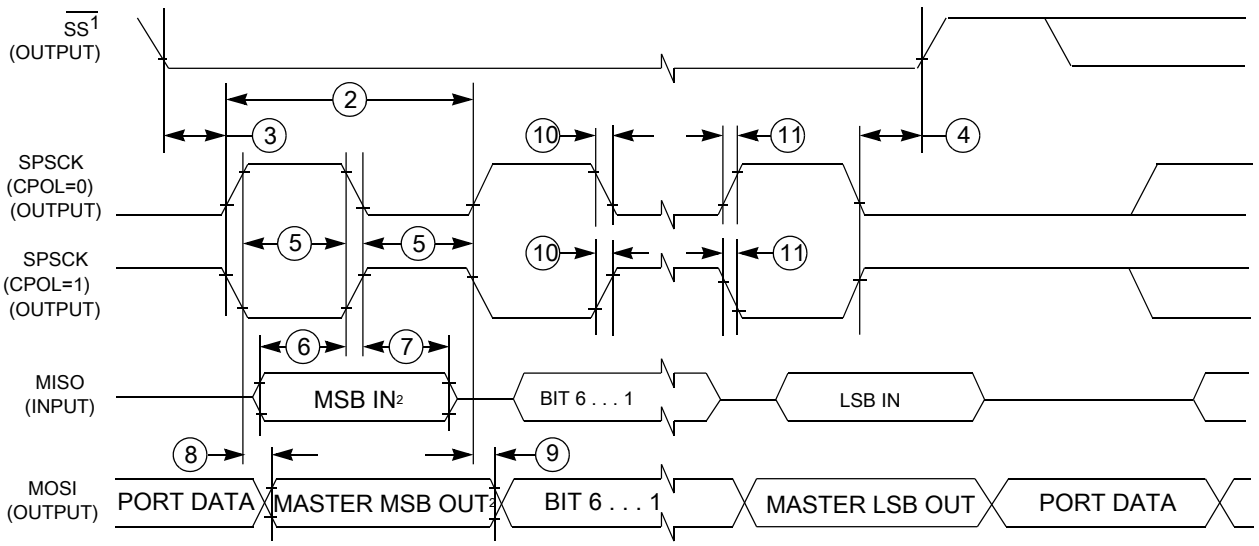
*Table continues on the next page...*

### 5.3.6.2 CMP and 6-bit DAC electrical specifications

**Table 60. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 30. SPI master mode timing (CPHA = 1)**

## Table 63. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

## Table 64. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 7 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 36 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

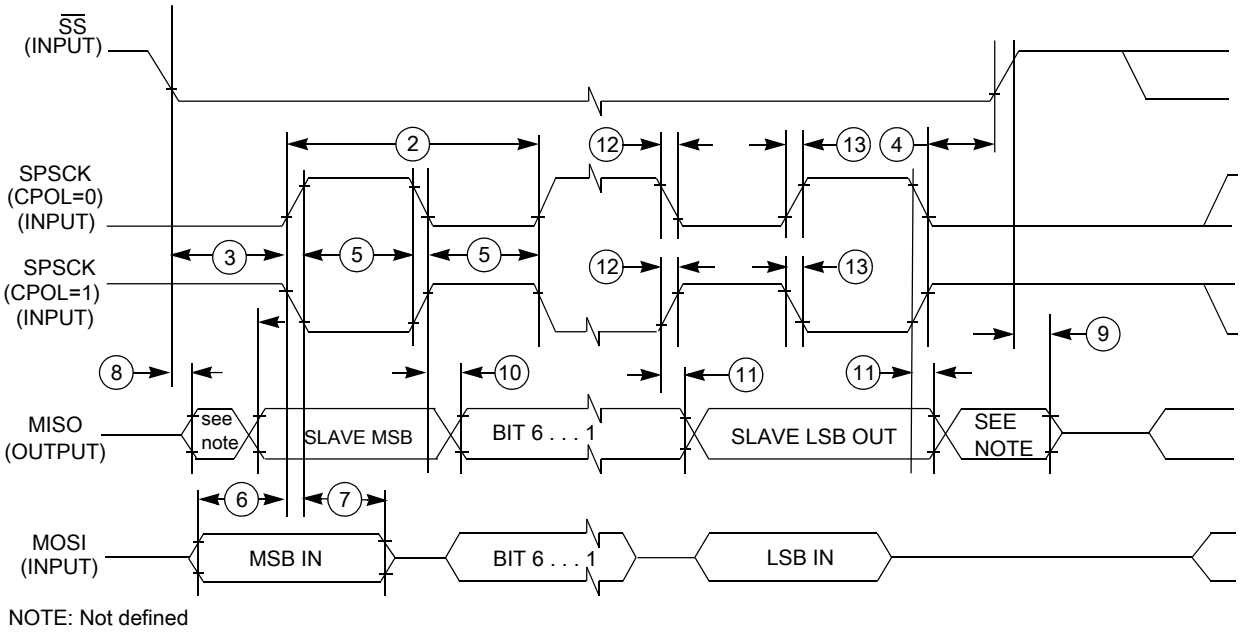
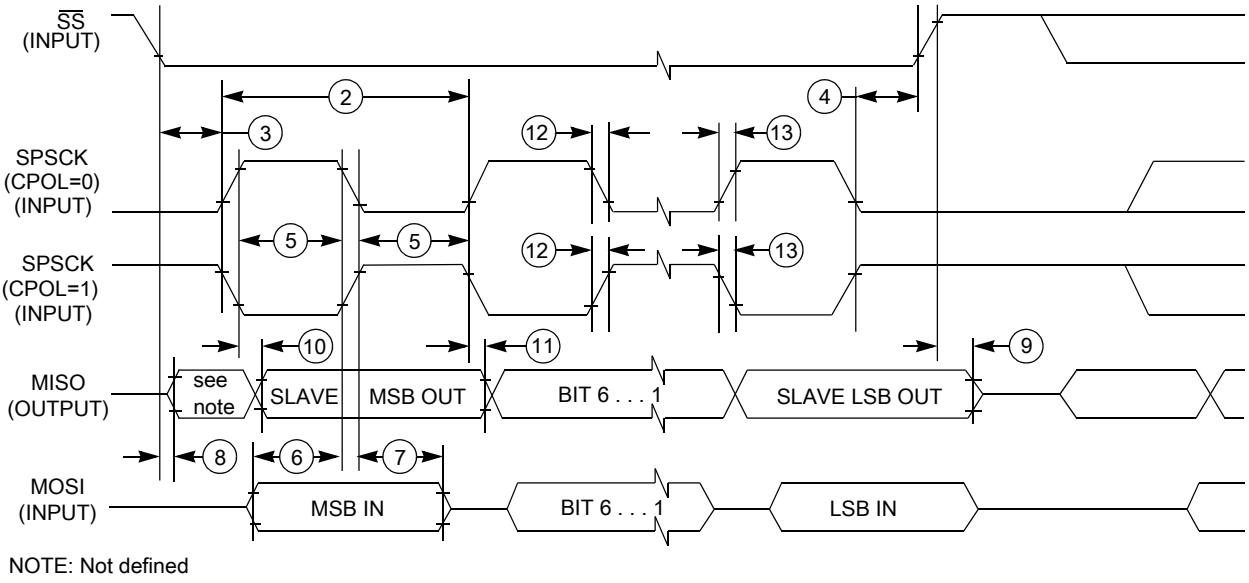



**Figure 31. SPI slave mode timing (CPHA = 0)**




NOTE: Not defined

**Figure 32. SPI slave mode timing (CPHA = 1)**

## 5.5.3 Inter-Integrated Circuit Interface (I2C) timing

**Table 65. I2C timing**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400[1] | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 4 | — | 0.6 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | — | 1.25 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 4.7 | — | 0.6 | — | µs |
| Data hold time for $I^2C$ bus devices | $t_{HD}$; DAT | 0[2] | 3.45[3] | 0[4] | 0.9[2] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[5] | — | 100[3, 6] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[7] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[6] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.

If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

### 6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2MHz does not require any series resistance.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

**Table 67. External crystal/resonator connections**

| Oscillator mode | Oscillator mode |
|---|---|
| Low frequency (32.768kHz), low power | Diagram 1 |
| Low frequency (32.768kHz), high gain | Diagram 2, Diagram 4 |
| High frequency (1-32MHz), low power | Diagram 3 |
| High frequency (1-32MHz), high gain | Diagram 4 |

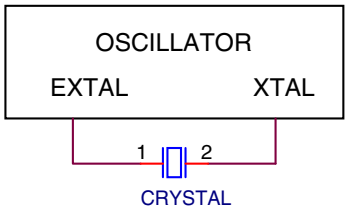



**Figure 40. Crystal connection – Diagram 1**

## Table 69. Revision history (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • Updated the features and completed the ordering information.<br>• Updated Table 9 - Power consumption operating behaviors with Max. values.<br>• Added a note before Table 9.<br>• Updated Table 17 - IRC48M specifications.<br>• Updated Table 28. VREF full-range (-40 – 105 °C) operating behaviors with Min., Max., and Typical values.<br>• Added section 5.1 - USB electrical specifications.<br>• Added Table 36 - $I^2C$ 1Mbit/s timing. |
| 4.1 | 2 February/ 2015 | • Moved the ordering information out of the front page to be a separate chapter.<br>• Added Module signal description table and Package dimension sections. |
| 5 | 21 April/2015 | • 32-pin QFN package is now standard part, added Marking information and thermal attributes of this package<br>• Added Overview chapter<br>• Added Memory map chapter<br>• Added Pin properties<br>• Added a note to the $t_{rd1all}$ in Flash timing specifications — commands<br>• Added a note to the Maximum of $f_{SCL}$ in the fast mode in Inter-Integrated Circuit Interface (I2C) timing<br>• Added a footnote to the Δfirc48m_ol_hv in MCG-Lite specifications<br>• Added Design considerations chapter |