NXP USA Inc. - MKL27Z32VLH4 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, FlexIO, SPI, UART/USART, USB
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x16b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl27z32vlh4

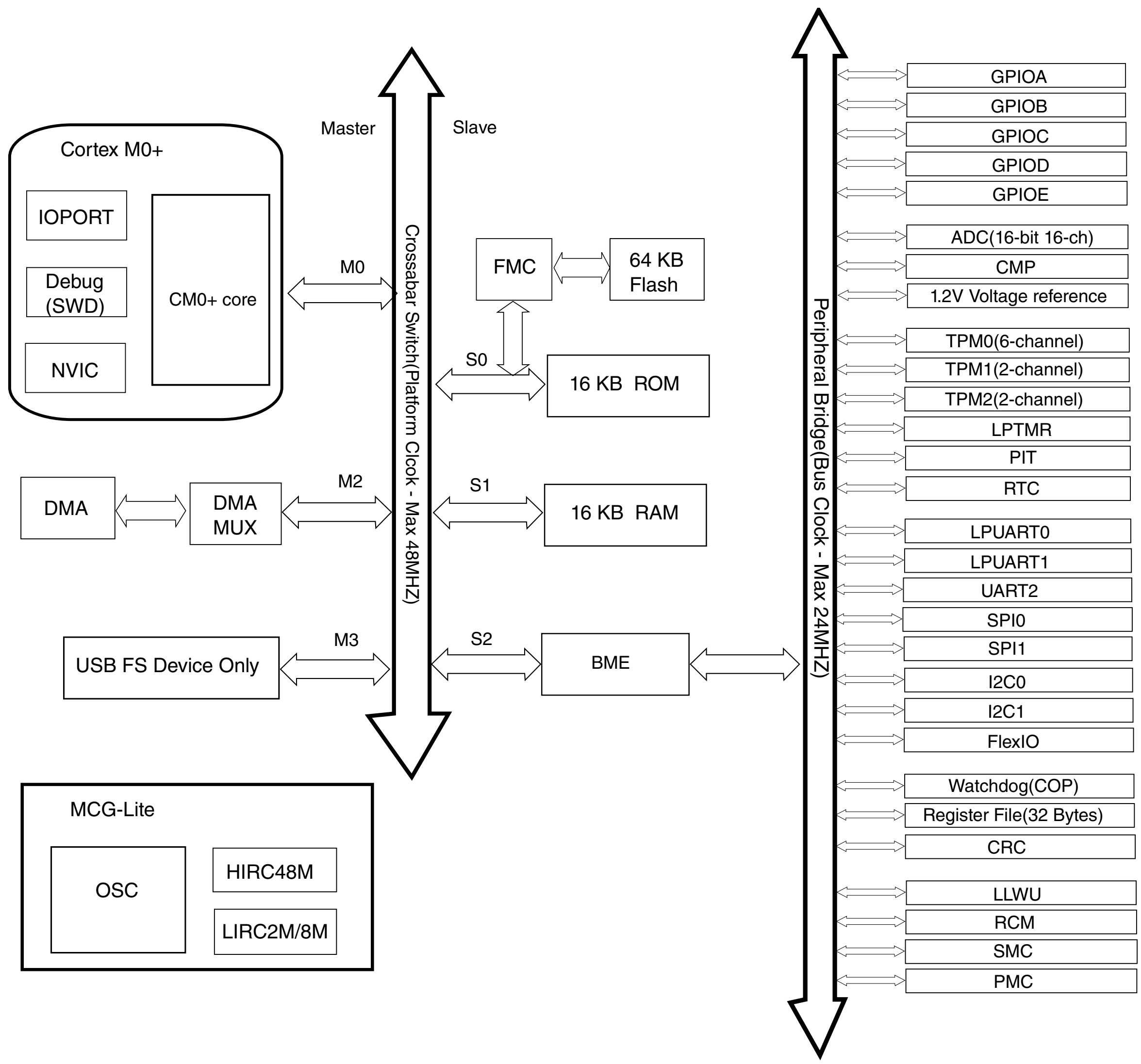


Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

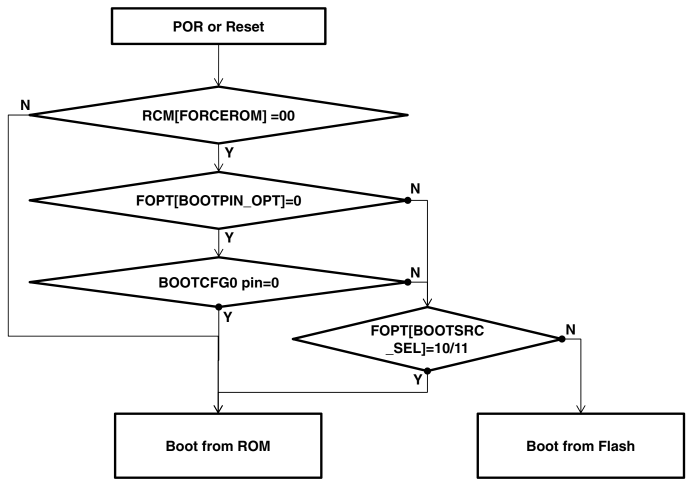


Figure 2. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.1.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, and ceramic resonators. These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the high-speed internal resister capacitor (HIRC) oscillator, the low-speed internal resister capacitor (LIRC) oscillator, and the low power oscillator (LPO).

The HIRC oscillator generates a 48 MHz clock and synchronizes with the USB clock in full speed mode to achieve the required accuracy.

The LIRC oscillator generates an 8 MHz or 2 MHz clock, and default to 8 MHz system clock on reset. The LIRC oscillator cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
I^2C1	System Clock	—	I2C1_SCL
LPUART0, LPUART1	Bus clock	LPUART0 clock LPUART1 clock	—
UART2	Bus clock	—	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM’s operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM’s operational modes, See the ARM® Cortex User Guide.

- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-Calibration mode

2.2.4.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see Table 56 for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031. We recommend to use internal reference voltage as ADC reference with long sample time.

2.2.5 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC or CMP.

The VREF supports the following programmable buffer modes:

- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

The VREF voltage output signal, bonded on VREFH for 48 QFN, 64 LQFP and 64 MAPBGA packages and on PTE30 for 32 QFN and 36 XFBGA packages, can be used by both internal and external peripherals in low and high power buffer mode. A 100 nF capacitor must always be connected between this pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has two independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
    - Optional interrupt can generate asynchronous wakeup from any low-power mode
    - Hardware trigger output
    - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

- 1/16 bit-time noise detection
- DMA interface

2.2.12 LPUART

This product contains two Low-Power UART modules, both of their clock sources are selectable from IRC48M, IRC8M/2M or external crystal clock, and can work in Stop and VLPS modes. They also support 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.13 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	C1	—	—	—	PTE17	ADC0_DM1/ ADC0_SE5a	ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_ CLKIN1	LPTMR0_ ALT3	FXIO0_D1	
—	D1	—	—	—	PTE18	ADC0_DP2/ ADC0_SE2	ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO	FXIO0_D2	
—	F2	9	—	—	VREF0	VREF0_B	VREF0_B							
—	—	—	—	C5	NC	NC	NC							
1	A1	1	—	A1	PTE0	DISABLED		PTE0/ CLKOUT32 K	SPI1_MISO	LPUART1_ TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	
2	—	—	—	B1	PTE1	DISABLED		PTE1	SPI1_MOSI	LPUART1_ RX		SPI1_MISO	I2C1_SCL	
3	—	—	1	—	VDD	VDD	VDD							
4	C4	2	2	C4	VSS	VSS	VSS							
5	B1	3	3	E1	USB0_DP	USB0_DP	USB0_DP							
6	D2	4	4	D1	USB0_DM	USB0_DM	USB0_DM							
7	C3	5	5	E2	USB_VDD	USB_VDD	USB_VDD							
8	C2	6	6	D2	PTE16	ADC0_DP1/ ADC0_SE1	ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_ CLKIN0		FXIO0_D0	
9	E3	—	7	G1	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_ TX		FXIO0_D4	
10	E2	—	8	F1	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_ RX		FXIO0_D5	
11	E1	—	—	G2	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
12	F1	—	—	F2	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
13	D3	7	9	F4	VDDA	VDDA	VDDA							
14	D3	7	10	G4	VREFH	VREFH	VREFH							
14	—	—	10	G4	VREFO	VREFO_A	VREFO_A							
15	D4	8	11	G3	VREFL	VREFL	VREFL							
16	D4	8	12	F3	VSSA	VSSA	VSSA							
17	—	—	13	H1	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_ CLKIN0			
18	F2	9	14	H2	PTE30	ADC0_ SE23/ CMP0_IN4	ADC0_ SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_ CLKIN1	LPUART1_ TX	LPTMR0_ ALT1	
19	—	—	—	H3	PTE31	DISABLED		PTE31		TPM0_CH4				

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
50	A5	26	38	A8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	
51	B4	27	39	A7	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
52	A4	28	40	B6	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT		SPI0_MOSI		
53	—	—	—	A6	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
54	—	—	—	B5	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
55	—	—	—	B4	PTC10	DISABLED		PTC10	I2C1_SCL					
56	—	—	—	A5	PTC11	DISABLED		PTC11	I2C1_SDA					
57	—	—	41	C3	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
58	—	—	42	A4	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
59	—	—	43	C2	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
60	—	—	44	B3	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
61	A3	29	45	A3	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
62	B3	30	46	C1	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
63	B2	31	47	B2	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_ RX	I2C1_SDA	SPI1_MISO	FXIO0_D6	
64	A2	32	48	A2	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_ TX	I2C1_SCL	SPI1_MOSI	FXIO0_D7	

4.2 Pin properties

The following table lists the pin properties.

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
—	C1	—	—	—	PTE17	ND	HI-Z	—	FS	N	N	Y
—	D1	—	—	—	PTE18	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

NOTE

The 48 QFN package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

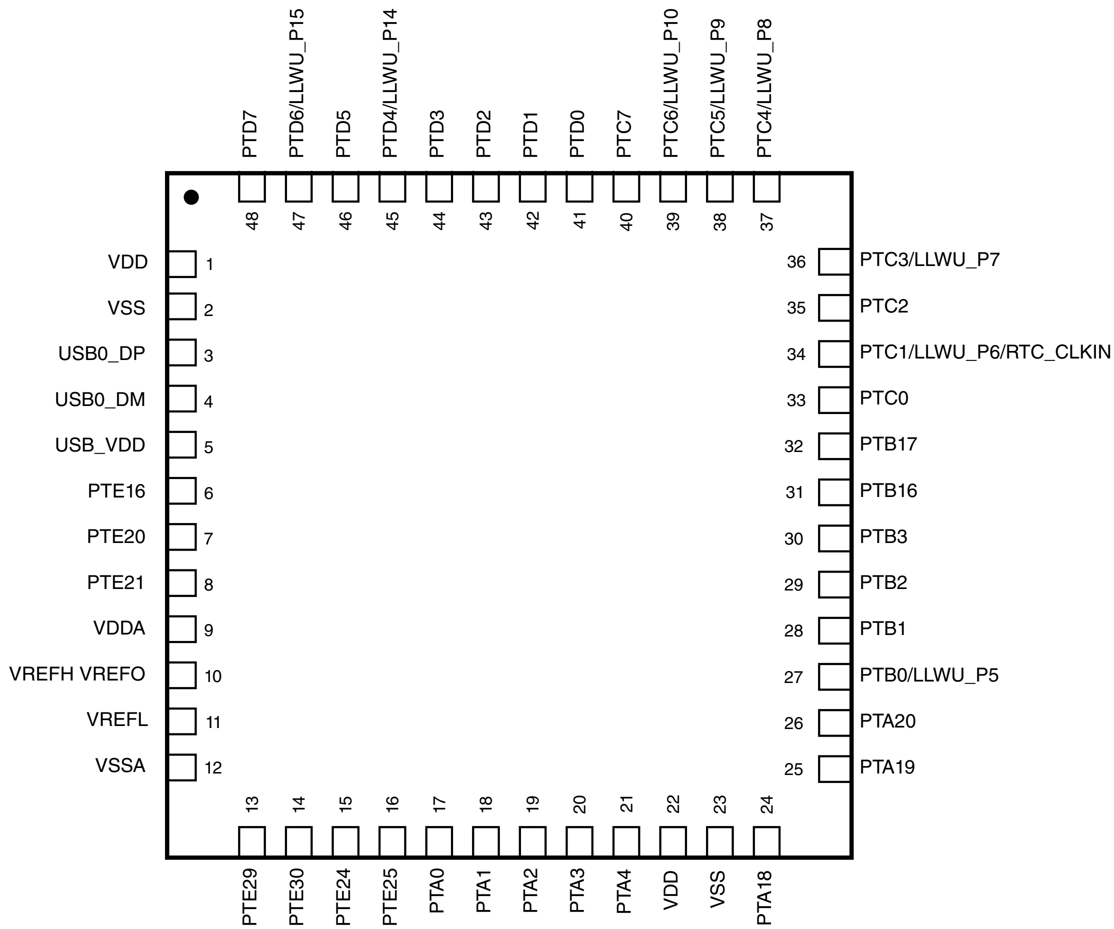


Figure 7. 48 QFN Pinout diagram (transparent top view)

The figure below shows the 64 MAPBGA pinouts.

NOTE

The 64 MAPBGA package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	NC	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	USB0_DM	PTE16	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	USB_VDD	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH VREFO	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 8. 64 MAPBGA Pinout diagram (transparent top view)

The figure below shows the 64 LQFP pinouts:

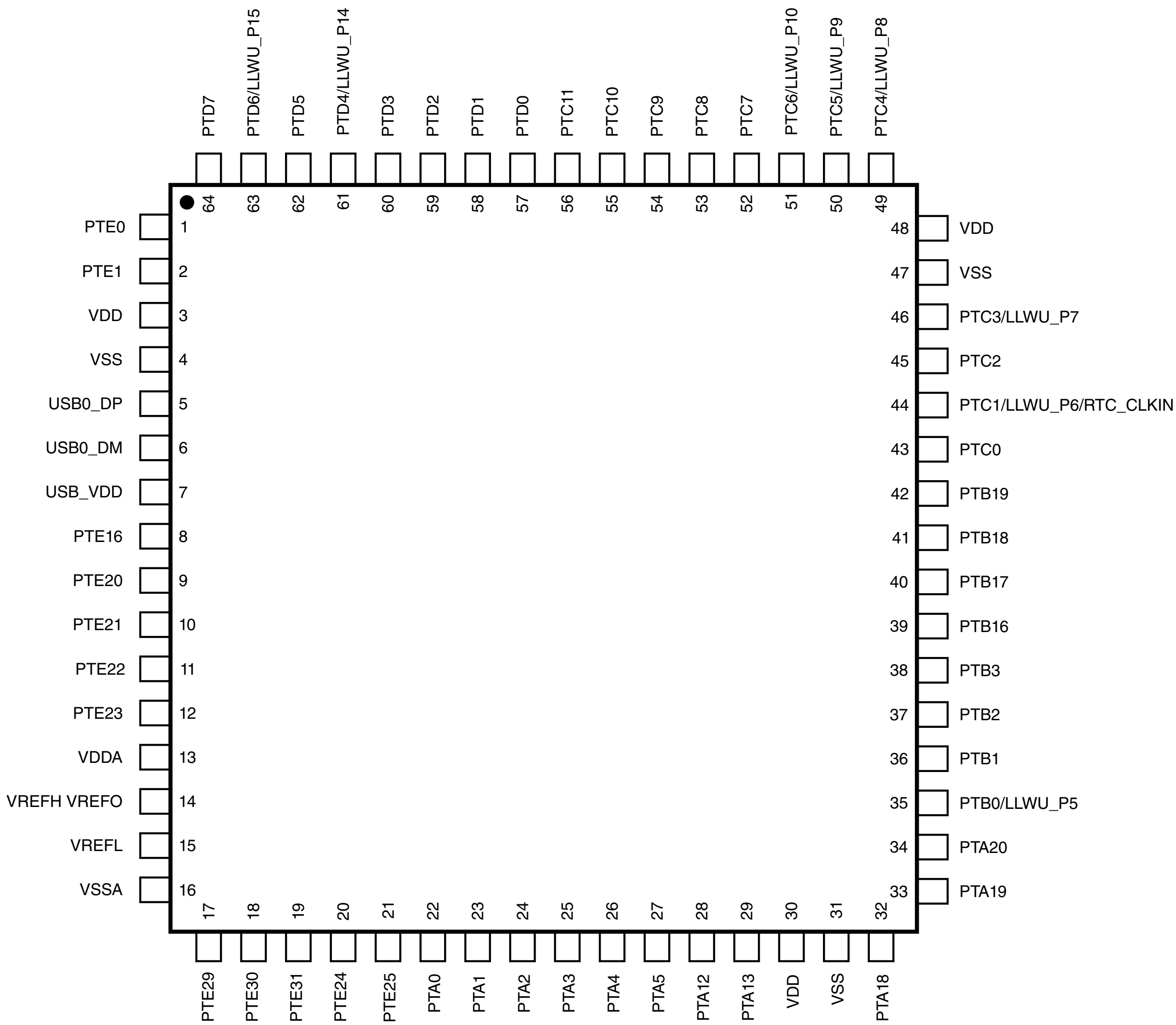
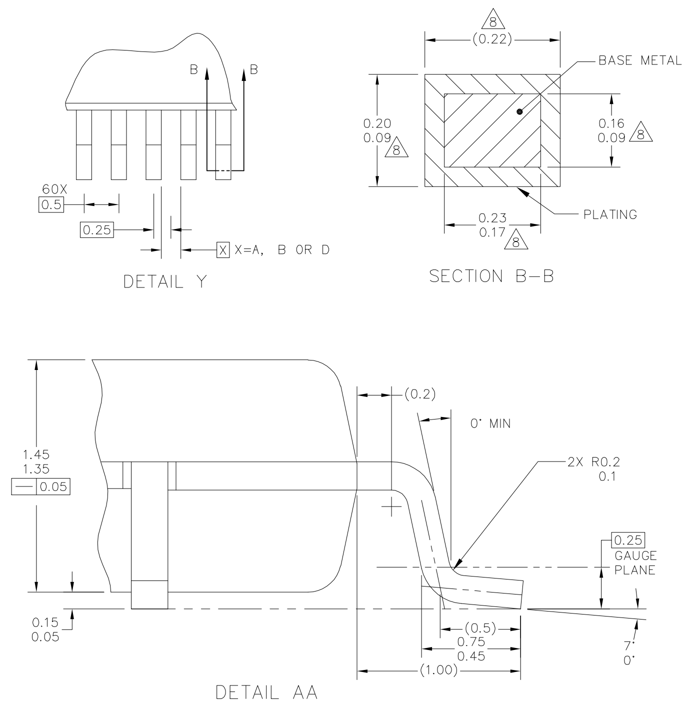


Figure 9. 64 LQFP Pinout diagram (top view)

The figure below shows the 36 XFBGA pinouts:



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

Table 39. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	91	136.5	µA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	34	51	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	212	318	µA	
I_{DD_VLPR}	Very-low-power run mode current—8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	302	392.6	µA	
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V • at 25 °C	—	1.81	2.12	mA	
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V • at 25 °C	—	1.27	1.46	mA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V • at 25 °C	—	156	193.2	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V • at 25 °C	—	63	100.8	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V • at 25 °C	—	32	48	µA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V • at 25 °C	—	1.68	2.05	mA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V • at 25 °C					

Table continues on the next page...

Table 39. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.43 2.06 3.51 5.91 13.36	 1.58 2.52 5.20 7.60 17.08	μA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.83 2.47 3.96 6.44 13.84	 1.98 2.93 5.65 8.13 17.56	μA	3
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.68 2.27 3.66 5.97 12.92	 1.83 2.73 5.35 7.66 16.64	μA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 0.84 1.19 2.03 3.54 8.53	 1.06 1.33 2.62 4.13 9.98	μA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 1.26 1.61 2.5 4.07 9	 1.48 1.75 3.09 4.66 10.45	μA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below	 — —	 1.08 1.42	 1.30 1.56		3

Table continues on the next page...

Table 55. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

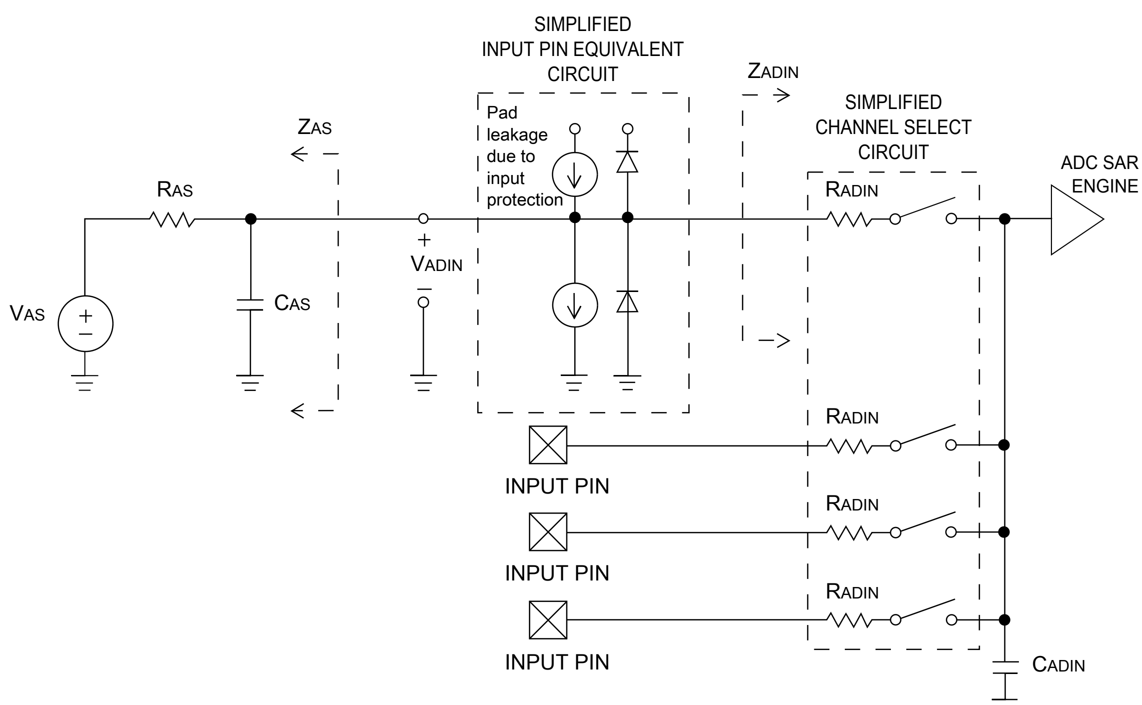


Figure 24. ADC input impedance equivalency diagram

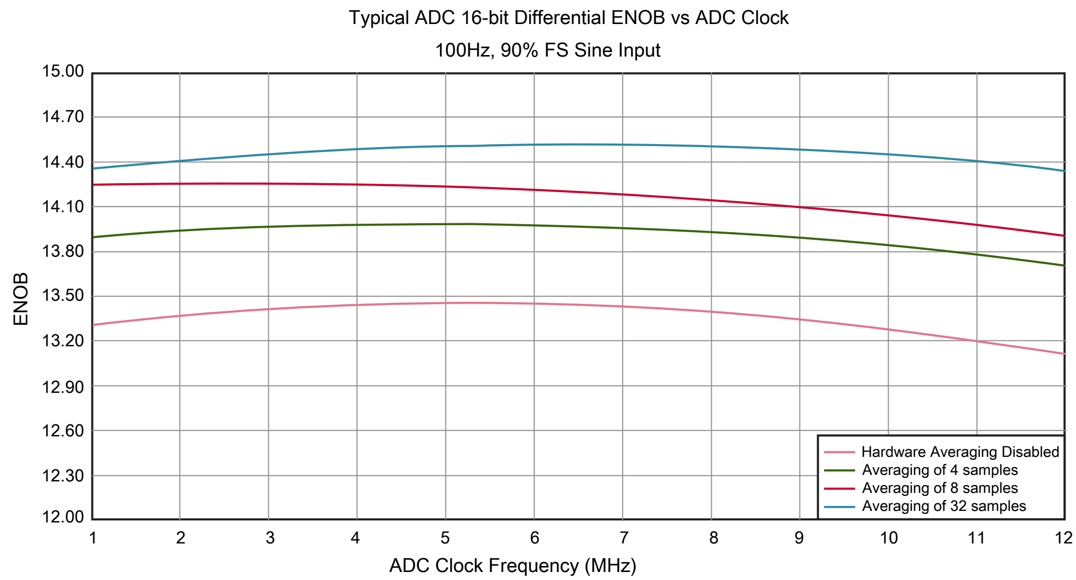


Figure 25. Typical ENOB vs. ADC_CLK for 16-bit differential mode

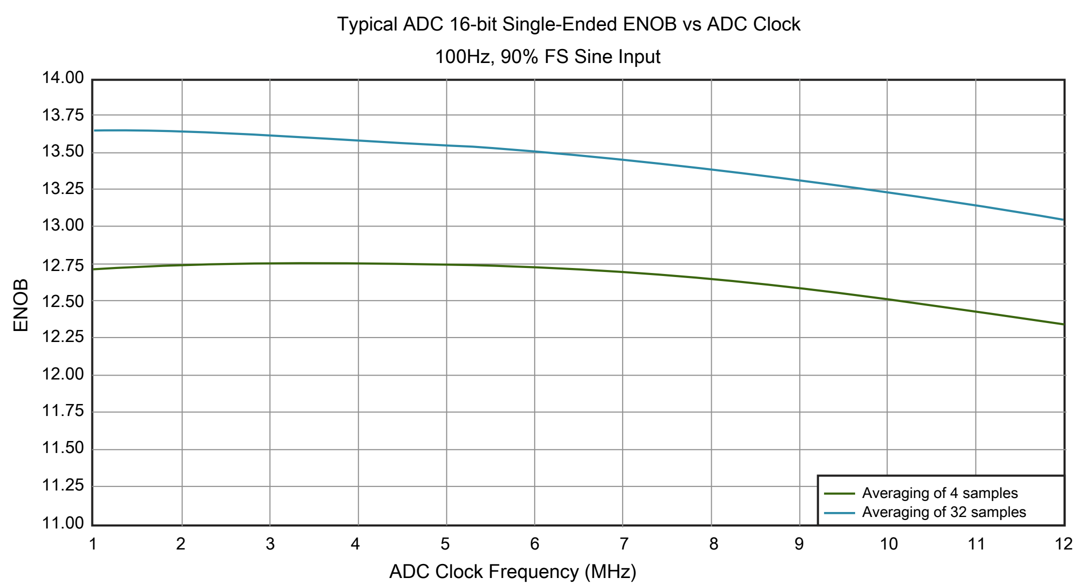


Figure 26. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.3.6.1.3 Voltage reference electrical specifications

Table 57. VREF full-range operating requirements

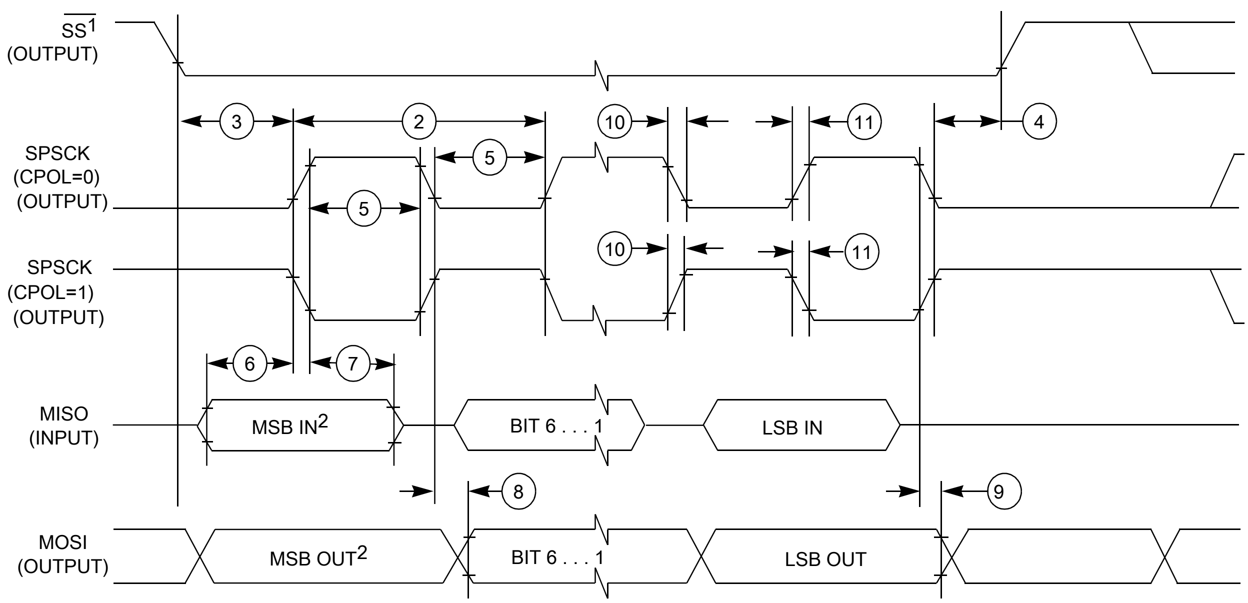
Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	

Table continues on the next page...

Table 62. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 29. SPI master mode timing (CPHA = 0)

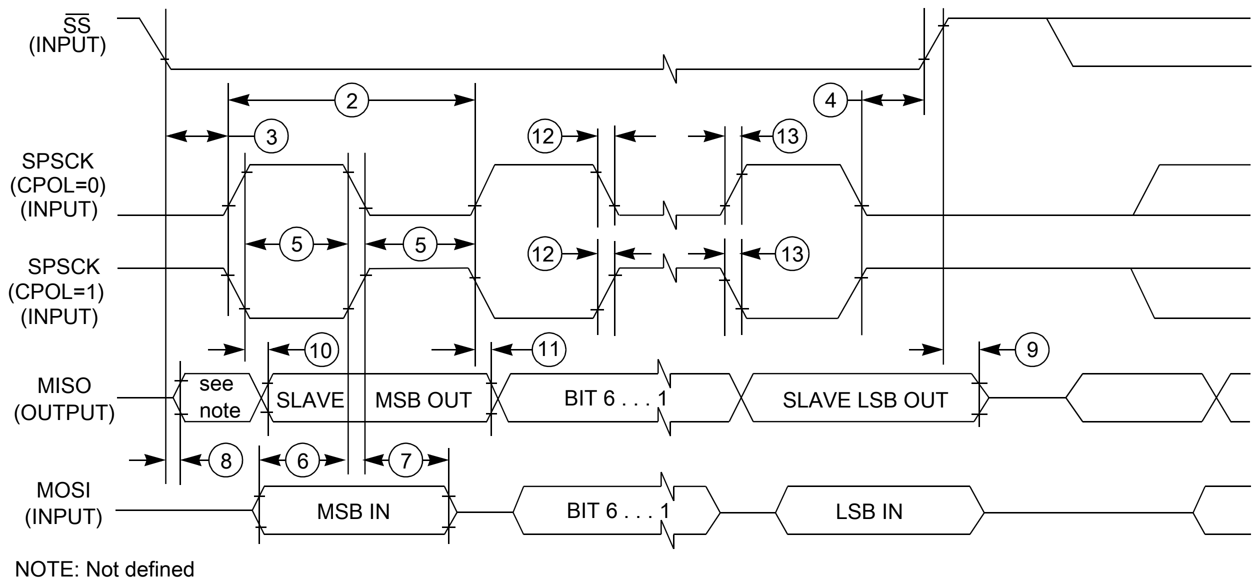


Figure 32. SPI slave mode timing (CPHA = 1)

5.5.3 Inter-Integrated Circuit Interface (I2C) timing

Table 65. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.

If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2MHz does not require any series resistance.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

Table 67. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768kHz), low power	Diagram 1
Low frequency (32.768kHz), high gain	Diagram 2, Diagram 4
High frequency (1-32MHz), low power	Diagram 3
High frequency (1-32MHz), high gain	Diagram 4

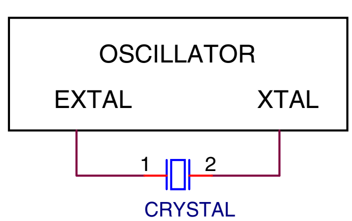


Figure 40. Crystal connection – Diagram 1

- Freescale Freedom Development Platform: http://www.freescale.com/freedom
- Tower System Development Platform: http://www.freescale.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Development Tools

- PEG Graphics Software: http://www.freescale.com/peg
- Processor Expert Software and Embedded Components: http://www.freescale.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed
- MQX RTOS: http://www.freescale.com/mqx

For all other partner-developed software and tools, visit http://www.freescale.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N