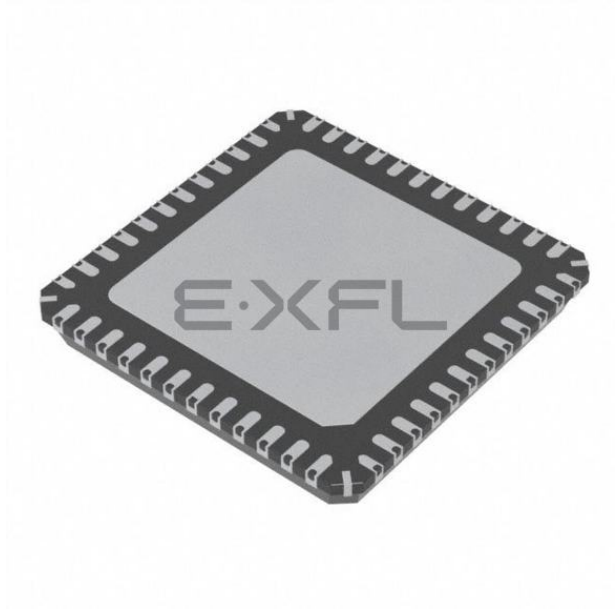

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle98322qxxuma1

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832-2 device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9832-2QV	40 MHz	2	5	36 kByte	11	no
TLE9832-2QX	40 MHz	2	5	36 kByte	11	no

Table 2 Acronyms

Acronyms	Name
ROM	Read Only Memory
SCK	SSC Clock
SFR	Special Function Register
SOW	Short Open Window (for WDT1)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
SSU	System Status Unit
TMS	Test Mode Select
UART	Universal Asynchronous Receiver Transmitter
UDIG	Universal Digital Controller for ADC1
VBG	Voltage reference Band Gap
WDT	Watchdog timer
WMU	Wake-up Management Unit
XRAM	On-Chip eXternal Data Memory
XSFR	On-Chip eXternal Special Function Register

Table 4 Power mode configurations

Module/function	Active Mode	Stop Mode	Sleep Mode	Comment
CYCLIC Modes	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ cyclic sense/OFF	cyclic sense with HS, VDDEXT; wake-up from cyclic wake needs MC for entering Sleep Mode / Stop Mode again
Measurement Unit	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/HALT	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (20 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON	ON	ON	for cyclic wake-up

1) Cannot not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, the LIN and MON inputs are activated after power-on reset only. GPIO ports as wake-up sources are disabled by default after power-on reset. The application software can reconfigure the wake-up sources according to the application needs.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor and GPIO input individually.

Table 5 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent Supply Voltage Generation for PMU	This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC).
LP_CLK (= 20 MHz)	- Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1
LP_CLK2 (= 100 kHz)	Clock Source for PMU	This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features
VDDEXT (Hall Sensor Supply)	Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor)
PMU-XSFR	All PMU relevant Extended Special Function Registers	This module contains all PMU relevant registers, which are needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module.
PMU-WMU	Wake-up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CYCMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions within cyclic mode.
PMU-CMU	Clock Management Unit of the PMU	This block is responsible for controlling all clocking actions within the PMU.
PMU-RMU	Reset Management Unit of the PMU	This block is responsible for generating all system required resets.

3.5 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 1.5V supply (VDDC) from the internal voltage regulator and does not require additional programming or erasing voltage.

Features

- In-System Programming via LIN (Flash mode) and DAP
- Error Correction Code (ECC) for dynamic correction of single Bit errors and signalling for double Bit failures
- Support for aborting erase operation
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- 4 Byte read access
- Read access time: 75 ns
- Program time for 1 page: 3 ms
- Page erase time: 4 ms

3.6 Watchdog Timer 1 (WDT1)

Features

- Windowed Watchdog Timer with programmable timing in Active Mode
- Long open window (80ms) after power-up, reset, wake-up
- Short open window (30ms) to facilitate Flash programming
- Disabled during debugging
- Safety shutdown to Sleep Mode after 5 missed WDT1 services

There are two watchdog timers in the system. The Watchdog Timer (WDT) within the microcontroller (see **Chapter 3.7**) and the Watchdog Timer 1 (WDT1), which is described in this section.

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and OCDS mode the WDT1 is disabled.

The behavior of the Watchdog Timer 1 in Active Mode is depicted in **Figure 12**.

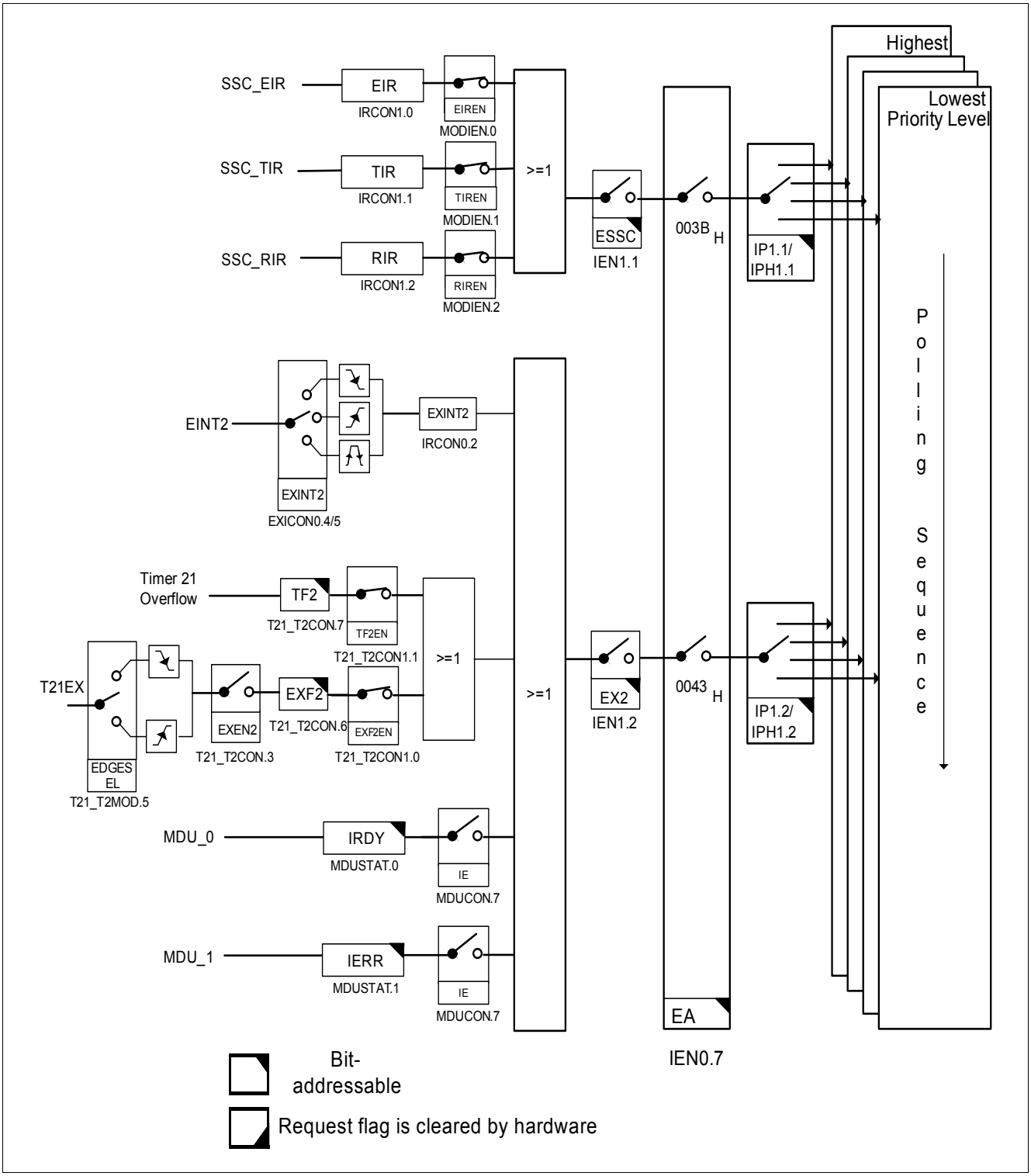

Figure 16 Interrupt Request Sources (Part 3)

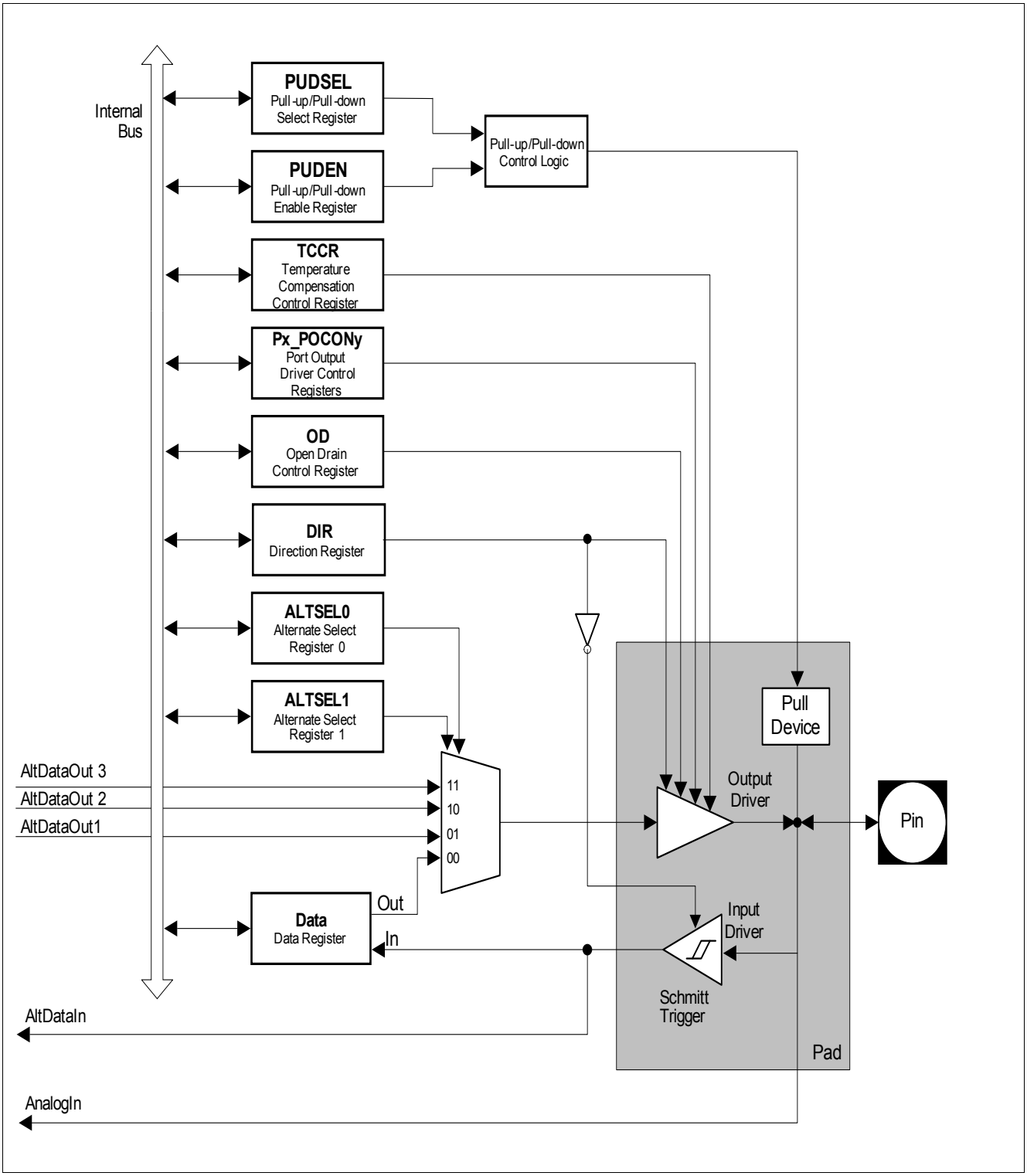

Figure 20 General Structure of a Bidirectional Port Pin

Figure 21 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via register. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. The analog input (Analog In) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC1 input channel.

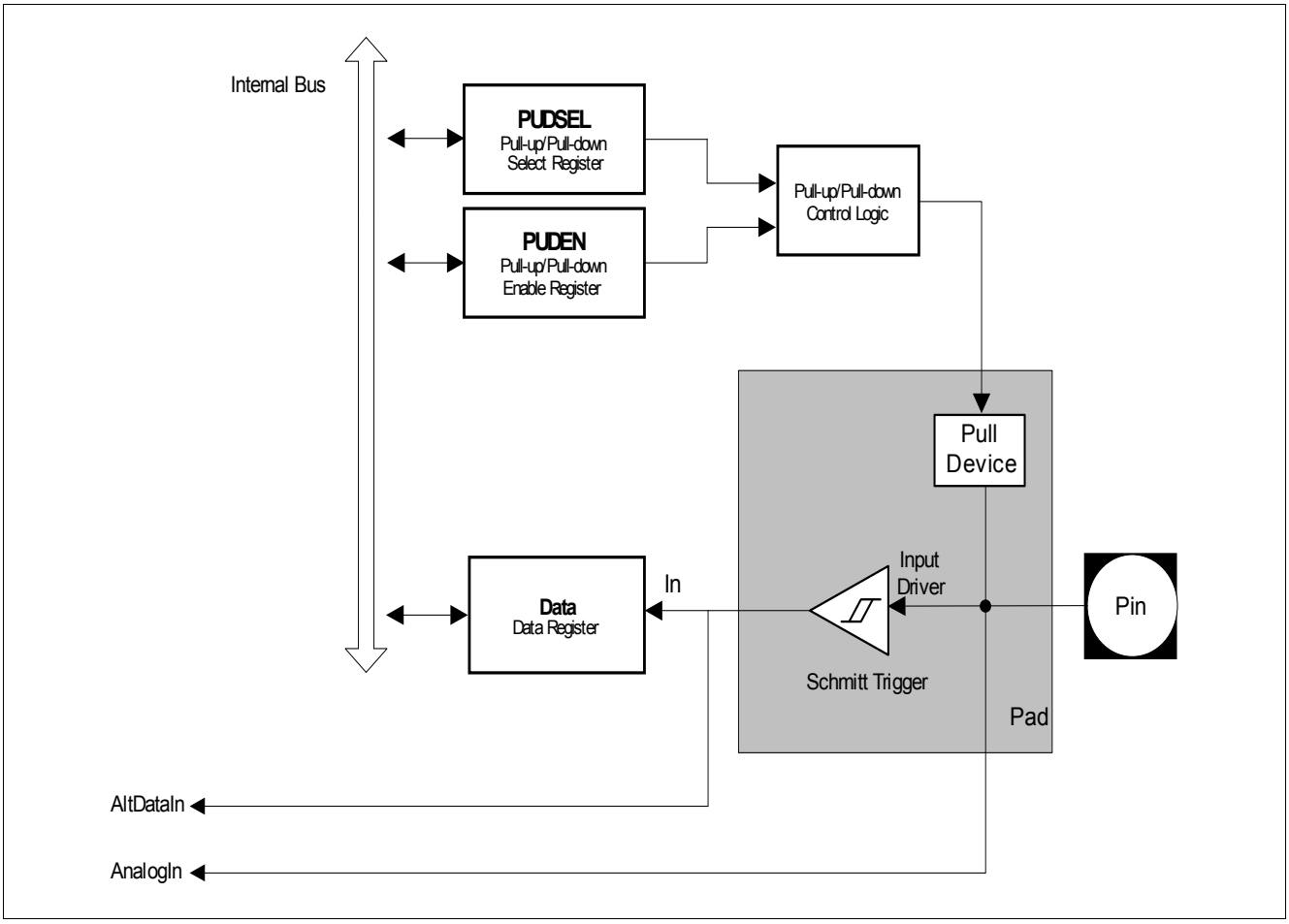

Figure 21 General Structure of an Input Port Pin

3.13 Timer 3

Timer 3 can function as timer or counter. When functioning as a timer, Timer 3 is incremented in periods based on the system clock. When functioning as a counter, Timer 3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer 3 can be configured in four different operating modes to use in a variety of applications, see **Table 8**.

Table 8 Timer 3 Modes

Mode	Sub-Mode	Operation
0	**-**	**13-Bit Timer** The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**a**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter.
1	**b**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable a single shot measurement on a preset channel with the measurement unit.
1	**c**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable the LIN Baudrate Measurement.
2	**-**	**8-Bit Timer with Auto-reload** The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow.
3	**a**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters.
3	**b**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters. In this mode the 100 kHz Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as an counter which counts the time between the edges.

3.16 LIN Transceiver

The LIN module is a transceiver for the Local Interconnect Network (LIN) compliant to the standards LIN 1.3, LIN 2.0 and LIN 2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kbps and 20 kbps. Additionally baud rates up to 40 kBaud are implemented.

The LIN module offers several different operation modes, including a Sleep Mode and the normal operation mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kBaud is also implemented.

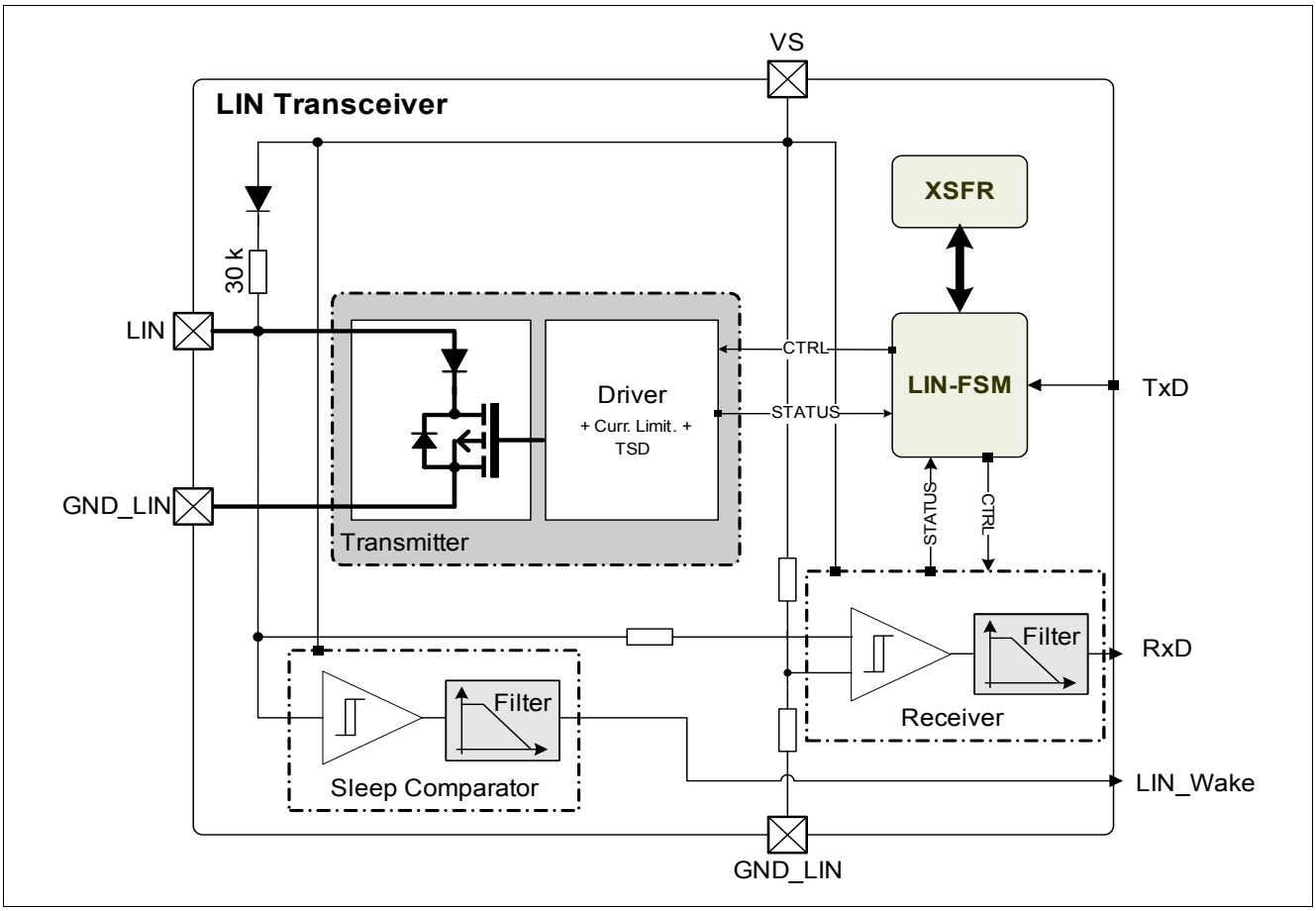

Figure 23 LIN Transceiver Block Diagram

3.17 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format

3.24 PWM Generator

The PWM generator provides up to two configurable PWM channels in order to drive the Low Side Switches LS1, LS2 and the High Side Switches HS1 and HS2 in a PWM mode.

Features

- Programmable modulation frequency per channel
- Programmable duty-cycle per channel with glitch-free reprogramming
- PWM frequency up to 25 kHz
- Duty-cycle resolution from 0 % ... 100 % in steps of 0.5 %

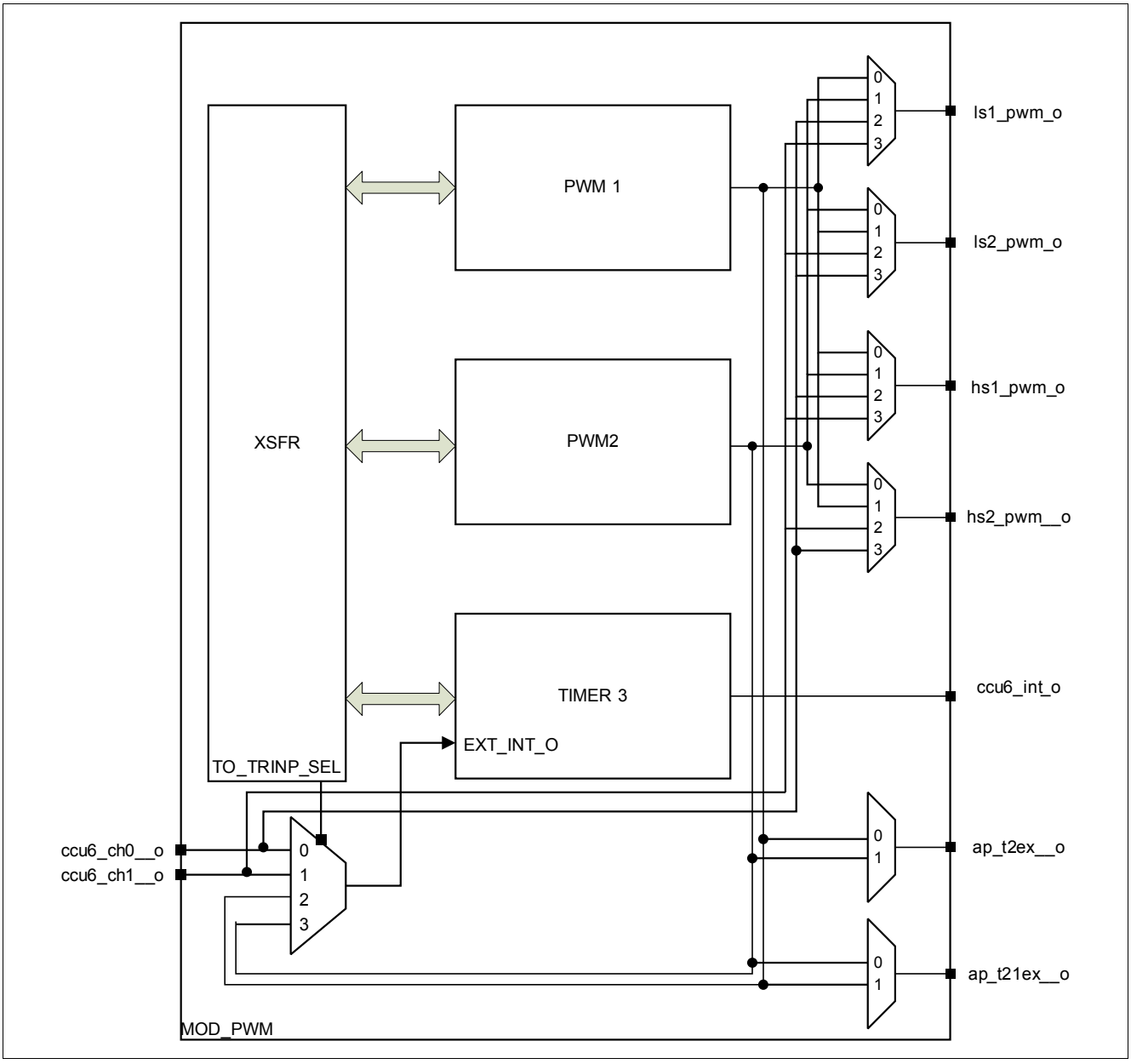

Figure 30 Module Block diagram of PWM module and included PWM switching matrix

5 Electrical Characteristics

This chapter includes all relevant Electrical Characteristics of the product TLE9832-2.

5.1 General Characteristics

5.1.1 Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings [1)]

T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages Supply Pins							
Supply voltage VS	V_S	-0.3	–	40	V	–	P_5.1.1
Voltage VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_5.1.2
Voltage VDDP	V_{DDP}	-0.3	–	6.0	V	t < 100ms, in Stop Mode only	P_5.1.50
Output voltage VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_5.1.3
Voltage VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_5.1.4
Voltages High Voltage Pins							
Battery Voltage VBAT_SENSE	V_{BAT_SENSE}	-27	–	40	V	–	P_5.1.5
Output voltage HS	V_{HS}	-0.3	–	40	V	–	P_5.1.6
Input voltage at LIN	V_{LIN}	-27	–	40	V	–	P_5.1.7
Input voltage MON_x	$V_{MON\_X\_maxrate}$	-40	–	40	V	–	P_5.1.8
Input voltage LS	V_{LS}	-0.3	–	40	V	–	P_5.1.9
Voltages GPIOs							
Voltage on any port pin	V_{in}	-0.3	–	V_{DDP} +0.3	V	V_{IN} < 5.4V	P_5.1.10
Voltages Others							
Input voltage VAREF	V_{AREF}	-0.3	–	5.3	V	–	P_5.1.11
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_5.1.12
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_5.1.13
ESD Resistivity							
ESD Resistivity **HBM** all pins	V_{ESD1}	-2	–	2	kV	EIA/JESD 22-A114B (1.5kΩ, 100pF)	P_5.1.14

5.5 Parallel Ports (GPIO)

5.5.1 Functional Range

Table 25 Functional Range

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output current on any pin	I_{OH} , I_{OL}	–	–	20	mA	1) 2)	P_5.5.1
Max output current for all GPIOs	I_{max}	–	–	60	mA	1) 2)	P_5.5.2

1) One of these limits must be kept.

2) Not subject to production test, specified by design

5.5.2 DC Parameters

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage (all except XTAL1)	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	–	P_5.5.3
Input high voltage (all except XTAL1)	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	–	P_5.5.4
Input Hysteresis[1)]	HYS	0.11 x V_{DDP}	–	–	V	Series resistance = 0 Ω	P_5.5.5
Output low voltage	V_{OL}	–	–	1.0	V	2) $I_{OL} \le I_{OLmax}$	P_5.5.6
Output low voltage	V_{OL}	–	–	0.4	V	2) $I_{OL} \le$ 3) I_{OLnom}	P_5.5.7
Output high voltage[4)]	V_{OH}	V_{DDP} - 1.0	–	–	V	2) $I_{OH} \ge I_{OHmax}$	P_5.5.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	2)3) $I_{OH} \ge I_{OHnom}$	P_5.5.9
Input leakage current (Port 2)	I_{OZ1}	-400	–	+400	nA	$T_J \le 85°C$, 0 V < V_{IN} < V_{DDP}	P_5.5.10
Input leakage current (all other)[5)]	I_{OZ2}	-5	–	+5	µA	$T_J \le 85°C$, 0.45 V < V_{IN} < V_{DDP}	P_5.5.11

Table 27 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Nominal Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	VDDP < 4.5V	VDDP ≥ 4.5V	VDDP < 4.5V	
Strong Driver	7.5 mA	7.5 mA	2.5 mA	2.5 mA	P_5.5.16
Medium Driver	4 mA	2.5 mA	1.0 mA	1.0 mA	P_5.5.17
Weak Driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA	P_5.5.18

1) Not subject to production test, specified by design.

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < GND$) the voltage on V_{DDP} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10,4 kBit/s)	t_{duty1}	0.417	–	–		[7] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 29)	P_5.6.24
Duty cycle D4 (for worst case at 10,4 kBit/s)	t_{duty2}	–	–	0.590		duty cycle 4 TH_{Rec}(max) = 0.389 × V_S; TH_{Dom}(max) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 30)	P_5.6.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	–	P_5.6.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	–	P_5.6.27
Receiver delay symmetry	$t_{sym,R}$	-1	–	1	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_5.6.28
Duty cycle D5 (for worst case at 40 kBit/s)	t_{duty1}	0.395	–	–		[6] duty cycle 5 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};	P_5.6.29
Duty cycle D6 (for worst case at 40 kBit/s)	t_{duty2}	–	–	0.581		[6] duty cycle 6 TH_{Rec}(max)= 0.422 × V_S; TH_{Dom}(max)= 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 25 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)	P_5.6.30
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	0.5	6	µs	–	P_5.6.31

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	0.5	6	µs	–	P_5.6.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.0	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_5.6.33
Duty cycle D7 (for worst case at 115 kBit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		8) duty cycle D7 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus\_rec(min)}$/2 t_{bit};	P_5.6.34
Duty cycle D8 (for worst case at 115 kBit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		6) duty cycle 8 TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus\_rec(max)}$/2 t_{bit};	P_5.6.35
TxD dominant time out	$t_{timeout}$	6	12	20	ms	8) V_{TxD} = 0 V	P_5.6.36

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) This parameter is not subject to production test
5) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Bus loads:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
7) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
8) Timeout can be disabled optional

5.8.4 Temperature Sensor Module

Table 33 Electrical Characteristics Temperature Sensor Module

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Linear temperature range	T_{RANGE}	-40		175	°C	–	P_5.8.21
Output voltage V_{TEMP} at T_0=273 K (0°C) Mode 1	a	–	0.4893	–	V	1) DVBE_MODE=0 T=273K (0°C)	P_5.8.22
Output voltage V_{TEMP} at T_0=273 K (0°C) Mode 2	a	–	0.5365	–	V	DVBE_MODE=1 T_0=273 K (0°C)	P_5.8.23
Temperature sensitivity b in Mode 1	b	–	1.685	–	mV/K	1) DVBE_MODE=0	P_5.8.24
Temperature sensitivity b Mode 2	b	–	1.834	–	mV/K	DVBE_MODE=1	P_5.8.25
Accuracy_1 2)	Acc_1	-10	–	10	°C	-40°C < T_j < 125°C	P_5.8.26
Accuracy_2	Acc_2	-15	–	15	°C	125°C < T_j < 175°C	P_5.8.27

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement

5.10 High-Voltage Monitor Input

Table 37 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_s	0.5*V_s	0.6*V_s	V	without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.1
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_s	0.06*V_s	0.12*V_s	V	in all modes; without external serial resistor R_s (with R_s: $\Delta V = I_{PD/PU} * R_s$);	P_5.10.2
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = low	$I_{PU, MONx}$	-20	-10	-1	µA	0 V < V_{MON_IN} < V_s - 2 V	P_5.10.3
Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PU, MONx}$	-20	-10	-1	µA	0.6*V_s < V_{MON_IN} < V_s - 2 V	P_5.10.4
Pull-down current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < V_s	P_5.10.5
Pull-down current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high	$I_{PD, MONx}$	4	10	18	µA	2 V < V_{MON_IN} < 0.4*V_s	P_5.10.6
Input leakage current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = low	$I_{LK,I}$	-2	–	2	µA	0 V < V_{MON_IN} < 28 V	P_5.10.7

The Parameters of the analog measurement are listed in the chapter Measurement Interface.

5.11 High Side Switches

5.11.1 Functional Range

Table 38 Functional Range

T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	5.5	–	27	V	–	P_5.11.1
Current range for Sleep Mode / Stop Mode	$I_{HS\ max\ sleep\_pd}$	–	–	40	mA	Cyclic Sense Mode	P_5.11.2
PWM frequency of HS with Slew Rate Control	$f_{PWM\_W\_SR}$	0	–	10	kHz	1) Frequency must be configured in the PWM Generator	P_5.11.3
PWM frequency of HS without Slew Rate Control	f_{PWM_W/O_SR}	0	–	25 2)	kHz	1) Frequency must be configured in the PWM Generator	P_5.11.4

1) Not subject to production test, specified by design.

2) referring to a 47ohm series resistor to charge an external power mos gate

5.11.2 Electrical Characteristics

Table 39 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Maximum ratings							
Output voltage	V_{HSxOUT}	-0.3	–	V_S	V	min. value referred to GND_A	P_5.11.5
Output HS							
ON-State Resistance	R_{ON}	–	–	20	Ω	V_S =5.5 to 27 V, Ids=100mA, higher resistance below V_S =5.5V	P_5.11.6
Output leakage Current	$I_{leakage}$	–	–	2	µA	Output OFF 0 V < V_{XLO} < V_S; T_j < 85 °C	P_5.11.7
Output Slew Rate (rising) with Slew Rate Control	$SR_{raise\_w\_SR}$	1	–	10	V/µs	10% to 90% of V_S V_S = 9 to 18V R_L =300Ω 1)	P_5.11.8