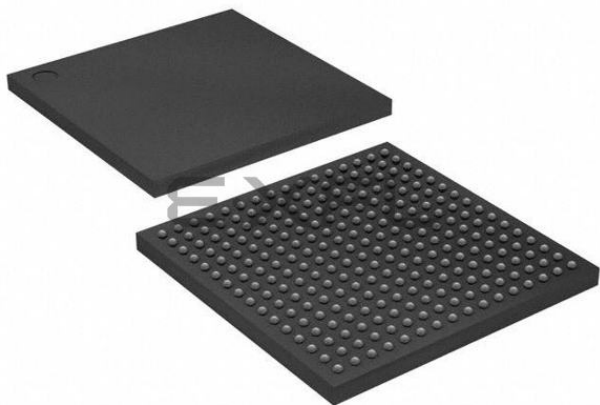




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	7925
Number of Logic Elements/Cells	101440
Total RAM Bits	4976640
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a100t-1ftg256i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	—	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	—	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	—	100	°C

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system consult [UG483](#), 7 Series FPGAs PCB Design and Pin Planning Guide.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in [UG482](#): 7 Series FPGAs GTP Transceiver User Guide.
- Voltages are specified for the temperature range of $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	—	—	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	—	—	V
I_{REF}	V_{REF} leakage current per pin	—	—	15	μA
I_L	Input or output leakage current per pin (sample-tested)	—	—	15	μA
$C_{IN}^{(2)}$	Die input capacitance at the pad	—	—	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 3.3\text{V}$	90	—	330	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 2.5\text{V}$	68	—	250	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.8\text{V}$	34	—	220	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.5\text{V}$	23	—	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.2\text{V}$	12	—	120	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3\text{V}$	68	—	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8\text{V}$	45	—	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	—	—	25	mA
$I_{BATT}^{(3)}$	Battery supply current	—	—	150	nA
$R_{IN_TERM}^{(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices	44	60	83	Ω

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Table 9: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO}-0.405$	$V_{CCO}-0.300$	$V_{CCO}-0.190$	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \bar{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	-0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	-0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	-13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	-8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	-13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	-8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	-8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	-13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: Artix-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: Artix-7 Device Production Software and Speed Specification Release

Device	Speed Grade		
	1.0V		0.9V
	-3	-2/-2L	-1
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 9](#).

Table 14: Networking Applications Interface Performances

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽¹⁾⁽²⁾

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).

Table 23: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.81	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.55	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.76/−0.05	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.42/−0.01	0.47/−0.01	0.53/−0.01	0.70/−0.05	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.79/−0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

DSP48E1 Switching Characteristics

Table 28: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.25/ 0.25	0.32/ 0.27	0.42/ 0.27	0.54/ 0.23	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B} input to M register CLK using multiplier	2.40/ −0.01	2.76/ −0.01	3.29/ −0.01	4.31/ −0.07	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.29/ −0.02	1.48/ −0.02	1.76/ −0.02	2.29/ −0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B} input to P register CLK using multiplier	4.02/ −0.28	4.60/ −0.28	5.48/ −0.28	6.95/ −0.48	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.93/ −0.73	4.50/ −0.73	5.35/ −0.73	6.73/ −1.68	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.73/ −0.28	1.98/ −0.28	2.35/ −0.28	2.80/ −0.48	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.54/ −0.26	1.76/ −0.26	2.10/ −0.26	2.54/ −0.45	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.32/ −0.15	1.51/ −0.15	1.80/ −0.15	2.13/ −0.25	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.36/ −0.03	0.43/ −0.03	0.52/ −0.03	0.68/ 0.14	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Table 28: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{\text{DSPDCK_RSTC_CREG}}/T_{\text{DSPCKD_RSTC_CREG}}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{\text{DSPDCK_RSTD_DREG}}/T_{\text{DSPCKD_RSTD_DREG}}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{\text{DSPDCK_RSTM_MREG}}/T_{\text{DSPCKD_RSTM_MREG}}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{\text{DSPDCK_RSTP_PREG}}/T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{\text{DSPDO_A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{\text{DSPDO_D_P_MULT}}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{\text{DSPDO_B_P}}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.33	1.53	1.82	2.22	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\{\text{ACOUT}; \text{BCOUT}\}}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT_MULT}}}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT}}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns

Table 34: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3				
MMCM_T _{OUTDUTY}	MMCM output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time	100.00	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMDCK_DEN} / T _{MMCMCKD_DEN}	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{MMCMDCK_DWE} / T _{MMCMCKD_DWE}	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3				
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/−0.46	2.89/−0.46	3.34/−0.46	5.66/−0.52	ns
		XC7A200T	3.03/−0.50	3.27/−0.50	3.79/−0.50	6.66/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7A100T	2.44/−0.62	2.80/−0.62	3.36/−0.62	2.15/−0.49	ns
		XC7A200T	2.57/−0.63	2.94/−0.63	3.52/−0.63	2.32/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7A100T	2.78/−0.32	3.15/−0.32	3.78/−0.32	2.47/−0.60	ns
		XC7A200T	2.91/−0.33	3.29/−0.33	3.94/−0.33	2.64/−0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 47: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		$1/2 V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

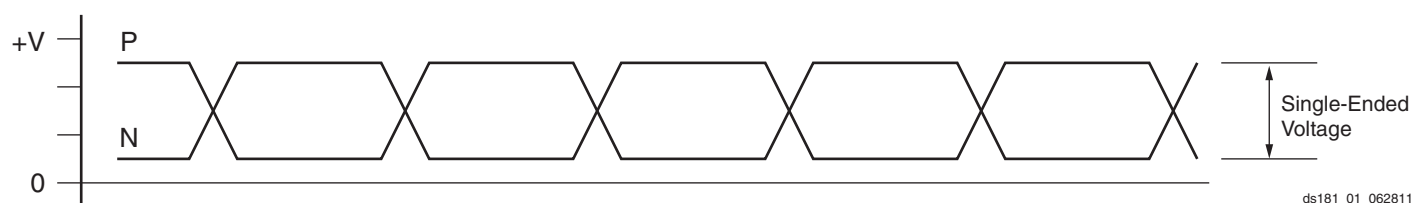


Figure 1: Single-Ended Peak-to-Peak Voltage

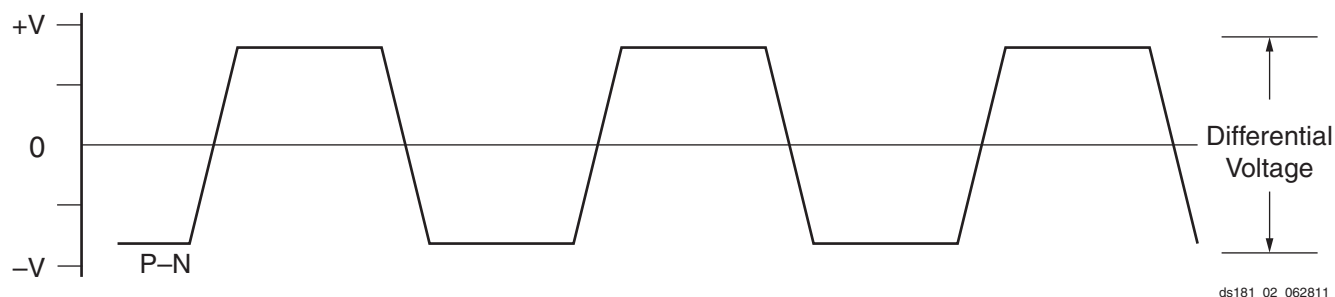


Figure 2: Differential Peak-to-Peak Voltage

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 48: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further information.

Table 49: GTP Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1		-2L		
			Package Type								
			FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	
F _{GTPMAX}	Maximum GTP transceiver data rate		6.6	5.4	6.6	5.4	3.75	3.75	3.75	3.75	Gb/s
F _{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F _{GTPRANGE}	PLL line rate range	1	3.2–6.6		3.2–6.6		3.2–3.75		3.2–3.75		Gb/s
		2	1.6–3.3		1.6–3.3		1.6–3.2		1.6–3.2		Gb/s
		4	0.8–1.65		0.8–1.65		0.8–1.6		0.8–1.6		Gb/s
		8	0.5–0.825		0.5–0.825		0.5–0.8		0.5–0.8		Gb/s
F _{GTPPLL} RANGE	GTP transceiver PLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz

Table 50: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTPDRPCLK}	GTPDRPCLK maximum frequency	175	175	156	125	MHz

Table 51: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range		60	–	660	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	20% – 80%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

Table 54: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTPTX}	Serial data rate range		0.500	—	F _{GTPMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	—	50	—	ps
T _{FTX}	TX fall time	20%–80%	—	50	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	140	ns
TJ _{6.6}	Total Jitter ⁽²⁾⁽³⁾	6.6 Gb/s	—	—	0.30	UI
DJ _{6.6}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.15	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	—	—	0.30	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	—	—	0.30	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.15	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	—	—	0.30	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.15	UI
TJ _{3.2}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁴⁾	—	—	0.2	UI
DJ _{3.2}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.1	UI
TJ _{3.2L}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁵⁾	—	—	0.32	UI
DJ _{3.2L}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁶⁾	—	—	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁷⁾	—	—	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.06	UI
TJ ₅₀₀	Total Jitter ⁽²⁾⁽³⁾	500 Mb/s	—	—	0.1	UI
DJ ₅₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
- Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 55: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTPMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	5000	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.6}	Sinusoidal Jitter ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter.

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Table 62: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference⁽⁵⁾						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted. On-chip reference variation is $\pm 1\%$.

Configuration Switching Characteristics

Table 63: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5.00	5.00	5.00	5.00	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 11 . Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13 . Added $MMCM_T_{FBDELAY}$ while adding $MMCM_$ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35 . In Table 36 through Table 43 , updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46 .
02/13/12	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1 . In Table 2 , revised V_{CCO} for the 3.3V HR I/O banks and updated T_j . Updated the notes in Table 5 . Added MGTAVCC and MGTAVTT power supply ramp times to Table 7 . Rearranged Table 8 , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10 . Revised the specifications in Table 11 . Revised V_{IN} in Table 47 . Updated the eFUSE Programming Conditions section and removed the endurance table. Added the table. Revised F_{TXIN} and F_{RXIN} in Table 53 . Revised I_{CCADC} and updated Note 1 in Table 62 . Revised DDR LVDS transmitter data width in Table 14 . Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63 . Updated Note 1 in Table 33 .
06/01/12	1.3	Reorganized entire data sheet including adding Table 40 and Table 44 . Updated T_{SOL} in Table 1 . Updated I_{BATT} and added R_{IN_TERM} to Table 3 . Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8 , updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 10 . Updated V_{OL} in Table 11 . Updated Table 14 and removed notes 2 and 3. Updated Table 15 . Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 27 , updated Reset Delays section including Note 10 and Note 11 . In Table 53 , replaced F_{TXOUT} with F_{GLK} . Updated many of the XADC specifications in Table 62 and added Note 2 . Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 63 to Table 34 and Table 35 .

Date	Version	Description
09/20/12	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24. Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.
02/01/13	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOVBVDDP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCCK} and added the Internal Configuration Access Port section.

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