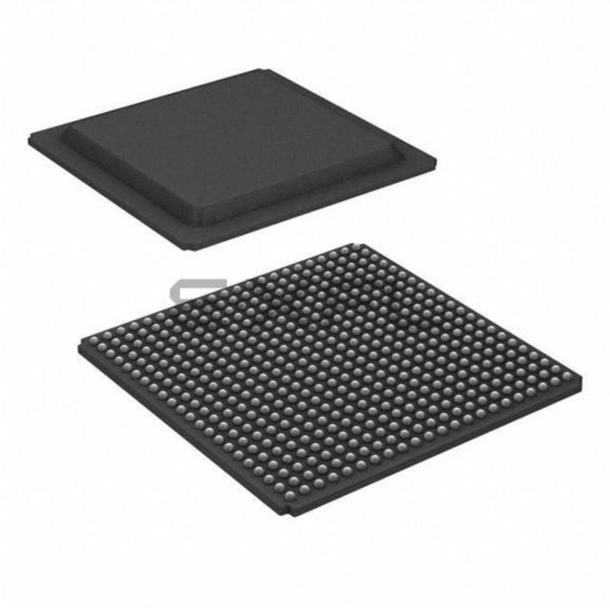
# AMD Xilinx - XC7A100T-L2FGG484E Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 7925 |
| Number of Logic Elements/Cells | 101440 |
| Total RAM Bits | 4976640 |
| Number of I/O | 285 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a100t-l2fgg484e |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Min | Typ[(1)] | Max | Units |
|---|---|---|---|---|---|
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[(1)]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.40 | 100 | –0.40 | 100 |
| $V_{CCO}$ + 0.45 | 100 | –0.45 | 61.7 |
| $V_{CCO}$ + 0.50 | 100 | –0.50 | 25.8 |
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7A100T | 155 | 155 | 155 | 108 | mA |
| | | XC7A200T | 328 | 328 | 328 | 232 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 5 | 5 | 5 | 5 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7A100T | 36 | 36 | 36 | 36 | mA |
| | | XC7A200T | 73 | 73 | 73 | 73 | mA |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 11 | 11 | 11 | 11 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$ and $V_{CCO}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} – V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7V$, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} – V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7V$, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

Table 6 shows the minimum current, in addition to $I_{CCQ}$, that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after $V_{CCINT}$ is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

*Table 6:* **Power-On Current for Artix-7 Devices(1)**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|
| | Typ(2) | Typ(2) | Typ(2) | Typ(2) | |
| XC7A100T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A200T | $I_{CCINTQ}$ + 340 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 80 | mA |

**Notes:**

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$ | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$ | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} – V_{CCAUX} > 2.625V$ | $T_J$ = 100°C(1) | – | 500 | ms |
| | | $T_J$ = 85°C(1) | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |

**Notes:**

1. Based on 240,000 power cycles with nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with worst case $V_{CCO}$ of 3.465V.

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.98 | 1.85 | 1.97 | 2.23 | 2.27 | 2.42 | 2.63 | 3.06 | 2.92 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.98 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.35 | 1.47 | 1.73 | 1.96 | 1.92 | 2.13 | 2.56 | 2.61 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.08 | 2.57 | 2.69 | 2.95 | 3.18 | 3.14 | 3.35 | 3.78 | 3.83 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.08 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.79 | 1.91 | 2.17 | 2.40 | 2.36 | 2.57 | 2.99 | 3.05 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.08 | 1.98 | 2.10 | 2.35 | 2.58 | 2.54 | 2.76 | 3.18 | 3.23 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.08 | 1.54 | 1.66 | 1.92 | 2.15 | 2.11 | 2.32 | 2.75 | 2.80 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.38 | 1.51 | 1.76 | 1.97 | 1.95 | 2.16 | 2.59 | 2.62 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.80 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.67 | 1.79 | 2.04 | 2.24 | 2.23 | 2.45 | 2.87 | 2.89 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.31 | 1.43 | 1.68 | 1.91 | 1.87 | 2.09 | 2.51 | 2.56 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.68 | 1.80 | 2.06 | 2.24 | 2.25 | 2.46 | 2.89 | 2.89 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.94 | 1.95 | 2.17 | 2.59 | 2.59 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.80 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.72 | 1.69 | 1.90 | 2.32 | 2.37 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.23 | 1.35 | 1.60 | 1.80 | 1.79 | 2.01 | 2.43 | 2.45 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.79 | 1.78 | 1.99 | 2.42 | 2.44 | ns |

Table 17 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 17:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.19 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.30 | ns |

## Input/Output Logic Switching Characteristics

*Table 18:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK | 0.48/0.02 | 0.54/0.02 | 0.76/0.02 | 0.40/–0.07 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin setup/hold with respect to CLK | 0.60/0.01 | 0.70/0.01 | 1.13/0.01 | 0.88/–0.35 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin setup/hold with respect to CLK without Delay | 0.01/0.27 | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY) | 0.02/0.27 | 0.02/0.29 | 0.02/0.33 | 0.01/0.33 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.11 | 0.11 | 0.13 | 0.14 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY) | 0.11 | 0.12 | 0.14 | 0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.41 | 0.44 | 0.51 | 0.54 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) | 0.41 | 0.44 | 0.51 | 0.55 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.53 | 0.57 | 0.66 | 0.71 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out | 0.96 | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum pulse width, SR inputs | 0.61 | 0.72 | 0.72 | 0.68 | ns, Min |

*Table 19:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.67/–0.11 | 0.71/–0.11 | 0.84/–0.11 | 0.60/–0.18 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.10 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.37/0.21 | 0.44/0.21 | 0.80/0.21 | 0.62/–0.25 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.69/–0.14 | 0.73/–0.14 | 0.89/–0.14 | 0.60/–0.18 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.10 | ns |
| **Combinatorial** | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.83 | 0.96 | 1.16 | 1.36 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| $T_{RQ\_OLOGIC}$ | SR pin to OQ/TQ out | 0.72 | 0.80 | 0.95 | 1.12 | ns |
| $T_{GSRQ\_OLOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_OLOGIC}$ | Minimum pulse width, SR inputs | 0.64 | 0.74 | 0.74 | 0.68 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 20:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.14 | 0.02/0.15 | 0.02/0.17 | 0.02/0.21 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.45/–0.01 | 0.50/–0.01 | 0.72/–0.01 | 0.35/–0.11 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.10/0.33 | –0.10/0.36 | –0.10/0.40 | –0.17/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.03/0.19 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.12/0.12 | 0.14/0.14 | 0.17/0.17 | 0.19/0.19 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.53 | 0.54 | 0.66 | 0.67 | ns |
| **Propagation Delays** | | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.11 | 0.11 | 0.13 | 0.14 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

*Table 23:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **IO_FIFO Clock to Out Delays** | | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs | 0.55 | 0.60 | 0.68 | 0.81 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags | 0.55 | 0.61 | 0.77 | 0.55 | ns |
| **Setup/Hold** | | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK | 0.47/0.02 | 0.51/0.02 | 0.58/0.02 | 0.76/–0.05 | ns |
| $T_{IFFCCK\_WREN}$ /$T_{IFFCKC\_WREN}$ | WREN to WRCLK | 0.42/–0.01 | 0.47/–0.01 | 0.53/–0.01 | 0.70/–0.05 | ns |
| $T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK | 0.53/0.02 | 0.58/0.02 | 0.66/0.02 | 0.79/–0.02 | ns |
| **Minimum Pulse Width** | | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 266.67 | 200.00 | 200.00 | 200.00 | MHz |

## CLB Switching Characteristics

*Table 24:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.10 | 0.11 | 0.13 | 0.15 | ns, Max |
| $T_{ILO\_2}$ | An – Dn LUT address to AMUX/CMUX | 0.27 | 0.30 | 0.36 | 0.41 | ns, Max |
| $T_{ILO\_3}$ | An – Dn LUT address to BMUX_A | 0.42 | 0.46 | 0.55 | 0.65 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.94 | 1.05 | 1.27 | 1.51 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.62 | 0.69 | 0.84 | 1.01 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.58 | 0.66 | 0.83 | 0.98 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.60 | 0.68 | 0.82 | 0.98 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.68 | 0.75 | 0.90 | 1.08 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.51 | 0.57 | 0.69 | 0.82 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.62 | 0.69 | 0.82 | 0.99 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.42 | 0.48 | 0.58 | 0.69 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.53 | 0.59 | 0.71 | 0.86 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.52 | 0.58 | 0.70 | 0.84 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.40 | 0.44 | 0.53 | 0.62 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.47 | 0.53 | 0.66 | 0.73 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{AS}/T_{AH}$ | $A_N$ – $D_N$ input to CLK on A – D flip-flops | 0.07/0.12 | 0.09/0.14 | 0.11/0.18 | 0.11/0.20 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | $A_X$ – $D_X$ input to CLK on A – D flip-flops | 0.06/0.19 | 0.07/0.21 | 0.09/0.26 | 0.09/0.31 | ns, Min |
| | $A_X$ – $D_X$ input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08 | 0.66/0.09 | 0.81/0.11 | 0.97/0.12 | ns, Min |
| $T_{CECK\_CLB}/$ $T_{CKCE\_CLB}$ | CE input to CLK on A – D flip-flops | 0.15/0.00 | 0.17/0.00 | 0.21/0.01 | 0.34/–0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | 0.38/0.03 | 0.43/0.04 | 0.53/0.05 | 0.62/0.05 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 0.95 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.53 | 0.59 | 0.71 | 0.83 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.70 | 0.83 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412 | 1286 | 1098 | 1098 | MHz |

## Block RAM and FIFO Switching Characteristics

*Table 27:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$(1) | Clock CLK to DOUT output (without output register)(2)(3) | 1.85 | 2.13 | 2.46 | 2.87 | ns, Max |
| | Clock CLK to DOUT output (with output register)(4)(5) | 0.64 | 0.74 | 0.89 | 1.02 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)(2)(3) | 2.77 | 3.04 | 3.84 | 5.30 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)(4)(5) | 0.73 | 0.81 | 0.94 | 1.11 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with cascade (without output register)(2) | 2.61 | 2.88 | 3.30 | 3.76 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register)(4) | 1.16 | 1.28 | 1.46 | 1.56 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs(6) | 0.76 | 0.87 | 1.05 | 1.14 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs(7) | 0.94 | 1.02 | 1.15 | 1.30 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.78 | 0.85 | 0.94 | 1.10 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register) | 2.56 | 2.81 | 3.55 | 4.90 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.68 | 0.76 | 0.89 | 1.05 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.75 | 0.88 | 1.07 | 1.15 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.84 | 0.93 | 1.08 | 1.29 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK\_ADDRA}$/$T_{RCKC\_ADDRA}$ | ADDR inputs(8) | 0.45/0.31 | 0.49/0.33 | 0.57/0.36 | 0.77/0.45 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode(9) | 0.58/0.60 | 0.65/0.63 | 0.74/0.67 | 0.92/0.76 | ns, Min |
| $T_{RDCK\_DI\_RF}$/$T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode(9) | 0.20/0.29 | 0.22/0.34 | 0.25/0.41 | 0.29/0.38 | ns, Min |
| $T_{RDCK\_DI\_ECC}$/$T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode(9) | 0.50/0.43 | 0.55/0.46 | 0.63/0.50 | 0.78/0.54 | ns, Min |
| $T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only(9) | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.38/0.48 | ns, Min |
| $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode(9) | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.55/0.77 | ns, Min |
| $T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.58/0.35 | 0.64/0.37 | 0.74/0.40 | 0.92/0.48 | ns, Min |
| $T_{RCCK\_EN}$/$T_{RCKC\_EN}$ | Block RAM enable (EN) input | 0.35/0.20 | 0.39/0.21 | 0.45/0.23 | 0.57/0.26 | ns, Min |
| $T_{RCCK\_REGCE}$/$T_{RCKC\_REGCE}$ | CE input of output register | 0.24/0.15 | 0.29/0.15 | 0.36/0.16 | 0.40/0.19 | ns, Min |
| $T_{RCCK\_RSTREG}$/$T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.29/0.07 | 0.32/0.07 | 0.35/0.07 | 0.41/0.07 | ns, Min |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of the RST Pins** | | | | | | |
| $T_{\text{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}}$/ $T_{\text{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/ 0.11 | 0.46/ 0.13 | 0.55/ 0.15 | 0.63/ 0.40 | ns |
| $T_{\text{DSPDCK\_RSTC\_CREG}}$/ $T_{\text{DSPCKD\_RSTC\_CREG}}$ | RSTC input to C register CLK | 0.07/ 0.10 | 0.08/ 0.11 | 0.09/ 0.12 | 0.13/ 0.11 | ns |
| $T_{\text{DSPDCK\_RSTD\_DREG}}$/ $T_{\text{DSPCKD\_RSTD\_DREG}}$ | RSTD input to D register CLK | 0.44/ 0.07 | 0.50/ 0.08 | 0.59/ 0.09 | 0.67/ 0.08 | ns |
| $T_{\text{DSPDCK\_RSTM\_MREG}}$/ $T_{\text{DSPCKD\_RSTM\_MREG}}$ | RSTM input to M register CLK | 0.21/ 0.22 | 0.23/ 0.24 | 0.27/ 0.28 | 0.28/ 0.35 | ns |
| $T_{\text{DSPDCK\_RSTP\_PREG}}$/ $T_{\text{DSPCKD\_RSTP\_PREG}}$ | RSTP input to P register CLK | 0.27/ 0.01 | 0.30/ 0.01 | 0.35/ 0.01 | 0.43/ 0.00 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | |
| $T_{\text{DSPDO\_A\_CARRYOUT\_MULT}}$ | A input to CARRYOUT output using multiplier | 3.79 | 4.35 | 5.18 | 6.61 | ns |
| $T_{\text{DSPDO\_D\_P\_MULT}}$ | D input to P output using multiplier | 3.72 | 4.26 | 5.07 | 6.41 | ns |
| $T_{\text{DSPDO\_B\_P}}$ | B input to P output not using multiplier | 1.53 | 1.75 | 2.08 | 2.48 | ns |
| $T_{\text{DSPDO\_C\_P}}$ | C input to P output | 1.33 | 1.53 | 1.82 | 2.22 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | |
| $T_{\text{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.55 | 0.63 | 0.74 | 0.87 | ns |
| $T_{\text{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}}$ | {A, B} input to CARRYCASCOUT output using multiplier | 4.06 | 4.65 | 5.54 | 7.03 | ns |
| $T_{\text{DSPDO\_D\_CARRYCASCOUT\_MULT}}$ | D input to CARRYCASCOUT output using multiplier | 3.97 | 4.54 | 5.40 | 6.81 | ns |
| $T_{\text{DSPDO\_\{A, B\}\_CARRYCASCOUT}}$ | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77 | 2.03 | 2.41 | 2.88 | ns |
| $T_{\text{DSPDO\_C\_CARRYCASCOUT}}$ | C input to CARRYCASCOUT output | 1.58 | 1.81 | 2.15 | 2.62 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | |
| $T_{\text{DSPDO\_ACIN\_P\_MULT}}$ | ACIN input to P output using multiplier | 3.65 | 4.19 | 5.00 | 6.40 | ns |
| $T_{\text{DSPDO\_ACIN\_P}}$ | ACIN input to P output not using multiplier | 1.37 | 1.57 | 1.88 | 2.44 | ns |
| $T_{\text{DSPDO\_ACIN\_ACOUT}}$ | ACIN input to ACOUT output | 0.38 | 0.44 | 0.53 | 0.63 | ns |
| $T_{\text{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}}$ | ACIN input to CARRYCASCOUT output using multiplier | 3.90 | 4.47 | 5.33 | 6.79 | ns |
| $T_{\text{DSPDO\_ACIN\_CARRYCASCOUT}}$ | ACIN input to CARRYCASCOUT output not using multiplier | 1.61 | 1.85 | 2.21 | 2.84 | ns |
| $T_{\text{DSPDO\_PCIN\_P}}$ | PCIN input to P output | 1.11 | 1.28 | 1.52 | 1.82 | ns |
| $T_{\text{DSPDO\_PCIN\_CARRYCASCOUT}}$ | PCIN input to CARRYCASCOUT output | 1.36 | 1.56 | 1.85 | 2.21 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | |
| $T_{\text{DSPCKO\_P\_PREG}}$ | CLK PREG to P output | 0.33 | 0.37 | 0.44 | 0.54 | ns |
| $T_{\text{DSPCKO\_CARRYCASCOUT\_PREG}}$ | CLK PREG to CARRYCASCOUT output | 0.52 | 0.59 | 0.69 | 0.84 | ns |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.73 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 3.12 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 4.60 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.99 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 6.84 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.65 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.81 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 6.77 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 1.02 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 7.24 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 3.04 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 7.17 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 3.20 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 363.77 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 310.08 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 210.44 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 191.28 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 150.13 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 140.10 | MHz |

*Table 32:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| $T_{BHCCK\_CE}/T_{BHCKC\_CE}$ | CE pin setup and hold | 0.19/0.13 | 0.22/0.15 | 0.28/0.21 | 0.35/0.08 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 394.00 | MHz |

*Table 33:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $T_{DCD\_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7A100T | 0.27 | 0.33 | 0.36 | 0.48 | ns |
| | | XC7A200T | 0.40 | 0.48 | 0.54 | 0.69 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

*Table 34:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| $MMCM\_F_{MIN\_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM\_F_{MAX\_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM\_F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |

*Table 34:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| MMCM_F$_{\text{BANDWIDTH}}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_T$_{\text{STATPHAOFFSET}}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| MMCM_T$_{\text{OUTJITTER}}$ | MMCM output jitter | Note 3 | | | | |
| MMCM_T$_{\text{OUTDUTY}}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| MMCM_T$_{\text{LOCKMAX}}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| MMCM_F$_{\text{OUTMAX}}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_F$_{\text{OUTMIN}}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_T$_{\text{EXTFDVAR}}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_RST$_{\text{MINPULSE}}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_F$_{\text{PFDMAX}}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_F$_{\text{PFDMIN}}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_T$_{\text{FBDELAY}}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{\text{MMCMDCK\_PSEN}}$/<br>$T_{\text{MMCMCKD\_PSEN}}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{\text{MMCMDCK\_PSINCDEC}}$/<br>$T_{\text{MMCMCKD\_PSINCDEC}}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{\text{MMCMCKO\_PSDONE}}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{\text{MMCMDCK\_DADDR}}$/<br>$T_{\text{MMCMCKD\_DADDR}}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{\text{MMCMDCK\_DI}}$/<br>$T_{\text{MMCMCKD\_DI}}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{\text{MMCMDCK\_DEN}}$/<br>$T_{\text{MMCMCKD\_DEN}}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{\text{MMCMDCK\_DWE}}$/<br>$T_{\text{MMCMCKD\_DWE}}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{\text{MMCMCKO\_DRDY}}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{\text{DCK}}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.  
   See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{\text{VCO}}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F$_{\text{OUTMIN}}$ is 0.036 MHz.

## PLL Switching Characteristics

*Table 35:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| PLL_F$_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_F$_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_F$_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| PLL_F$_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| PLL_F$_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_F$_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| PLL_F$_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| PLL_T$_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_T$_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | |
| PLL_T$_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| PLL_T$_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| PLL_F$_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_F$_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| PLL_T$_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| PLL_RST$_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_F$_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| PLL_F$_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_T$_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| T$_{PLLDCK\_DADDR}$/ T$_{PLLCKD\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| T$_{PLLDCK\_DI}$/T$_{PLLCKD\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| T$_{PLLDCK\_DEN}$/ T$_{PLLCKD\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| T$_{PLLDCK\_DWE}$/ T$_{PLLCKD\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| T$_{PLLCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| F$_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F$_{VCO}$/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 41:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.[1] | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF[2] without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7A100T | 2.69/–0.46 | 2.89/–0.46 | 3.34/–0.46 | 5.66/–0.52 | ns |
| | | XC7A200T | 3.03/–0.50 | 3.27/–0.50 | 3.79/–0.50 | 6.66/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

*Table 42:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.[1] | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF[2] with MMCM | XC7A100T | 2.44/–0.62 | 2.80/–0.62 | 3.36/–0.62 | 2.15/–0.49 | ns |
| | | XC7A200T | 2.57/–0.63 | 2.94/–0.63 | 3.52/–0.63 | 2.32/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 43:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.[1] | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF[2] with PLL | XC7A100T | 2.78/–0.32 | 3.15/–0.32 | 3.78/–0.32 | 2.47/–0.60 | ns |
| | | XC7A200T | 2.91/–0.33 | 3.29/–0.33 | 3.94/–0.33 | 2.64/–0.63 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 44:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.31 | –0.38/1.46 | –0.38/1.76 | –0.16/1.89 | ns |

*Table 45:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

*Table 46:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7A100T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |
| | | XC7A200T | SBG484 | 111 | ps |
| | | | FBG484 | 109 | ps |
| | | | FBG676 | 121 | ps |
| | | | FFG1156 | 151 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

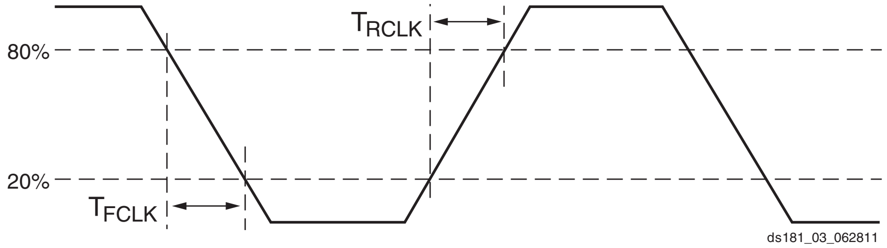

*Figure 3:* **Reference Clock Timing Parameters**

*Table 52:* **GTP Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time. | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 2.3 x$10^6$ | UI |

*Table 53:* **GTP Transceiver User Clock Switching Characteristics**(1)

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

*Table 54:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 50 | – | ps |
| $T_{FTX}$ | TX fall time | 20%–80% | – | 50 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{6.6}$ | Total Jitter(2)(3) | 6.6 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.6}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.2}$ | Total Jitter(2)(3) | 3.20 Gb/s(4) | – | – | 0.2 | UI |
| $DJ_{3.2}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.2L}$ | Total Jitter(2)(3) | 3.20 Gb/s(5) | – | – | 0.32 | UI |
| $DJ_{3.2L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(6) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(7) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total Jitter(2)(3) | 500 Mb/s | – | – | 0.1 | UI |
| $DJ_{500}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

*Table 62:* **XADC Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DCLK Duty Cycle | | | 40 | – | 60 | % |
| **XADC Reference**[5] | | | | | | |
| External Reference | $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| On-Chip Reference | | Ground $V_{REFP}$ pin to AGND,<br>$T_j$ = –40°C to 100°C | 1.2375 | 1.25 | 1.2625 | V |

**Notes:**

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

## Configuration Switching Characteristics

*Table 63:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$[1] | Program latency | 5.00 | 5.00 | 5.00 | 5.00 | ms, Max |
| $T_{POR}$[1] | Power-on reset (50 ms ramp rate time) | 10/50 | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time) | 10/35 | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| $T_{PROGRAM}$ | Program pulse width | 250.00 | 250.00 | 250.00 | 250.00 | ns, Min |
| **CCLK Output (Master Mode)** | | | | | | |
| $T_{ICCK}$ | Master CCLK output delay | 150.00 | 150.00 | 150.00 | 150.00 | ns, Min |
| $T_{MCCKL}$ | Master CCLK clock Low time duty cycle | 40/60 | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $T_{MCCKH}$ | Master CCLK clock High time duty cycle | 40/60 | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $F_{MCCK}$ | Master CCLK frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| | Master CCLK frequency for AES encrypted x16 | 50.00 | 50.00 | 50.00 | 35.00 | MHz, Max |
| $F_{MCCK\_START}$ | Master CCLK frequency at start of configuration | 3.00 | 3.00 | 3.00 | 3.00 | MHz, Typ |
| $F_{MCCKTOL}$ | Frequency tolerance, master mode with respect to nominal CCLK | ±50 | ±50 | ±50 | ±50 | %, Max |
| **CCLK Input (Slave Modes)** | | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{SCCK}$ | Slave CCLK frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **EMCCLK Input (Master Mode)** | | | | | | |
| $T_{EMCCKL}$ | External master CCLK Low time | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{EMCCKH}$ | External master CCLK High time | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{EMCCK}$ | External master CCLK frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |

| Date | Version | Description |
|---|---|---|
| 09/20/12 | 1.4 | In Table 1, updated the descriptions, changed $V_{IN}$ and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet.<br>Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and $T_{CINCK}/T_{CKCIN}$ from Table 24.Changed $F_{PFDMAX}$ conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated $T_{POR}$. |
| 02/01/13 | 1.5 | Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications.<br>Revised $I_{DCIN}$ and $I_{DCOUT}$ and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46.<br>Updated $D_{VPPIN}$ in Table 47. Updated $V_{IDIFF}$ in Table 48. Removed $T_{LOCK}$ and $T_{PHASE}$ and revised $F_{GCLK}$ in Table 51. Updated $T_{DLOCK}$ in Table 52. Updated Table 53. In Table 54, updated $T_{RTX}$, $T_{FTX}$, $V_{TXOOBVDPP}$, and revised Note 1 through Note 7. In Table 55, updated $RX_{SST}$ and $RX_{PPMTOL}$ and revised Note 4 through Note 7. In Table 60, revised and added Note 1.<br>Revised the maximum external channel input ranges in Table 62. In Table 63, revised $F_{MCCK}$ and added the Internal Configuration Access Port section. |