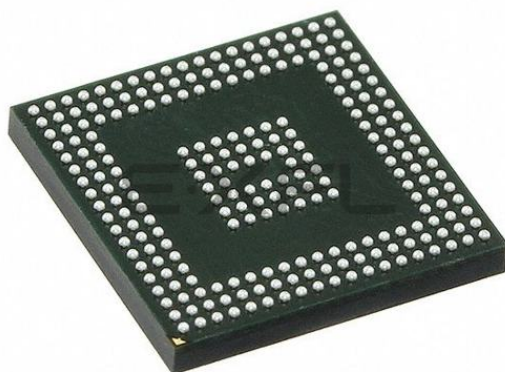




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	737280
Number of I/O	106
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	238-LFBGA, CSPBGA
Supplier Device Package	238-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a12t-1cpg236c

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 6 shows the minimum current, in addition to I_{CCQ} , that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: Power-On Current for Artix-7 Devices⁽¹⁾

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
	Typ ⁽²⁾	Typ ⁽²⁾	Typ ⁽²⁾	Typ ⁽²⁾	
XC7A100T	$I_{CCINTQ} + 170$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7A200T	$I_{CCINTQ} + 340$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 80$	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.10	-0.10
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.7	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.10	-0.10
PCI33_3	-0.500	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.50	-0.50
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.00	-13.00
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.90	-8.90
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.00	-13.00
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.90	-8.90
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.00	-8.00
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.40	-13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see [UG471](#): 7 Series FPGAs SelectIO Resources User Guide.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 12](#) correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: Artix-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 13](#) lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: Artix-7 Device Production Software and Speed Specification Release

Device	Speed Grade		
	1.0V		0.9V
	-3	-2/-2L	-1
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_II_F	0.65	0.73	0.80	0.85	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
HSTL_I_18_F	0.67	0.75	0.82	0.87	1.13	1.26	1.51	1.72	1.70	1.92	2.34	2.37	ns
HSTL_II_18_F	0.66	0.75	0.81	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.85	1.18	1.30	1.56	1.77	1.75	1.96	2.39	2.42	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.85	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
LVC MOS33_S4	1.26	1.34	1.41	1.62	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVC MOS33_S8	1.26	1.34	1.41	1.62	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVC MOS33_S12	1.26	1.34	1.41	1.62	3.09	3.21	3.46	3.69	3.65	3.87	4.29	4.34	ns
LVC MOS33_S16	1.26	1.34	1.41	1.62	3.40	3.52	3.77	4.00	3.97	4.18	4.60	4.65	ns
LVC MOS33_F4	1.26	1.34	1.41	1.62	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVC MOS33_F8	1.26	1.34	1.41	1.62	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS33_F12	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS33_F16	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS25_S4	1.12	1.20	1.27	1.43	3.13	3.26	3.51	3.72	3.70	3.91	4.34	4.37	ns
LVC MOS25_S8	1.12	1.20	1.27	1.43	2.88	3.01	3.26	3.49	3.45	3.67	4.09	4.14	ns
LVC MOS25_S12	1.12	1.20	1.27	1.43	2.48	2.60	2.85	3.08	3.05	3.26	3.68	3.73	ns
LVC MOS25_S16	1.12	1.20	1.27	1.43	2.82	2.94	3.20	3.43	3.39	3.60	4.03	4.08	ns
LVC MOS25_F4	1.12	1.20	1.27	1.43	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS25_F8	1.12	1.20	1.27	1.43	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS25_F12	1.12	1.20	1.27	1.43	2.16	2.29	2.54	2.77	2.73	2.95	3.37	3.42	ns
LVC MOS25_F16	1.12	1.20	1.27	1.43	2.01	2.13	2.39	2.61	2.58	2.79	3.21	3.26	ns
LVC MOS18_S4	0.74	0.83	0.89	0.94	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
LVC MOS18_S8	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S12	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S16	0.74	0.83	0.89	0.94	1.52	1.65	1.90	2.13	2.09	2.31	2.73	2.78	ns
LVC MOS18_S24	0.74	0.83	0.89	0.94	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVC MOS18_F4	0.74	0.83	0.89	0.94	1.45	1.57	1.82	2.05	2.01	2.23	2.65	2.70	ns
LVC MOS18_F8	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F12	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F16	0.74	0.83	0.89	0.94	1.40	1.52	1.77	2.00	1.97	2.18	2.60	2.65	ns
LVC MOS18_F24	0.74	0.83	0.89	0.94	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVC MOS15_S4	0.77	0.86	0.93	0.98	2.05	2.18	2.43	2.50	2.62	2.84	3.26	3.15	ns
LVC MOS15_S8	0.77	0.86	0.93	0.98	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVC MOS15_S12	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns
LVC MOS15_S16	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns

Table 23: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.81	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.55	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.76/−0.05	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.42/−0.01	0.47/−0.01	0.53/−0.01	0.70/−0.05	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.79/−0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 25: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.98	1.09	1.32	1.54	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	2.18	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.54/0.28	0.60/0.30	0.72/0.35	0.96/0.40	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.27/0.55	0.30/0.60	0.37/0.70	0.43/0.71	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/0.18	0.77/0.21	0.94/0.26	1.11/0.29	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.38/0.10	0.43/0.12	0.53/0.17	0.62/0.13	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.39/0.10	0.44/0.11	0.53/0.17	0.63/0.12	ns, Min
Clock CLK						
T _{MPW_LRAM}	Minimum pulse width	1.05	1.13	1.25	0.82	ns, Min
T _{MCP}	Minimum clock period	2.10	2.26	2.50	1.64	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 26: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	1.19	1.33	1.61	1.89	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.77	2.15	2.53	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	1.12	1.23	1.46	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.37/0.10	0.41/0.12	0.51/0.17	0.59/0.13	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.37/0.10	0.42/0.11	0.52/0.17	0.60/0.12	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.33/0.34	0.37/0.37	0.44/0.43	0.54/0.47	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.77	0.86	0.98	1.04	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 27: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCKK_RSTRAM}/T_{RCKC_RSTRAM}$	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	0.40/0.47	ns, Min
$T_{RCKK_WEA}/T_{RCKC_WEA}$	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	0.64/0.23	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	0.77/0.44	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	0.71/0.44	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.25	ns, Max
$T_{RREC_RST}/T_{RREM_RST}$	FIFO reset recovery and removal timing ⁽¹¹⁾	1.87/–0.81	2.07/–0.81	2.37/–0.81	2.44/–0.71	ns, Max
Maximum Frequency						
$F_{MAX_BRAM_WF_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode	509.68	460.83	388.20	315.66	MHz
$F_{MAX_BRAM_RF_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B	509.68	460.83	388.20	315.66	MHz
$F_{MAX_BRAM_RF_DELAYED_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses	447.63	404.53	339.67	268.96	MHz
$F_{MAX_CAS_WF_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode	467.07	418.59	345.78	273.30	MHz
$F_{MAX_CAS_RF_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled	467.07	418.59	345.78	273.30	MHz
$F_{MAX_CAS_RF_DELAYED_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	405.35	362.19	297.35	226.60	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	509.68	460.83	388.20	315.66	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	215.38	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- These parameters include both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 28: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.25/ 0.25	0.32/ 0.27	0.42/ 0.27	0.54/ 0.23	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B} input to M register CLK using multiplier	2.40/ −0.01	2.76/ −0.01	3.29/ −0.01	4.31/ −0.07	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.29/ −0.02	1.48/ −0.02	1.76/ −0.02	2.29/ −0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B} input to P register CLK using multiplier	4.02/ −0.28	4.60/ −0.28	5.48/ −0.28	6.95/ −0.48	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.93/ −0.73	4.50/ −0.73	5.35/ −0.73	6.73/ −1.68	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.73/ −0.28	1.98/ −0.28	2.35/ −0.28	2.80/ −0.48	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.54/ −0.26	1.76/ −0.26	2.10/ −0.26	2.54/ −0.45	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.32/ −0.15	1.51/ −0.15	1.80/ −0.15	2.13/ −0.25	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.36/ −0.03	0.43/ −0.03	0.52/ −0.03	0.68/ 0.14	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Table 28: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T _{DSPCKO_P_MREG}	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
T _{DSPCKO_CARRYCASCOUT_MREG}	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
T _{DSPCKO_CARRYCASCOUT_ADREG_MULT}	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
T _{DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F _{MAX}	With all registers used	628.93	550.66	464.25	363.77	MHz
F _{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	310.08	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	349.28	305.62	257.47	210.44	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	191.28	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	397.30	346.26	290.44	223.26	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	397.30	346.26	290.44	223.26	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	150.13	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	140.10	MHz

Clock Buffers and Networks

Table 29: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.10	0.14	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	394.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 30: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.11	1.26	1.54	1.56	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 31: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.76	0.99	1.24	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.34	0.39	0.52	0.72	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.81	0.85	1.09	0.96	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/−0.46	2.89/−0.46	3.34/−0.46	5.66/−0.52	ns
		XC7A200T	3.03/−0.50	3.27/−0.50	3.79/−0.50	6.66/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7A100T	2.44/−0.62	2.80/−0.62	3.36/−0.62	2.15/−0.49	ns
		XC7A200T	2.57/−0.63	2.94/−0.63	3.52/−0.63	2.32/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7A100T	2.78/−0.32	3.15/−0.32	3.78/−0.32	2.47/−0.60	ns
		XC7A200T	2.91/−0.33	3.29/−0.33	3.94/−0.33	2.64/−0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T _{PSCS} /T _{PHCS}	Setup and hold of I/O clock	−0.38/1.31	−0.38/1.46	−0.38/1.76	−0.16/1.89	ns

Table 45: Sample Window

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling error at receiver pins ⁽¹⁾	0.59	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO ⁽²⁾	0.35	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 46: Package Skew

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew ⁽¹⁾	XC7A100T	CSG324	113	ps
			FTG256	120	ps
			FGG484	144	ps
			FGG676	153	ps
		XC7A200T	SBG484	111	ps
			FBG484	109	ps
			FBG676	121	ps
			FFG1156	151	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 47: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		$1/2 V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

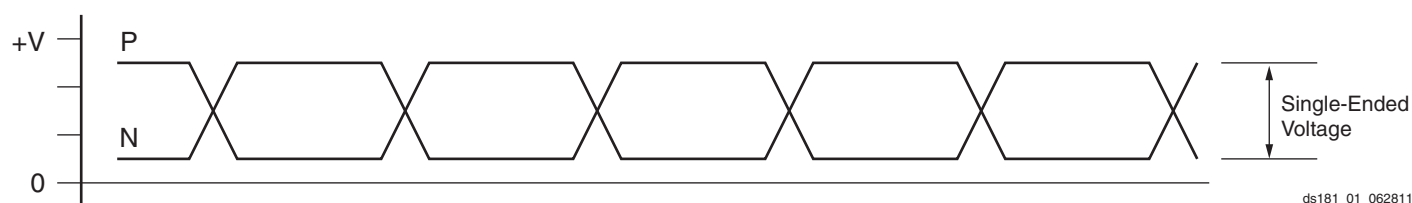


Figure 1: Single-Ended Peak-to-Peak Voltage

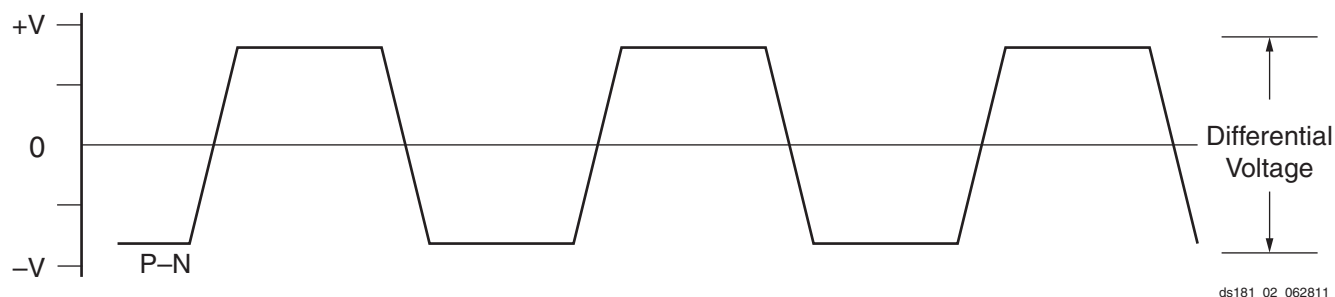


Figure 2: Differential Peak-to-Peak Voltage

Table 54: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTPTX}	Serial data rate range		0.500	–	F _{GTPMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	50	–	ps
T _{FTX}	TX fall time	20%–80%	–	50	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{6.6}	Total Jitter ⁽²⁾⁽³⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{3.2}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁴⁾	–	–	0.2	UI
DJ _{3.2}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.2L}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.32	UI
DJ _{3.2L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₅₀₀	Total Jitter ⁽²⁾⁽³⁾	500 Mb/s	–	–	0.1	UI
DJ ₅₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
- Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 55: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTPMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELEC_IDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	5000	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.6}	Sinusoidal Jitter ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using $RXOUT_DIV = 1, 2, \text{ and } 4$.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 1.6 GHz and $RXOUT_DIV = 1$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 4$.
- Composite jitter.

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: CEI-6G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

XADC Specifications

Table 62: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Unipolar operation	–	–	±8	LSBs
		Bipolar operation	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 11 . Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13 . Added $MMCM_T_{FBDELAY}$ while adding $MMCM_$ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35 . In Table 36 through Table 43 , updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46 .
02/13/12	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1 . In Table 2 , revised V_{CCO} for the 3.3V HR I/O banks and updated T_j . Updated the notes in Table 5 . Added MGTAVCC and MGTAVTT power supply ramp times to Table 7 . Rearranged Table 8 , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10 . Revised the specifications in Table 11 . Revised V_{IN} in Table 47 . Updated the eFUSE Programming Conditions section and removed the endurance table. Added the table. Revised F_{TXIN} and F_{RXIN} in Table 53 . Revised I_{CCADC} and updated Note 1 in Table 62 . Revised DDR LVDS transmitter data width in Table 14 . Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63 . Updated Note 1 in Table 33 .
06/01/12	1.3	Reorganized entire data sheet including adding Table 40 and Table 44 . Updated T_{SOL} in Table 1 . Updated I_{BATT} and added R_{IN_TERM} to Table 3 . Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8 , updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 10 . Updated V_{OL} in Table 11 . Updated Table 14 and removed notes 2 and 3. Updated Table 15 . Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 27 , updated Reset Delays section including Note 10 and Note 11 . In Table 53 , replaced F_{TXOUT} with F_{GLK} . Updated many of the XADC specifications in Table 62 and added Note 2 . Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 63 to Table 34 and Table 35 .

Date	Version	Description
09/20/12	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24. Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.
02/01/13	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOVBVDDP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCCK} and added the Internal Configuration Access Port section.