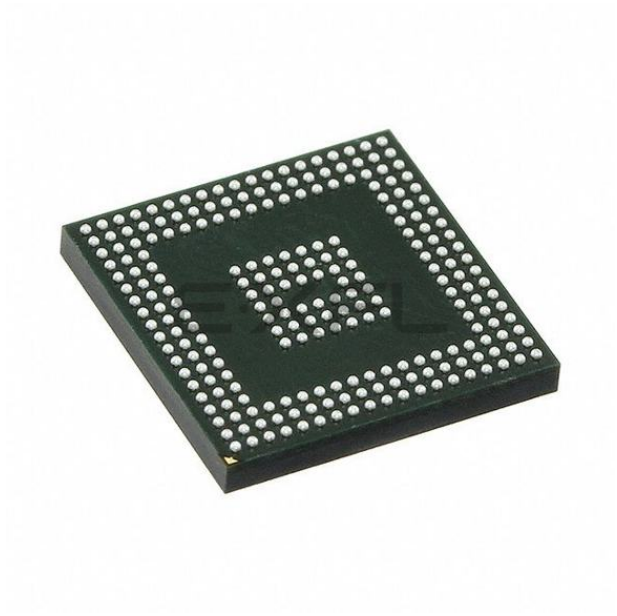

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	737280
Number of I/O	106
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	238-LFBGA, CSPBGA
Supplier Device Package	238-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a12t-1cpg238c

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies (6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies (6)	–	+260	°C
T_j	Maximum junction temperature(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applied to DC signals.
5. For maximum undershoot and overshoot AC specifications, see Table 4.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.95	1.00	1.05	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}	Block RAM supply voltage	0.95	1.00	1.05	V
V_{CCO}(3)(4)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
V_{IN}(5)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage for V_{REF} and differential I/O standards	–0.20	–	2.625	V
I_{IN}(6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(7)	Battery voltage	1.0	–	1.89	V
GTP Transceiver					
$V_{MGTAVCC}$(8)(9)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(8)(9)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.500	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: **Artix-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: **Artix-7 Device Production Software and Speed Specification Release**

Device	Speed Grade			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

Table 14: **Networking Applications Interface Performances**

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Input/Output Logic Switching Characteristics

Table 18: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.40/–0.07	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/–0.35	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.68	ns, Min

Table 19: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.60/–0.18	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/–0.10	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/–0.25	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.60/–0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/–0.10	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.68	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 20: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.14	0.02/0.15	0.02/0.17	0.02/0.21	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.45/–0.01	0.50/–0.01	0.72/–0.01	0.35/–0.11	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.10/0.33	–0.10/0.36	–0.10/0.40	–0.17/0.40	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.04/0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.03/0.19	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.04/0.19	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.12/0.12	0.14/0.14	0.17/0.17	0.19/0.19	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.53	0.54	0.66	0.67	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.11	0.11	0.13	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 21: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.44/–0.25	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	0.60/–0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	0.46/–0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/–0.15	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/–0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.83	0.92	1.11	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	2.22	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	363.77	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	310.08	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	210.44	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	191.28	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	150.13	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	140.10	MHz

Table 32: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.16	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.19/0.13	0.22/0.15	0.28/0.21	0.35/0.08	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	394.00	MHz

Table 33: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global clock tree duty-cycle distortion(1)	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7A100T	0.27	0.33	0.36	0.48	ns
		XC7A200T	0.40	0.48	0.54	0.69	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.14	0.14	0.14	0.14	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 34: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the UG482: *7 Series FPGAs GTP Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: **PCI Express Protocol Characteristics(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: **CEI-6G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 60: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2(1)	0.60	–	UI
	6144.0(1)	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 61: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

XADC Specifications

Table 62: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Unipolar operation	–	–	±8	LSBs
		Bipolar operation	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Table 62: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 63: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency	5.00	5.00	5.00	5.00	ms, Max
T_{POR}(1)	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 11. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35. In Table 36 through Table 43, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46.
02/13/12	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Updated the notes in Table 5. Added MGTAVCC and MGTAVTT power supply ramp times to Table 7. Rearranged Table 8, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10. Revised the specifications in Table 11. Revised V_{IN} in Table 47. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the table. Revised F_{TXIN} and F_{RXIN} in Table 53. Revised I_{CCADC} and updated Note 1 in Table 62. Revised DDR LVDS transmitter data width in Table 14. Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63. Updated Note 1 in Table 33.
06/01/12	1.3	Reorganized entire data sheet including adding Table 40 and Table 44. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8, updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 10. Updated V_{OL} in Table 11. Updated Table 14 and removed notes 2 and 3. Updated Table 15. Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 27, updated Reset Delays section including Note 10 and Note 11. In Table 53, replaced F_{TXOUT} with F_{GLK}. Updated many of the XADC specifications in Table 62 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 63 to Table 34 and Table 35.

Date	Version	Description
09/20/12	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24.Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.
02/01/13	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOOBVDPP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCCK} and added the Internal Configuration Access Port section.

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